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The influence of the band structure of epitaxial graphene on SiC on the transistor characteristics

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Abstract
We fabricated high-mobility field-effect transistors based on epitaxial graphene synthesized by vacuum graphitization of both the Si- and C-faces of SiC. Room-temperature field-effect mobilities > 4,000 cm^2/Vs for both electrons and holes were achieved, although with wide distributions. By using a high-k gate dielectric, we were able to measure transistor characteristics in a wide carrier density range, where the mobility is seen to decrease as the carrier density increases. We formulate a simple semiclassical model of electrical transport in graphene, and explain the sub-linear dependence of conductivity on carrier density from the view point of few-layer graphene energy band structure. Our analysis reveals important differences between few-layer graphene energy dispersion on the SiC Si- and C-faces, providing the first evidence based on electrical device characteristics for the theoretically proposed energy dispersion difference between graphene synthesized on these two faces of SiC.

1. Introduction
Graphene has attracted tremendous research interest, due to both its scientific significance and technological potentials [1], with the latter especially in ultrafast electronics. Field-effect transistors (FETs) have been demonstrated with room-temperature mobilities up to 15,000 cm^2/Vs using few layer graphene (FLG) exfoliated from graphite [2]. It is desirable for device manufacturing and integration, however, to synthesize graphene on a solid state substrate instead of exfoliation and placing. To this end, graphitization of SiC represents a promising approach towards epitaxial synthesis of graphene [3, 4]. Transistors using epitaxially synthesized graphene on SiC have been demonstrated [5, 6, 7].

In this work, we synthesized graphene on both the (0001) and $(000\bar{1})$ surfaces (referred to respectively as the Si- and C-faces hereafter) of 4H SiC, and fabricated graphene FETs using a high-k dielectric HfO_2 as the gate dielectric. Room-temperature field-effect mobilities > 4,000 cm^2/Vs were achieved. The use of the high-k dielectric enabled us to measure transfer characteristics in a wide carrier density range. We can therefore analyze the I_D-V_G data and explain the bending of the I_D-V_G curves in terms of the band structure of FLG. The physical picture we present is consistent with data in early work [7, 8]. Our analysis revealed important differences between few-layer graphene energy dispersion on the SiC Si- and C-faces, providing the first evidence based on electrical device characteristics for the theoretically proposed energy dispersion difference between graphene synthesized on the two faces of SiC.

Section 2 describes device fabrication and characterization. Section 3 and 4 present data analysis for devices using graphene synthesized on the C- and Si-faces, respectively. Section 5 draws conclusions as well as discusses our physical picture as related to data in early work. Mathematical details are in the Appendix.

2. Experiment

Our epitaxial synthesis and thickness estimate of graphene on the Si-face have been described elsewhere [9]. The average thicknesses of both Si-face samples were estimated to be ~ 2 ML by Auger electron spectroscopy (AES) (this thickness does not include the C-rich "buffer layer" at the SiC/graphene interface [9]). The synthesis on the C-face starts from a hydrogen etched substrate, and graphene formation is observed over the temperature range 1200-1400 ºC. The low energy electron diffraction (LEED) pattern of the Si-face graphene reveals a six-fold pattern, the same as described in the literature [3, 4]. The pattern of the C-face graphene is more complex, revealing a six-fold pattern together with additional spots at 30° ± φ with angles φ ranging from 6 to 13°. This pattern is similar to that observed by Hass et al [4] (although their angle φ was 2.2°), and following those authors we interpret it as indicative of rotational disorder in the C-face graphene layers. Thickness estimate by AES was not reliable for thicker films on the C-face, and for that reason we use heights as measured by atomic force microscopy (AFM) as further discussed below.

Transistors with the structure shown in Fig. 1(a) were fabricated at Lincoln Labs in a process described elsewhere [7], using two Si- and two C-face graphene samples as listed Table I, each 1 cm × 1 cm in size. The HfO_2 gate dielectric is 40 nm thick with a dielectric constant ε_r = 23, resulting in a unit area gate capacitance C_i = 509 nF/cm^2.
The patterned graphene is totally covered by the gate/dielectric stack, the source/drain (S/D) metals, or their overlap. Edges of the graphene islands translate to edges in the top surface. The thickness of the graphene films on the C-face was estimated by measuring by AFM the average height of the covered graphene islands in completed devices. This measurement avoids the uncertainty caused by different interaction of the AFM tip with different materials [2], but assumes that the HfO_2 or S/D metal films have same thicknesses on graphene and bare SiC. To verify the AFM result, transmission electron microscopy (TEM) was performed on one device on sample 20 (C-face). The high resolution images (to be published) reveals ~27 graphene MLs with a total thickness of ~9 nm, as well as a 3 to 4 nm thick unknown layer between epitaxial graphene and HfO_2. This unknown layer is tentatively attributed to an organic residue. The TEM result indicates that the AFM-measured height is the actual graphene thickness plus 3 to 4 nm of the unknown layer, consistent with the 12 to 13 nm AFM-measured height on the two C-face samples.

Figure 1(b) shows the channel conductivity σ of many devices on sample 20 (C-face), measured at room temperature with a drain voltage V_D = 0.1 V, versus the gate voltage V_G. Here, we name the grounded electrode S, and the biased contact D, although this is not perfectly appropriate for the ambipolar FETs [7]. For a low V_D = 0.1 V, however, the difference between the electron and the hole sources is simply ignored. Similar to [7], large non-uniformity was observed. Field-effect mobilities, μ, were calculated from the largest slopes of the transfer curves above and below the minimum conductance voltage V_m for electrons and holes, respectively. Figure 1(c) shows σ-V_G

curves for two representative devices on sample 29 (Si-face), featuring wide linear portions of the curves near V_m to be discussed later; the non-uniformity among devices for this face is also large.

3. Analysis of C-face graphene FETs

Figure 1(b) shows that the σ-V_G curves bend downward at high gate biases, i.e. the mobility decreases with increasing $|V_G - V_m|$. To show this effect more clearly, the σ-V_G curve of one representative FET on this sample is shown in Fig. 2.

To explain this behavior, we start from monolayer graphene, with a linear energy dispersion $E = \hbar v_F k$, where k is the wavevector and $v_F \approx 10^8$ cm/s the Fermi velocity. For simplicity, we assume that carrier scattering can be characterized by a scattering time τ without considering the microscopic scattering mechanisms. Under an applied electric field F, the carrier distribution in the momentum space is shifted by $\hbar\Delta k = qF\tau$, where q is the electron charge. While the velocity of each carrier is still v_F, a net drift velocity v_d results. A simple expression can be found by averaging the velocity projection along the field direction over all carriers for zero absolute temperature (see Appendix):

$$v_d = v_F \frac{\Delta k}{k_F} = v_F \frac{qF\tau}{\hbar k_F} = v_F^{\,2} \frac{qF\tau}{E_F} \qquad (1)$$

For temperature T = 0 K, we also have

$$E_F = \hbar v_F k_F = \hbar v_F \sqrt{\pi n}\,, \qquad (2)$$

where n is the carrier density, considering the spin degeneracy of 2 and the valley degeneracy of 2 [10, 11]. Therefore, the conductivity

$$\sigma = qn\left(\frac{q v_F^{\,2}}{E_F}\tau\right) = \frac{q^2 v_F}{\hbar\sqrt{\pi}} \cdot \sqrt{n} \cdot \tau\,. \qquad (3)$$

The general case of $T > 0$ K is discussed in the Appendix, where Eq. (3) is corrected by a factor that depends only on the ratio $E_F/(k_B T)$. For $n > \sim 4\times10^{12}$ cm^{-2}, the temperature correction is negligible even at room temperature.

In a graphene FET, the minimum conductivity gate voltage V_m is usually not 0 V, due to unintentional doping, and hence the carrier density $n = C_i(V_G - V_m)/q$. Therefore, Eq. (3) means that $\sigma \propto \sqrt{|V_G - V_m|}$ at sufficiently high carrier densities and low temperatures, assuming a constant τ. This is consistent with the transfer characteristics of the back-gated single layer graphene FET demonstrated by Lemme *et al* (Fig. 2 of Ref. [8]). Indeed, the Appendix shows that our semiclassical model is consistent with that transfer curve all over the gate bias range when finite temperature is considered (see Fig. A2).

Back to our device in Fig. 2, we first determine the minimum conductance voltage V_m = 0.69 V by linearly extrapolating the several data points near the minimum conductivity on both sides. We then fit the data to $\sigma = K\sqrt{|V_G - V_m|} + \sigma_0$ for 1.6 V $\geq |V_G|$ $\geq$ 0.8 V for the hole conduction part of the curve. The offset parameter σ_0 was introduced for the following reason: The minimum conductivity of an epitaxial graphene FET on SiC is more than can be explained by thermally excited carriers. Such epitaxial graphene FETs thereby exhibit significantly lower on-off ratio [6, 7] than their exfoliated graphene counterparts [2, 8]. Since the mechanism of the minimum conductivity is

unclear, we introduce σ_0 as a fitting parameter. To fit the hole conduction, σ_0 = 2.71 mS, reasonably close to the measured minimum conductivity.

In the V_G range where we obtained the above fit, the effect of finite temperature is negligible: for V_G = –0.8 V, the hole concentration is 4.75 × 10^{12} cm^{-2}, where the temperature correction factor $\sqrt{G_T} \cdot F_T \approx 0.99$ (see Fig. A3 in the Appendix). We then consider room temperature using Eq. (A9), and fit the hole conduction portion of the curve to

$$\sigma = K'\sqrt{n} \cdot \sqrt{G_T(\frac{\hbar v_F k_F}{k_B T})} \cdot F_T(\frac{\hbar v_F k_F}{k_B T}) + \sigma_0, \qquad (4)$$

where $\sqrt{G_T} \cdot F_T$ was calculated numerically (see Fig. A3), and σ_0 = 2.71 mS had been obtained by fitting the the temperature insensitive bias range. The hole density *n* was related to V_G by $qn = C_i|V_G - V_m|$. This fit is plotted in Fig. 2. Interestingly, for $|V_G| \leq$ 1.6 V, very good fitting was obtained, suggesting that the band structure of our C-face FLG is linear, as of the single layer graphene. This is seemingly contradictory to FLG and graphite band structures that comprise parabolic conduction band bottoms and valence band tops [2, 12, 13].

In this regard it should be noted that our C-face FLG is misoriented as evidenced by LEED, as discussed in Section 2, consistent with other work [3, 4, 14]. It has been shown [4, 15, 16] that the energy dispersion of misorented FLG is linear, similar to the massless fermions of the single layer graphene, due to the loss of A-B stacking [14]. Indeed, the retention of the graphene linear band structure is considered an advantage of the epitaxial FLG on the SiC C-face over the Si-face counterpart [4, 14].

For V_G more negative than –1.6 V, the σ-V_G curve of this device bends down faster than the fit, and no reasonable fit to $\sigma = K\sqrt{|V_G - V_m|} + \sigma_0$ can be found if this range is included. Some other FETs even exhibit a decrease in σ at high $|V_G|$ as shown in Fig. 1(b). Similar fast bend-down or even decrease in σ at high $|V_G|$ was observed in other work using epitaxial graphene on SiC and the same dielectric deposition process [7], while a back-gated FET without deposited dielectric using exfoliated graphene [8] exhibit transfer characteristics consistent with Eq. (4) at all gate biases. This discrepancy will be discussed in Sect. 5. Gate leakage is excluded as a cause; the measured gate current in always negligible compared to the drain current.

The same trend is seen for electron conduction, although there are not enough data points for fitting due to the fast bend-down at high V_G and a positive V_m = 0.69 V.

4. Analysis of Si-face graphene FETs

Figure 3 shows the σ-V_G curve of a well-behaved Si-face graphene FET on sample 25. Similar as in Fig. 2, V_m = 0.75 V was determined by linearly extrapolating the curve near the minimum conductivity. We then fit the data to $\sigma = K\sqrt{|V_G - V_m|} + \sigma_0$ for 2 V ≥ $|V_G|$ ≥ 1 V for the hole conduction part of the curve. Here, σ_0 = 2.51 mS, reasonably close to the measured minimum conductivity. Similar to the above analysis of C-face FLG FETs, we attempted to fit the data over the range –2 V ≤ $V_G \leq V_m$ to Eq. (4), taking into account the finite temperature correction. As plotted in Fig. 3, good agreement is seen only down

to V_G = –0.6 V. At lower overdrive voltages $|V_G - V_m|$, however, the σ-V_G data is linear.

To explain the behavior shown in Fig. 3, we consider the band structures of A-B stacked FLG or bilayer graphene [12, 13, 17]. The conduction (valence) bands are quadratic close to the bottoms (tops), and become linear at larger momentums [12, 13, 17]. At low $|V_G - V_m|$, the conduction (valence) band is filled up (down) to a level within the quadratic energy dispersion, therefore the transfer curve exhibit a constant slope (mobility) as expected for a conventional semiconductor with parabolic bands. At sufficiently high $|V_G - V_m|$, the Fermi level is beyond the transition between quadratic and linear dispersions, therefore the transfer curve resembles that of a single layer graphene FET.

Again, since V_m = +0.75 V, there are not enough electron conduction data for reliable fitting, but the trend of the curve is qualitatively the same: linear close to V_m and sub-linear at higher V_G.

5. Discussion and Conclusions

We have presented a simple Drude-like model of electrical transport in graphene FETs to explain the decreasing mobility with increasing gate overdrive voltage $|V_G - V_m|$. This model reasonably fits the transfer curves of well-behaved transistors in our work. It is also consistent with data from a FET based on exfoliated, single layer graphene in other work [8]. Most interestingly, our fits reveal that the energy dispersion of FLG on the SiC C-face is linear, while that on the Si-face comprise a quadratic portion at lower energies. The difference between the FET characteristics on the two faces is pronounced for all well-behaved devices in this work, and even for some less well-behaved devices: For the Si-face graphene, the linear portion of the σ-V_G curve near the minimum conductivity is ~1 V, and the transition between the linear and sub-linear dependences is relatively abrupt. Figure 1(c) shows these features with two additional devices; the two are representative of well-behaved and less-well behaved device. On the C-face, however, the apparent linear range of the σ-V_G curve is only ~0.4 V. The difference between the FLG films on the two faces is attributed to different orientational orders in the two cases.

The validity of our simple model hinges on the assumption of a scattering time independent of the carrier density. Various scattering mechanisms, such as short range scatterers [18, 19], ionized impurities [18, 19], graphene acoustic phonons [19], surface phonons in the gate dielectric [20], and types of disorder including vacancies [19] and ripples [21], have been studied for exfoliated graphene. The early work by Novoselov *et al* [2] showed linear transfer characteristics up to $n \sim 7 \times 10^{12}$ cm^{-2}, probably due to the dominance of Coulomb scattering [18, 19], where $\tau \propto \sqrt{n}$ leads to $\sigma \propto n$ in Eq. (3). Others observed sublinear σ-n [22] due to short range scattering [18, 19]. For surface phonons, $\sigma \propto E_F \propto \sqrt{n}$ for realistic graphene-dielectric distances [20], implying near constant τ. For our epitaxial graphene FETs with moderate mobilities compared to exfoliated graphene [2, 22], we expect many mechanisms to coexist, among which the surface phonons and morphological disorder dominate, due to the use of the high-k dielectric [20] and the rough surface morphology (see AFM images in Refs. [9] and [23]), respectively. For the morphological disorder, it is reasonable to assume the mean free path $v_F\tau$ as determined by surface roughness and average graphene domain size, thus

independent of the carrier density. Given the coexistence of many mechanisms and the possible dominance of the two with near constant τ, our assumption of a constant τ seems reasonable for a range of carrier densities. This assumption should also be reasonable for the back-gated device of Ref. [8], given the moderate mobility comparable to ours, although the scattering mechanisms may be different. The poor fits of our model to the data at high overdrive voltages, however, suggests the failure of this assumption at high carrier densities, where mechanisms such as short range scattering [18, 19] becomes more important.

In summary, we have fabricated high-mobility FETs using epitaxial graphene synthesized by vacuum graphitizing the Si- and C-faces of SiC. Analysis of the electrical data reveals the important difference between the band structures of FLG formed on the C- and Si-faces, providing the first device electrical characteristics evidence for the difference in energy dispersions of FLG on the two faces of SiC.

Appendix

Each carrier is shifted in the momentum space by $\hbar\Delta k = qF\tau$ by an electric field F. The velocity projection to the direction of the field is $v_x = v_F\cos\theta'$, where the angles θ and θ' are related by $\tan\theta' = k\sin\theta / (\Delta k + k\cos\theta)$ as shown in Fig. A1. Hence the drift velocity is

$$v_d = \frac{\int_0^\infty dk \int_0^{2\pi} d\theta [k\cos\theta' f(k)]}{2\pi \int_0^\infty dk [kf(k)]} v_F , \qquad \text{(A1)}$$

where $f(k) = 1/\{1+\exp[\hbar v_F(k-k_F)/k_BT]\}$ is the Fermi distribution, and k_B is the Boltzmann constant.

At this point, to simplify the physical picture, we consider the $T = 0$ K case, where Eq. (A1) reduces to

$$v_d = \frac{\int_0^{k_F} dk \int_0^{2\pi} d\theta \left[k\cos\left(\tan^{-1} \frac{k\sin\theta}{\Delta k + k\cos\theta} \right) \right]}{\pi k_F^{\,2}} v_F ; \qquad \text{(A2)}$$

consideration of finite temperatures is deferred until we discuss temperature dependence. Equation (A2) is still too complicated to analytically evaluate. Notice in Fig. A1 that only the carriers in the shaded areas contribute to the drift velocity. For $\Delta k << k_F$, the contribution of the shaded area is easily calculated:

$$v_d = \frac{2\int_{-\pi/2}^{\pi/2} (v_F\cos\theta)\cdot\Delta k\cdot(k_F\, d\theta\cos\theta)}{\pi k_F^{\,2}} . \qquad \text{(A3)}$$

Taking the integral, we simply get Eq. (1) for $\Delta k << k_F$ and $T = 0$ K.

Although Eq. (A1) is general, we have so far only given an analytical expression of v_d for $T = 0$ K. Here we consider the general case of finite temperatures, once again for $\Delta k << k_F$, which is valid in practical device operation. Assuming the electric field and the momentum shift Δk are in the x direction, we consider that for each k_y the distribution $f(k_x, k_y)$ is shifted to $f(k_x-\Delta k, k_y)$, and that for each carrier the x direction projection of the velocity is $v_F \cdot k_x / k$. The drift velocity can therefore be calculated as:

$$v_d = \frac{4\int_0^\infty dk_y \int_0^\infty \left(v_F \frac{k_x}{k} \right) \left[f(k_x - \Delta k, k_y) - f(k_x, k_y) \right] dk_x}{2\pi \int_0^\infty f(k) dk}. \quad \text{(A4)}$$

Since Δk is small, we have

$$f(k_x - \Delta k, k_y) - f(k_x, k_y) = -\frac{\partial f}{\partial k_x} \Delta k. \quad \text{(A5)}$$

Inserting (A5) into (A4), we get

$$v_d = \frac{4v_F \int_0^\infty dk_y \int_0^\infty \left(\frac{k_x}{k} \right) \left(-\frac{\partial f}{\partial k_x} \right) \Delta k dk_x}{2\pi \int_0^\infty f(k) dk}. \quad \text{(A6)}$$

It can be shown that

$$v_d = v_F \frac{\Delta k}{k_F} \cdot F_T \left(\frac{\hbar v_F k_F}{k_B T} \right), \quad \text{(A7)}$$

where the temperature factor F_T is a function of the ratio $\hbar v_F k_F / (k_B T)$ and approaches 1 as $\hbar v_F k_F / (k_B T) \to \infty$.

For $T > 0$ K, the carrier density

$$n = 4 \cdot \frac{1}{4\pi^2} \cdot 2\pi \int_0^\infty f(k) dk \equiv \frac{k_F^{\,2}}{\pi} \cdot G_T \left(\frac{\hbar v_F k_F}{k_B T} \right). \quad \text{(A8)}$$

Again the temperature dependence factor G_T depends only on $\hbar v_F k_F / (k_B T)$ and approaches 1 as ratio $\hbar v_F k_F / (k_B T) \to \infty$.

The conductivity is therefore

$$\sigma = \frac{q^2 v_F}{\hbar \sqrt{\pi}} \cdot \tau \cdot \sqrt{n} \cdot \sqrt{G_T \left(\frac{\hbar v_F k_F}{k_B T} \right)} \cdot F_T \left(\frac{\hbar v_F k_F}{k_B T} \right). \quad \text{(A9)}$$

The temperature correction factors G_T and F_T are calculated numerically. Figure A2 shows $\sqrt{n} \cdot \sqrt{G_T} \cdot F_T$ versus n at T = 300 K, where k_F is related to n by Eq. (2). This curve is a scaled version of the σ versus $|V_G - V_m|$ curve for a monolayer graphene FET. Without fitting to the data in Fig. 2 of Ref. [8], we qualitatively state that the shape of the curve in Fig. A2 agrees with the hole and electron conduction portions of the transfer curve there.

Figure A3 shows n at T = 300 K versus $\hbar v_F k_F$ as compared to k_F^2/π, as well as the temperature correction factor $\sqrt{G_T} \cdot F_T$ versus $\hbar v_F k_F$. The top axis gives k_F for reference. For $n = 4 \times 10^{12}$ cm^{-2}, $\sqrt{G_T} \cdot F_T = 0.98$ and the difference between n and k_F^2/π is negligible, therefore the effect of room temperature is negligible above $n = 4 \times 10^{12}$ cm^{-2}.

The analysis in the Appendix is valid only for Dirac Fermions, i.e. for monolayer graphene or mis-oriented FLG.

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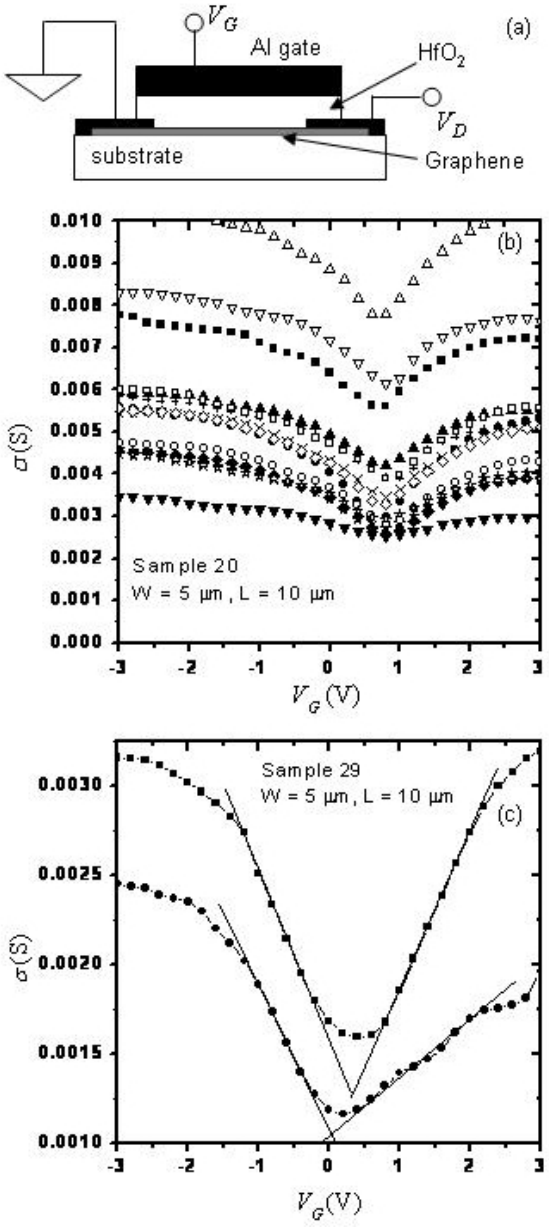

Fig. 1. (a) Device structure. (b) Transfer characteristics (channel conductivity σ vs. gate bias V_G) of devices using C-face graphene on sample 20. (c) σ-V_G curves for two representative devices Si-face graphene on sample 29. The straight lines are visual guidance to emphasize the wide linear ranges of these curves to be discussed later.

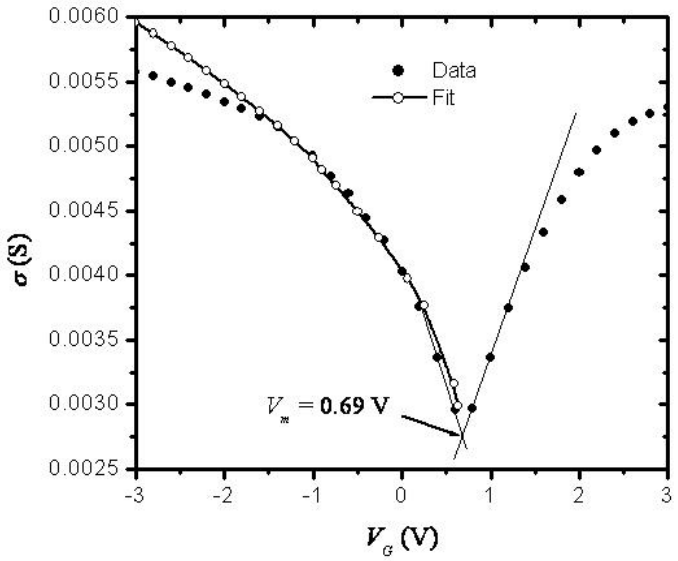

Fig. 2. Channel conductivity vs. gate bias of one C-face graphene FET on sample 20 (Fig. 1(b)). The minimum conductivity point is found by linearly extrapolating the curve near the minimum. The fit matches hole conduction data down close to V_m, revealing that the C-face graphene has a linear band structure.

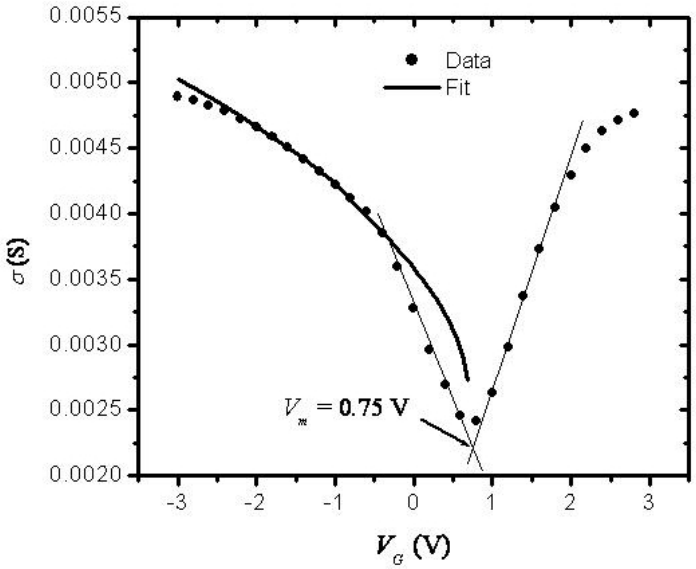

Fig. 3. The transfer characteristics of a Si-face graphene FET on sample 25. The minimum conductivity point is found by linearly extrapolating the curve near the minimum. In contrast to Fig. 2, the fit to hole conduction data is only good down to V_G = –0.6 V, suggesting a different band structure than the linear dispersion.

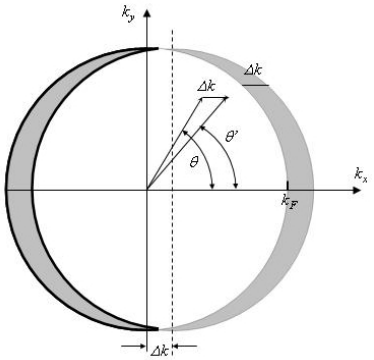

Fig. A1. The momentum is shifted by Δk by an applied electric field. When T = 0 K, only the carriers in the shaded areas have net contribution to the drift velocity.

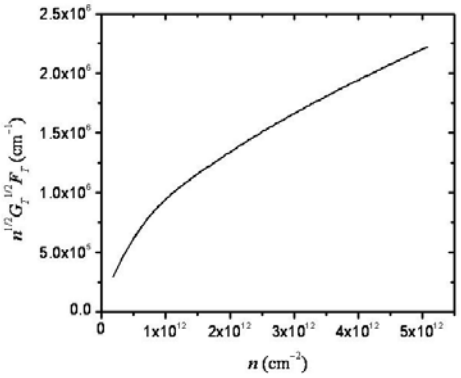

Fig. A2. $\sqrt{n} \cdot \sqrt{G_T} \cdot F_T$ versus carrier density n. Since the channel conductivity is proportional to $\sqrt{n} \cdot \sqrt{G_T} \cdot F_T$ and n is proportional to the gate overdrive voltage, this curve is a scaled version of the transfer curve of a FET based on graphene with linear energy band dispersion.

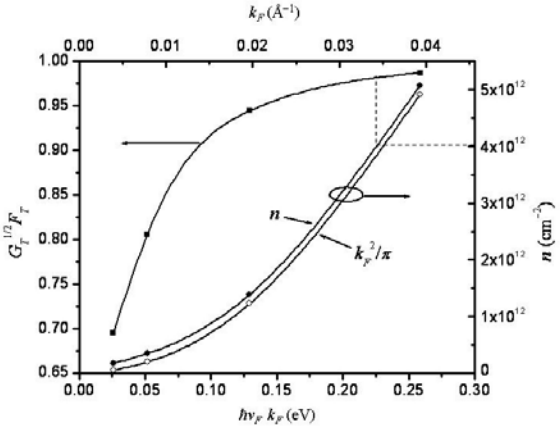

Fig. A3. Carrier density n at T = 300 K versus $\hbar v_F k_F$, as compared to k_F^2/π (right axis), and the temperature correction factor $\sqrt{G_T} \cdot F_T$ (left axis) versus $\hbar v_F k_F$. The top axis gives k_F for reference, assuming $v_F = 10^8$ cm/s. For $n = 4 \times 10^{12}$ cm^{-2}, $\sqrt{G_T} \cdot F_T = 0.98$ and the difference between n and k_F^2/π is negligible, therefore the effect of room temperature is negligible above $n = 4 \times 10^{12}$ cm^{-2}.