Use of Phase Transitions in Electronics

Moonkyung Kim[1*], Sang Hyeon Lee[1], Shriram Ramanathan[2], Byung-ki Cheong[3], Sandip Tiwari[1]
[1]Cornell University, New York, USA, 14853
[2]Harvard University, Massachusetts 02138, USA
[3]Korea Institute of Science and Technology, Korea

[*]Email: mkk23@cornell.edu

Ultra-high speed and reconfigurable electronic elements have a significant potential in circuits and applications which need to dynamically respond to changes. Materials where properties change at low energy with fast transition time provide a path to easy scalability provided CMOS process comparability can be maintained. We employ phase transitions induced by electric field and/or thermal energy at fast time scales in electronic device structures with CMOS compatible materials to show the potential of phase transitions for such a direction.

Three phase transition materials – $Ge_2Sb_2Te_5$ (GST), VO_2, and $SmNiO_3$ – have been employed to demonstrate different memory structures, all operating at low voltages. The phase transition employed in these demonstrations is structural and in crystalline phase. Conventionally, GST is employed as a current-driven and heat-triggered structural phase change via a transition being between amorphous and crystalline phases. It has two structural phase transitions: amorphous-to-FCC at ~150 ˚C and FCC-to-HCP at ~250 ˚C. In FCC phase, GST has a distorted rocksalt-like structure with a lattice parameter of 6.02 Å. The phase transition we employ is an unheated field-induced transition where Ge atoms shift from the ideal rocksalt positions in between two positions, a Ge-Te bond length of 2.83 Å and 3.15 Å [1]. These off-centered displacements result in a net dipole moment. A novel phase transition memory results where GST is akin to a floating gate layer but without the need of charge injection. Retention time of hundreds of second constrained by depolarization is observed and the extracted remnant polarization is ~0.13 $\mu C/cm^2$ (see Fig. 1).

In VO_2. a large permittivity and conductivity change occurs via both thermal and field-activated processes. This phenomenon has been adapted to many applications including in optics and sensors using its low transition temperature in the 60-70 ˚C range. During this transition, VO_2 becomes tetragonal above the temperature and is in a metallic state. Resistivity changes of up to 3-5 orders in the material have been observed [2]. In implemented single element memories, a hysteresis memory window of about 1 V is achieved with -4 and 4 V gate sweeps (Fig. 2). The remnant polarization and the coercive field of VO_2 are ~5.3 $\mu C/cm^2$ and 450 kV/cm. Similar hysteretic effects are observed in $SnNiO_3$, in this case because of oxygen vacancy induced polarization.

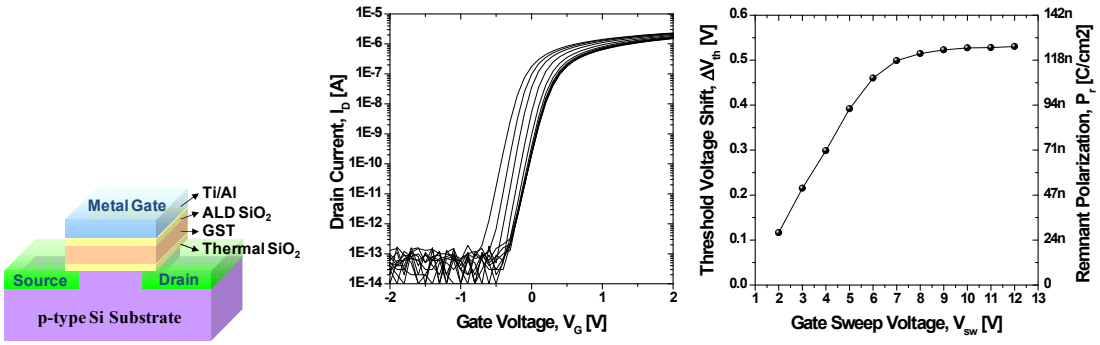
The effects are volatile due to depolarization. But, the properties are appropriate for single element DRAM-like embedded structures, including in new architectures.

ACKNOWLEDGMENT

This work was partially supported by NSF through Center for Nanoscale Systems, Focus Center Research Program, and NYSTAR.

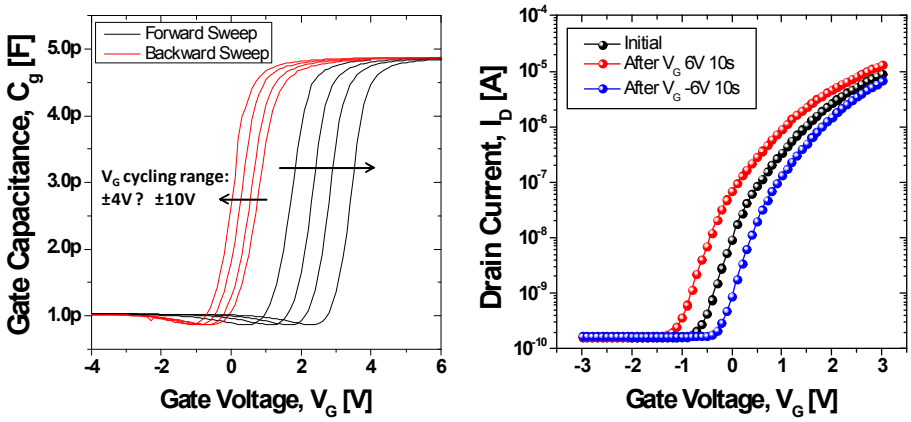
[1] T. Uruga et al., Nature Materials, vol. 3, pp. 703–708 (2004)

[2] S. Ramanathan et al., APPLIED PHYSICS LETTERS 91, 062104 (2007)



(a) (b)

Figure 1. (a) Schematic of a single element memory device with a GST floating gate and (b) its transfer curve and V_{th} saturation characteristics.



(a) (b)

Figure 2. (a) Hysteresis behavior of gate capacitance in response to gate voltage and (b) gate field dependency of threshold voltage