Introducing the Research Centers for Solar Energy Harvesting

1. *Research Center for Next-generation Thin Film Solarcells, funded by MKE, Korea*
2. *Pioneer Research Center (PRC) for Solar Thermal Conversion Nanodevices, funded by MEST, Korea*

Jung-Ho Lee, Professor and Director

Hanyang University

차세대박막태양전지
원천기술연구센터

Research Center for Next-generation Thin Film Solarcells

- *Towards the next-generation thin film solarcell using silicon wires*

Jung-Ho Lee (PI), Bongyoung Yoo, Jong-Ryoul Kim, Yong-Ho Choa, Yongwoo Cho
Hanyang University

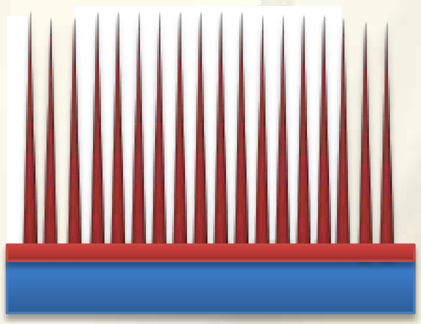
Collaborated with
Yonsei University, KIMM, NNFC, Korea Institute for Energy Research, Sungkyunkwan University, Ewha Women's University

Hanyang University
SEMICONDUCTOR NANO-PROCESSING LAB.

Motivation

Combining the AR enhancement of dense NWs and the radial p-n junctions of sparse MWs.

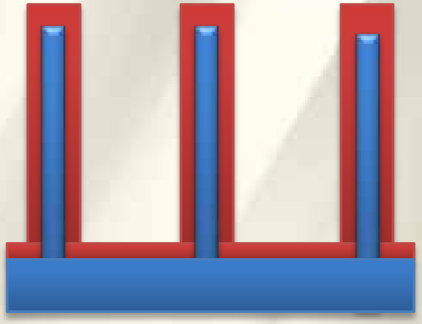
Tapered SiNWs



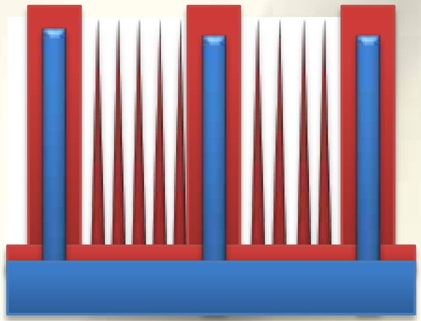
Antireflection (AR) role
è Enhancement of optical absorption

High efficiency solar cell

SiMWs



Radial p-n junction of MWs
è utilization of low-purity silicon enabling short diffusion of carriers



Very dense tapered NWs co-integrated with periodic MW arrays

Radial p-n junction wired solarcell

<Vertically aligned nanowires>

1. Strong broadband optical absorption

à Light trapping enhancement in between nanowires (NWs)

2. More light absorption due to Graded-refractive-index (GRI) effect using tapered NWs

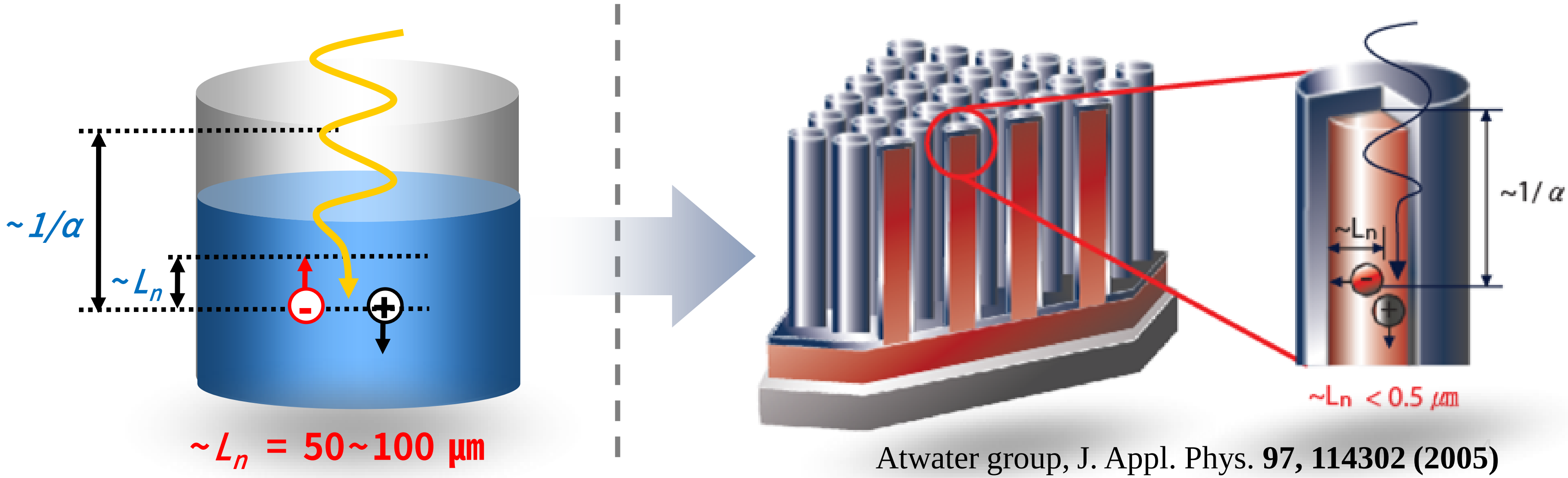
< Radial p-n junction microwires>

3. Long absorption paths & short distances for carrier collection

à Orthogonal separation of carriers to a sunlight direction

4. Large surface areas for light harvest

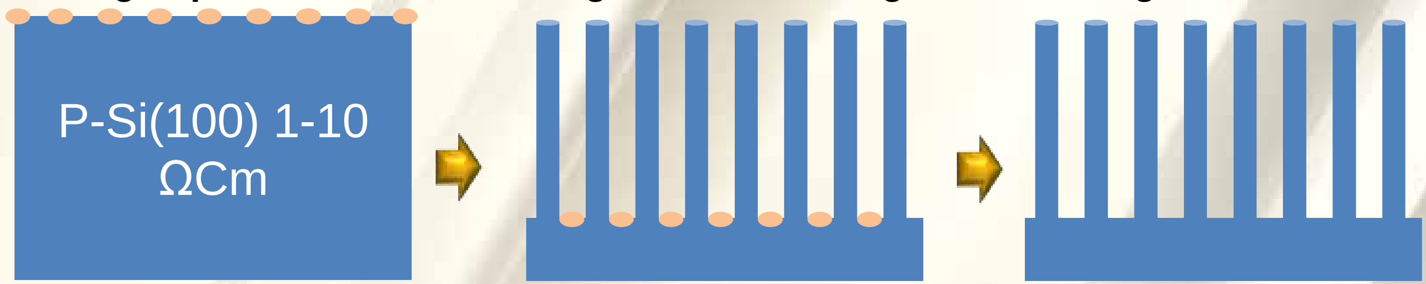
Planar *p-n* junction solarcell | **Radial *p-n* junction solarcell**



Atwater group, J. Appl. Phys. **97, 114302 (2005)**

Very dense, vertical SiNWs prepared by Ag induced etching

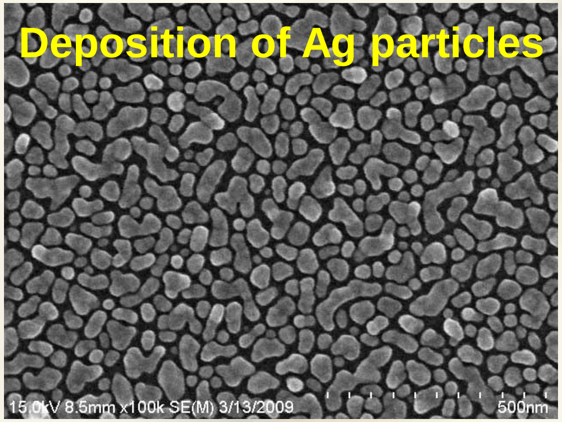
Ag deposition | **Ag induced etching** | **Ag removal**

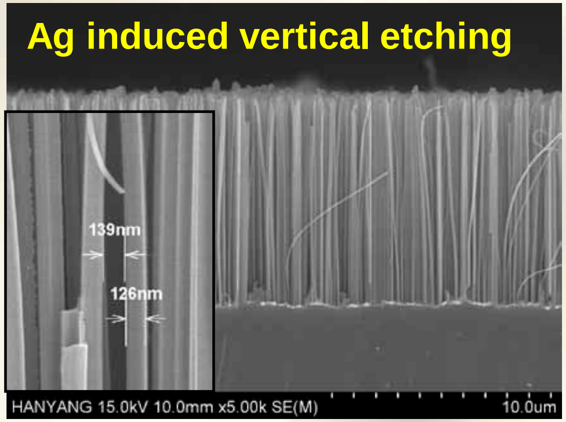


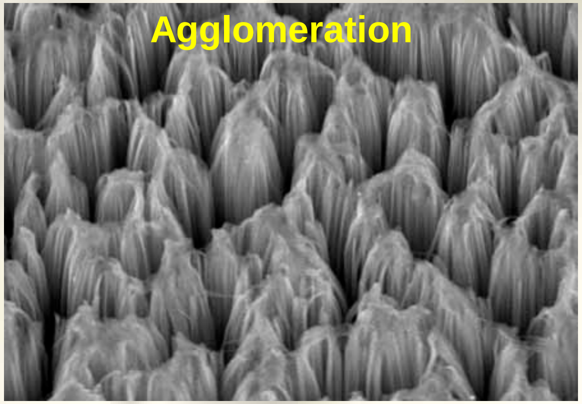
AgNO3 (0.01M) + HF(4.6M)

HF(4.6M) + H_2O_2 (0.44M)
20min (0.5 um/min)

Ag removal – nitric acid





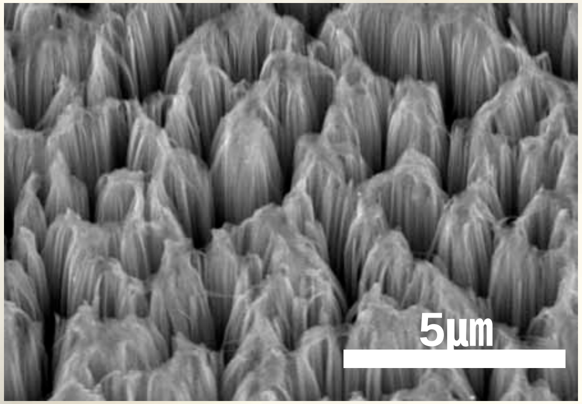


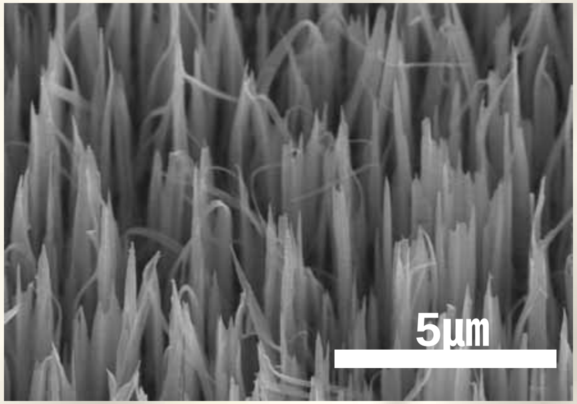
- Simple, Cost-effective, Room temperature approach
- Waferscale fabrication of vertical SiNWs with a 20-200 nm diameter range
- Highly uniform feature across the wafer
- Easy agglomeration at the tops of NWs upon drying

Sharp tip, tapered SiNWs

Top-sides of SiNWs agglomerate to form a bundle

Tapered SiNWs

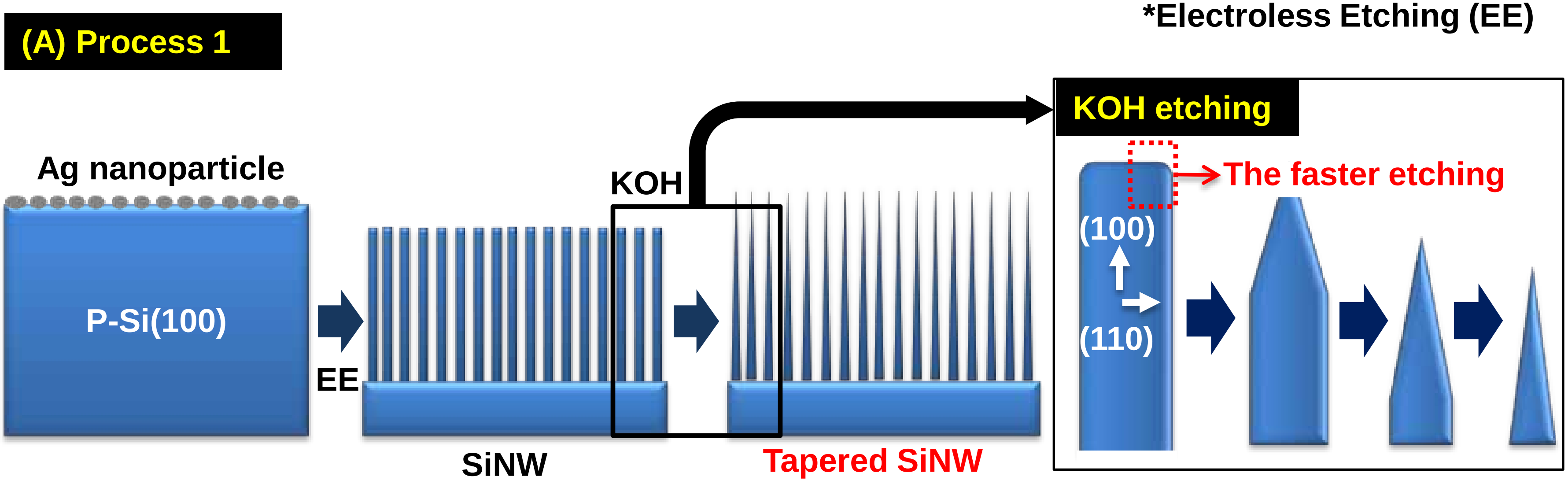


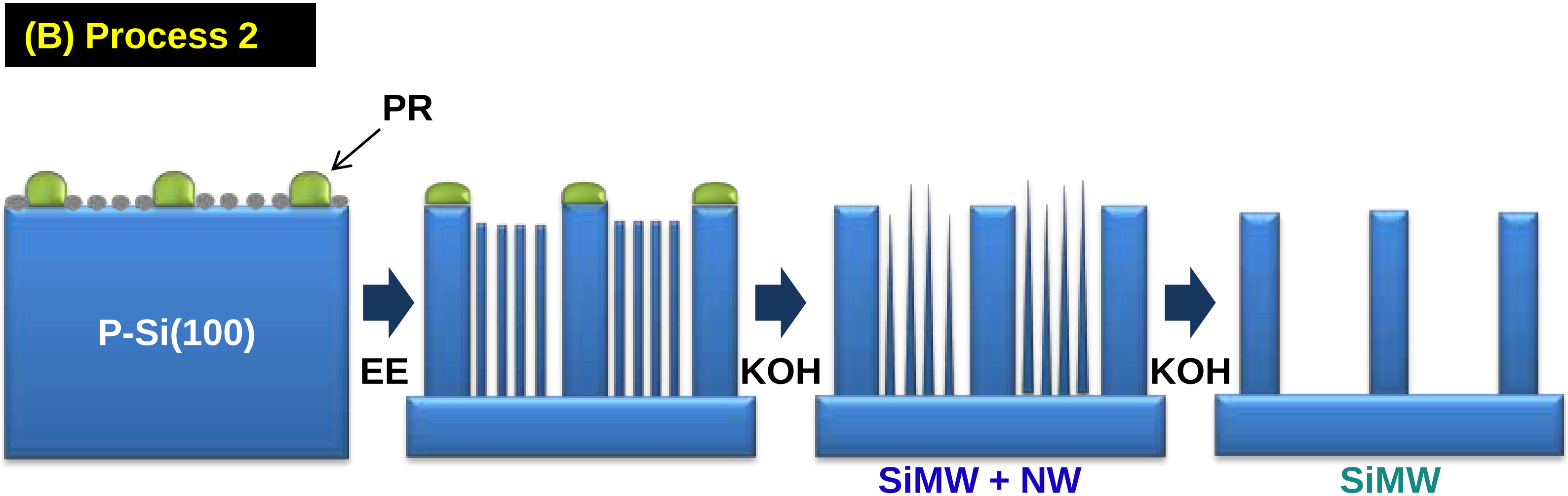


•**Effect of KOH etching:** **SiNW arrays agglomerated by a van der waals force could be easily separated while making their tops very sharp**

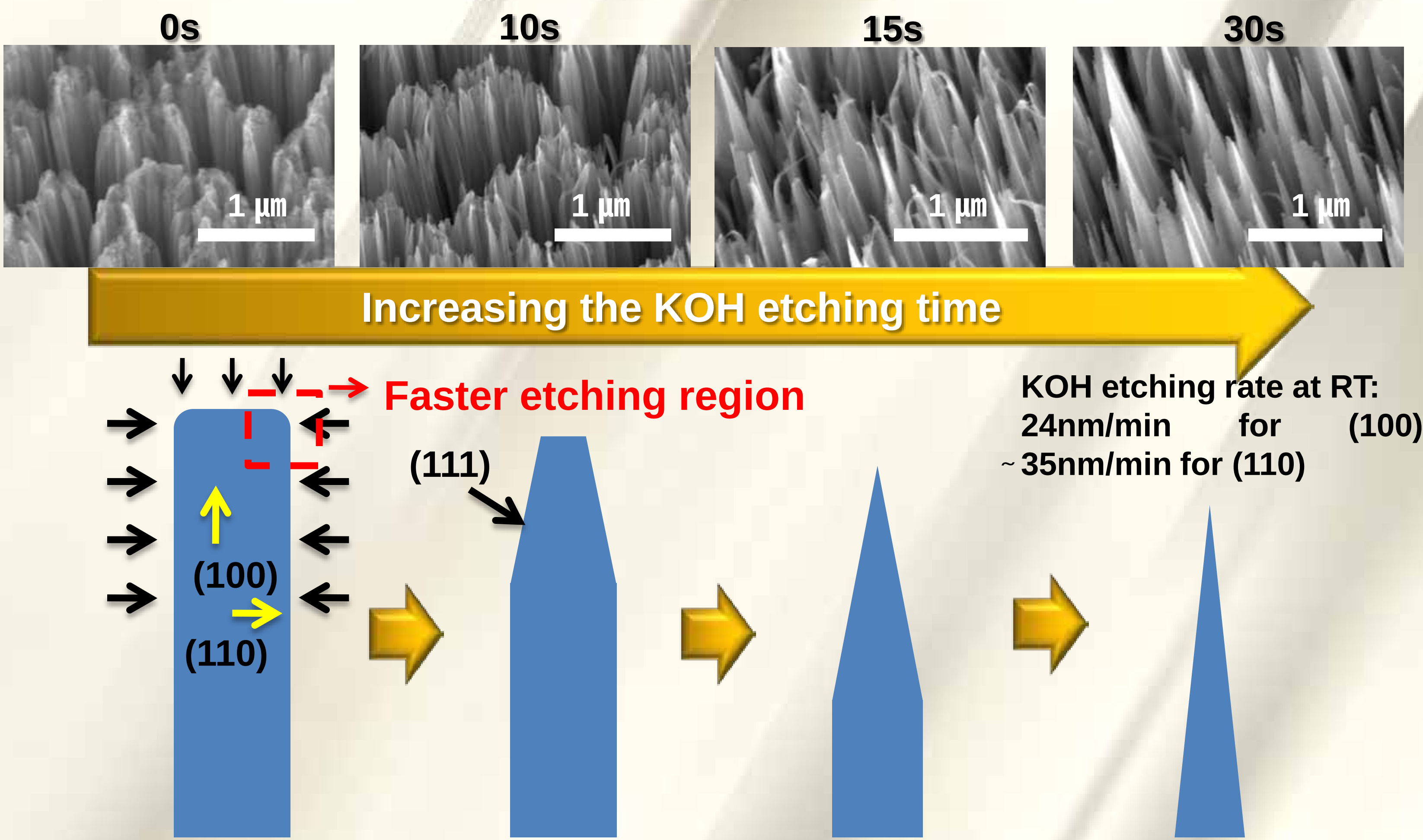
Fabrication of tapered SiNW, SiMW+SiNW, and SiMW

*Electroless Etching (EE)



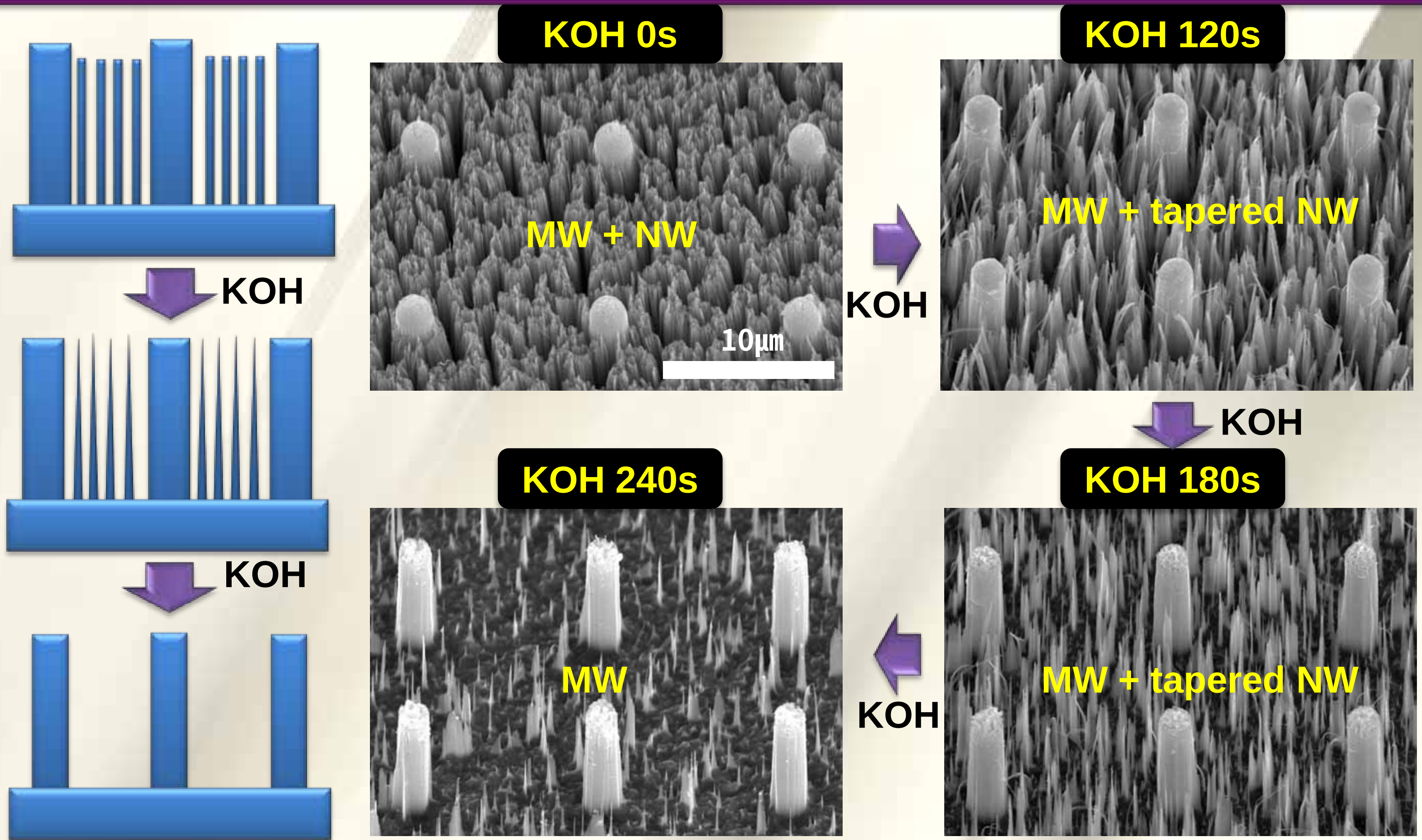


Morphological variation of tapered SiNWs with KOH etching time



- Initially, the corner sides of NWs strongly attacked by KOH because the complicated high-index surfaces develop easily.
- Finally, sharp-tip, tapered SiNW arrays with (111) side planes remains because the etching rate of those planes is slowest.

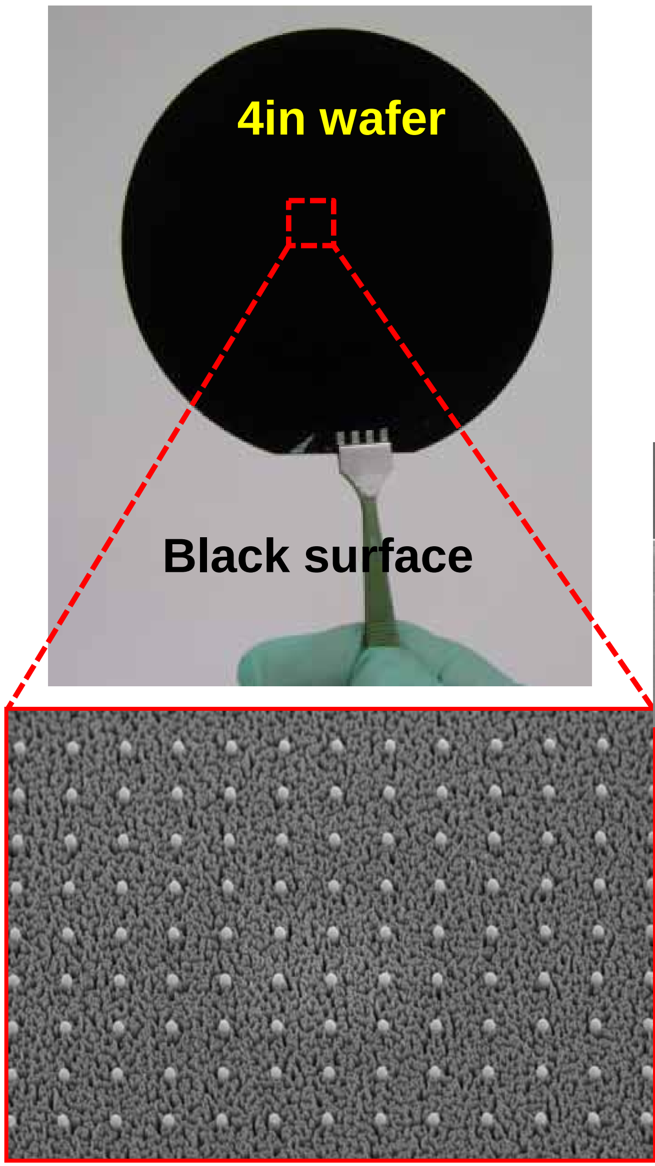
Co-integrated wire structure of SiNW+SiMW

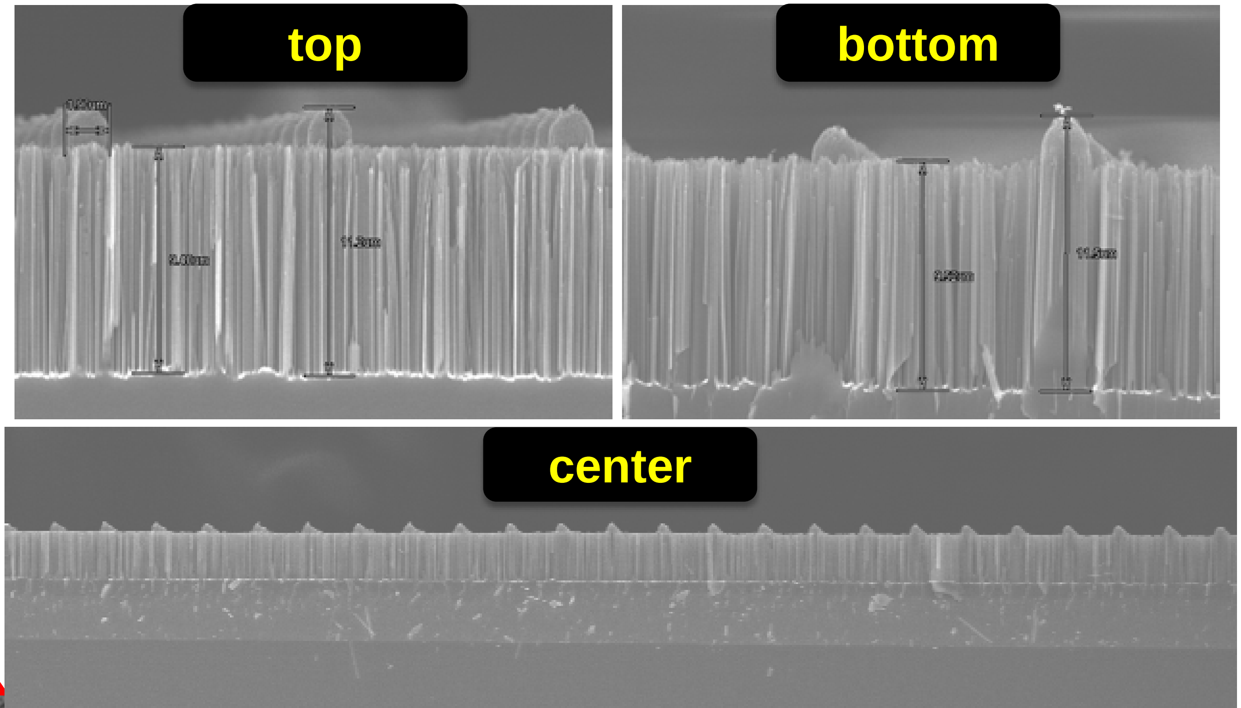


KOH etching could reduce the areal density of NWs while improving the surface roughness of NW.
Diameter of MWs normally decreases from ~2 μm to 1.75 μm while KOH etching for 240 s.

Waferscale uniformity of the co-integrated wire structure

Waferscale fabrication of SiNWs+MWs

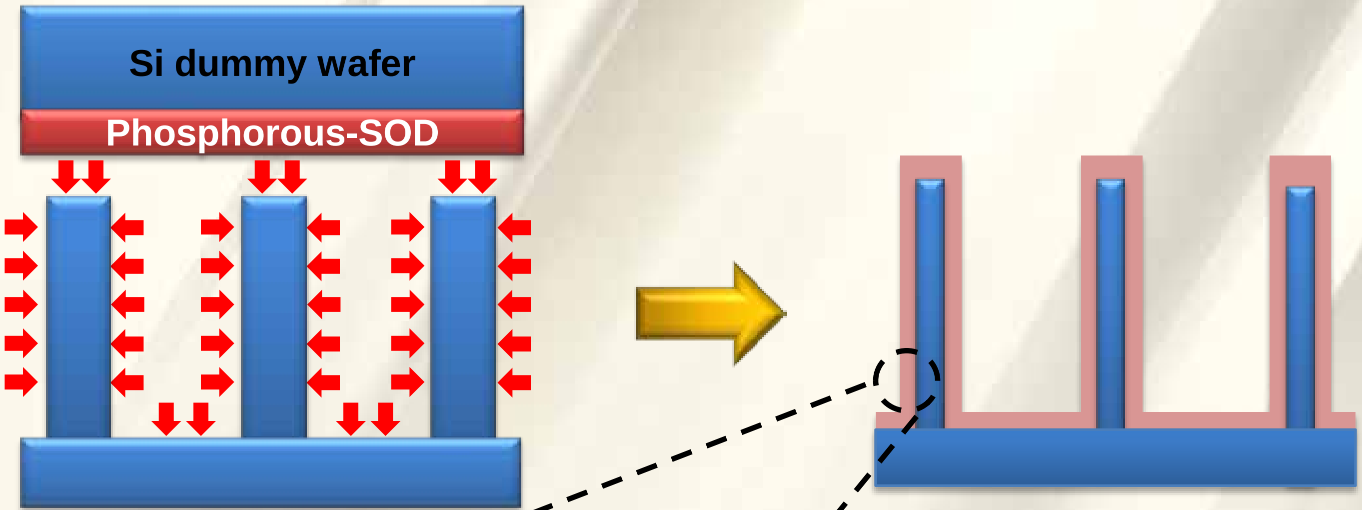


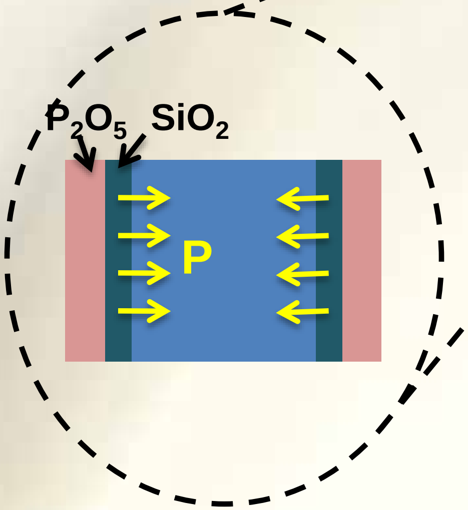


Waferscale co-integrated SiNW+MW arrays show the black color due to excellent absorption.

Doping method: Spin-on-doping (SOD)

Fabrication of p-n junction



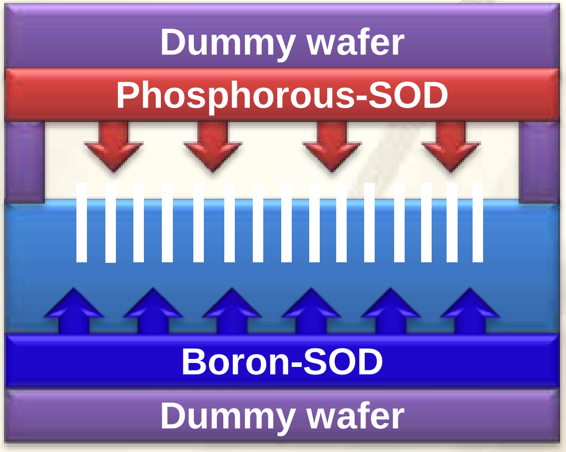


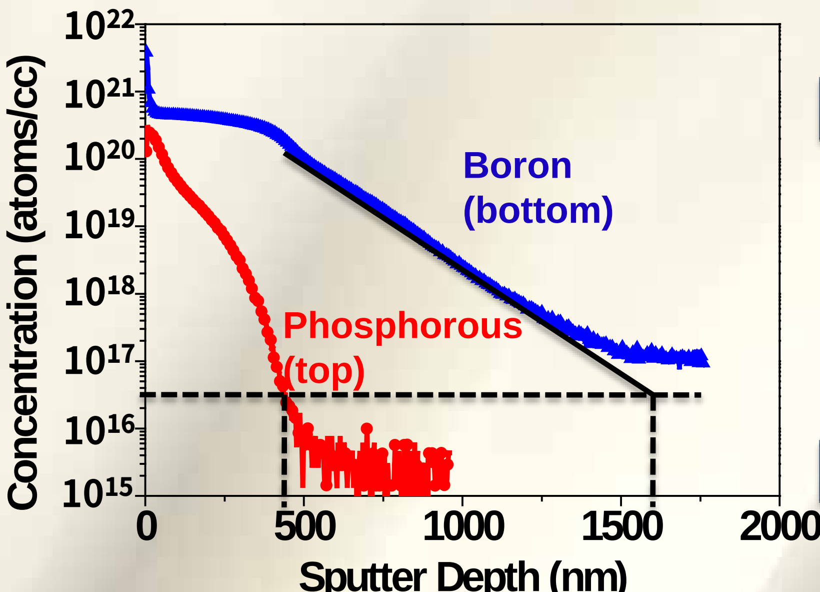
<Doping mechanism of pSOD>

$2P_2O_5 + 5Si$ à $5SiO_2 + 4P$

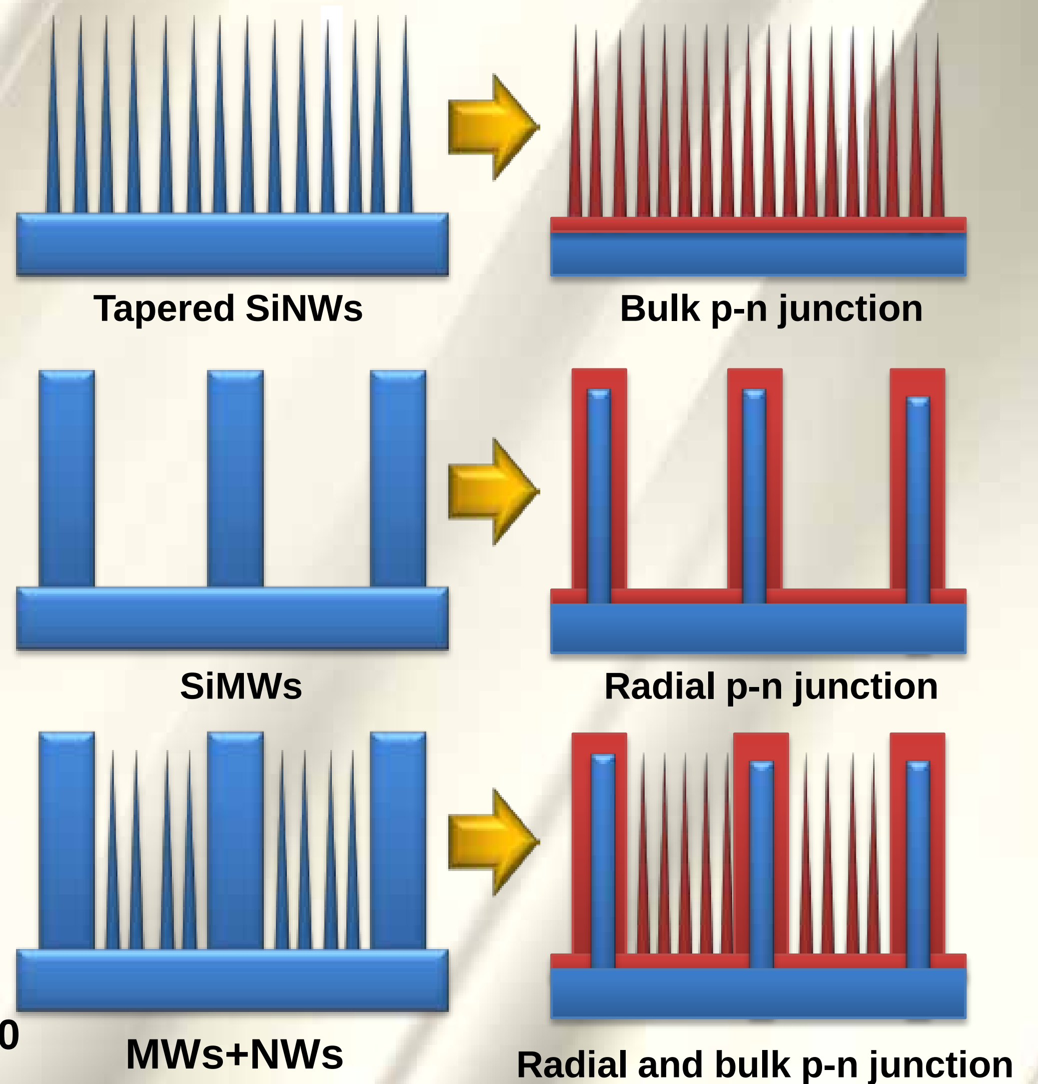
Solid-state diffusion:
Predeposition followed by drive-in

Bulk or radial p-n junction forms depending upon wire diameters

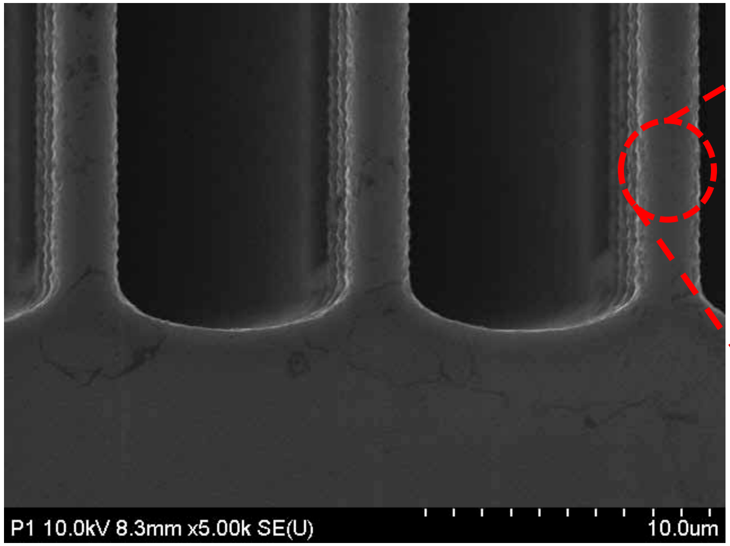




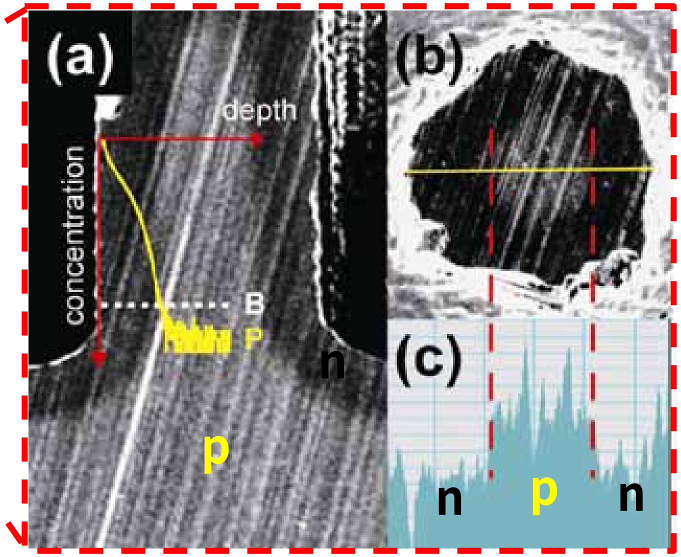
Fabrication of p-n junction using SOD



Low-voltage SEM images of a radial p-n junction MW

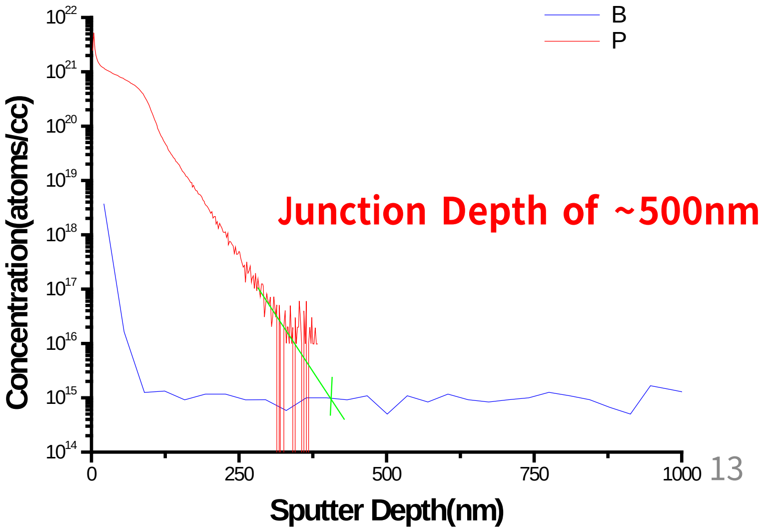


< Accelerating voltage of **10 keV** >

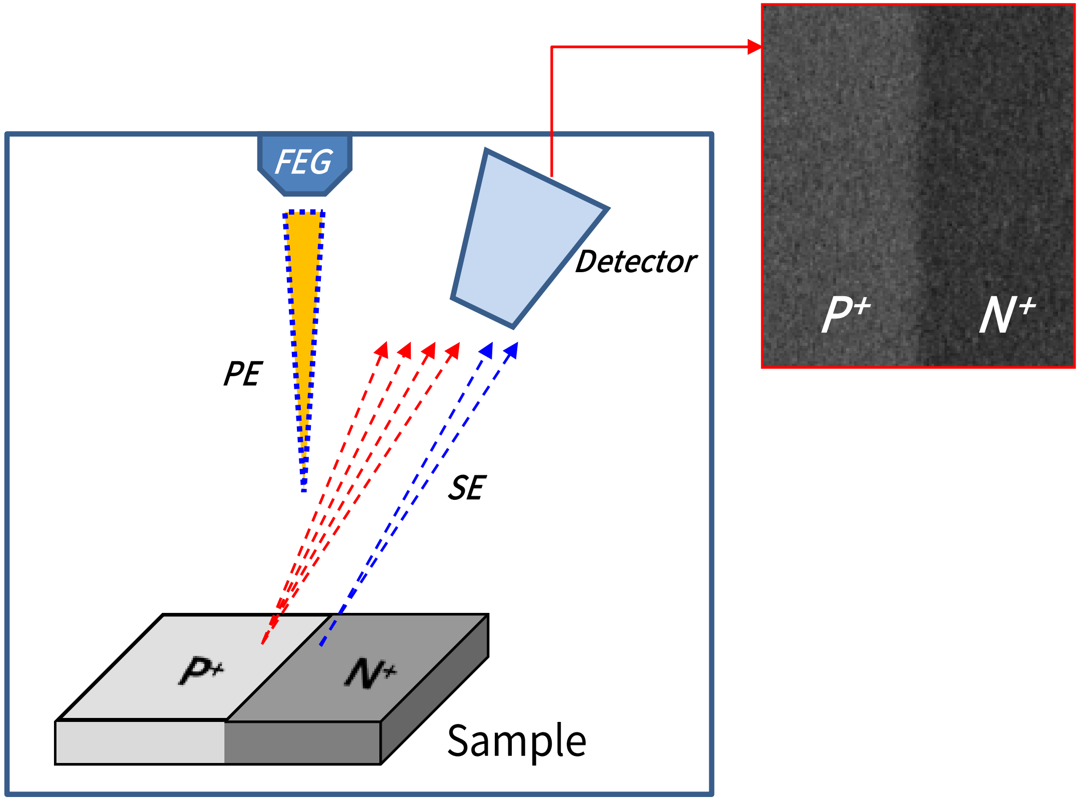


< Accelerating voltage of **1 keV** >

- **LVSEM images clarify the formation of a radial p(core)-n(shell) junction inside the Si wire.**
- **The vanishing contrast at high accelerating voltage is due to the dominance of the energetic backscattered electrons (BSE) and their respectively generated SEs.**

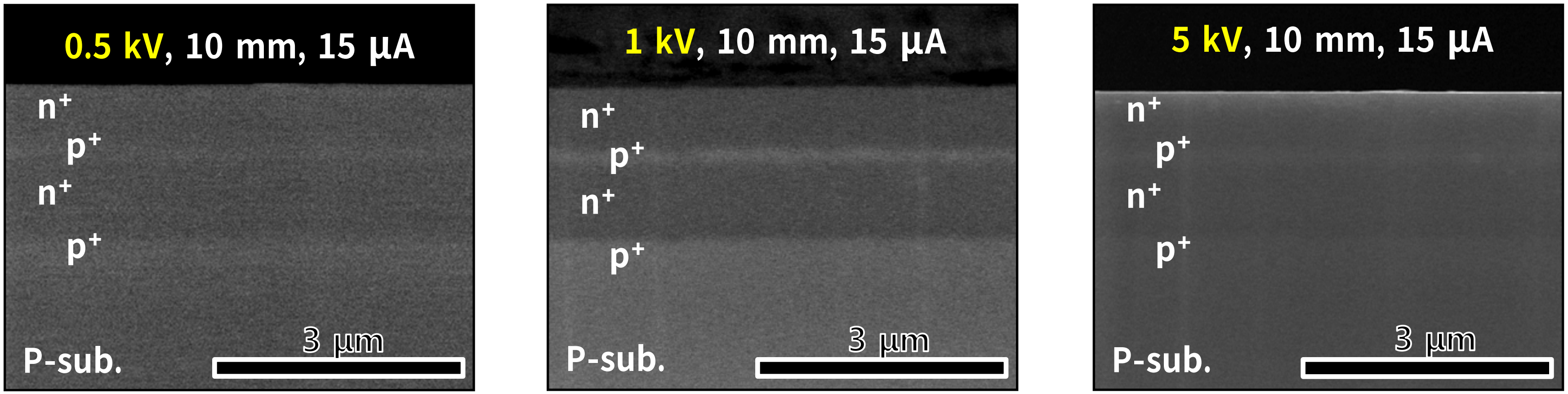


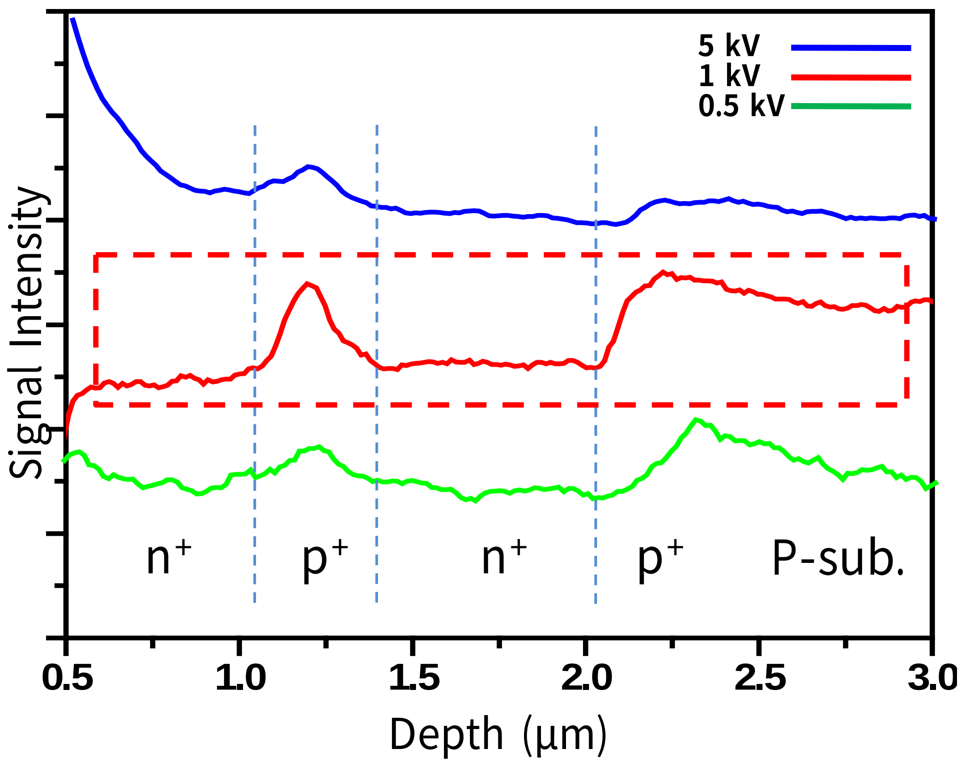
Dopant contrast in LV-SEM



- Dopant profiling using SEM is based on the fact that the amount of emitted SEs from the *p*-type region is greater than that of *n*-type one.
- *p*-type region appears brighter than *n*-type.
- Built-in potential difference in btw doped regions has been suggested for explaining this feature.

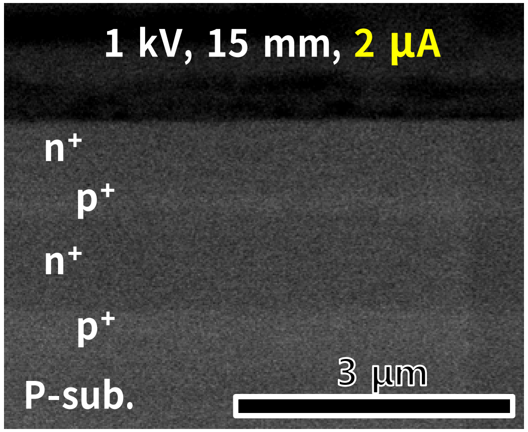
Accelerating voltage effect on dopant contrast

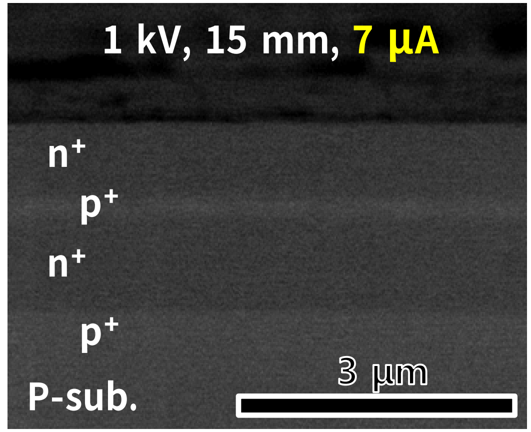


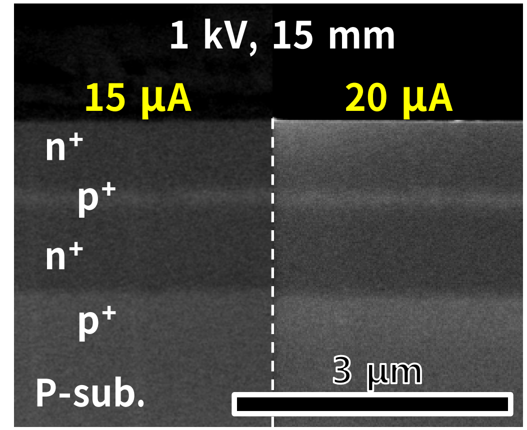


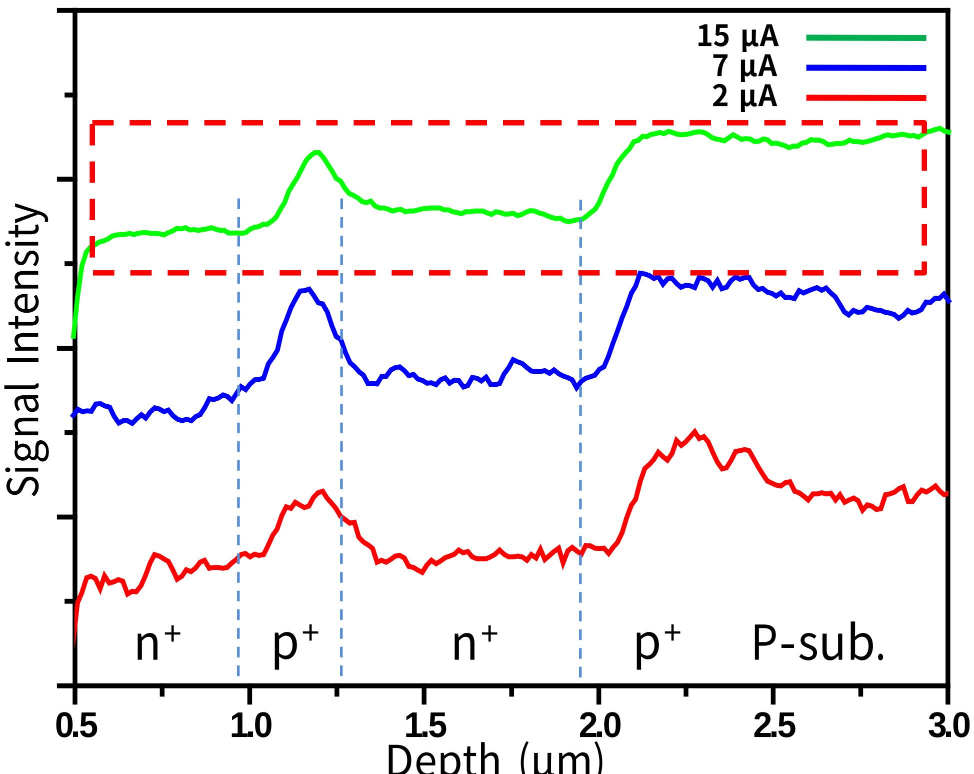
- Accelerating Voltage ↑, dopant contrast ↓
- Contrast can be obtained between 0.5-5 kV

Electron beam current effect on dopant contrast



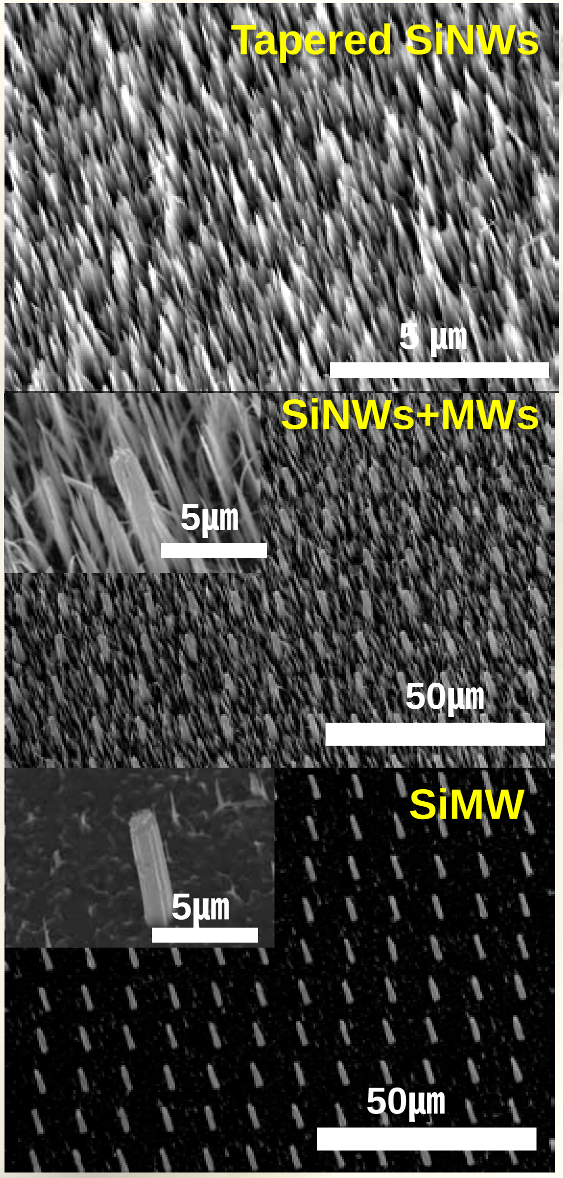


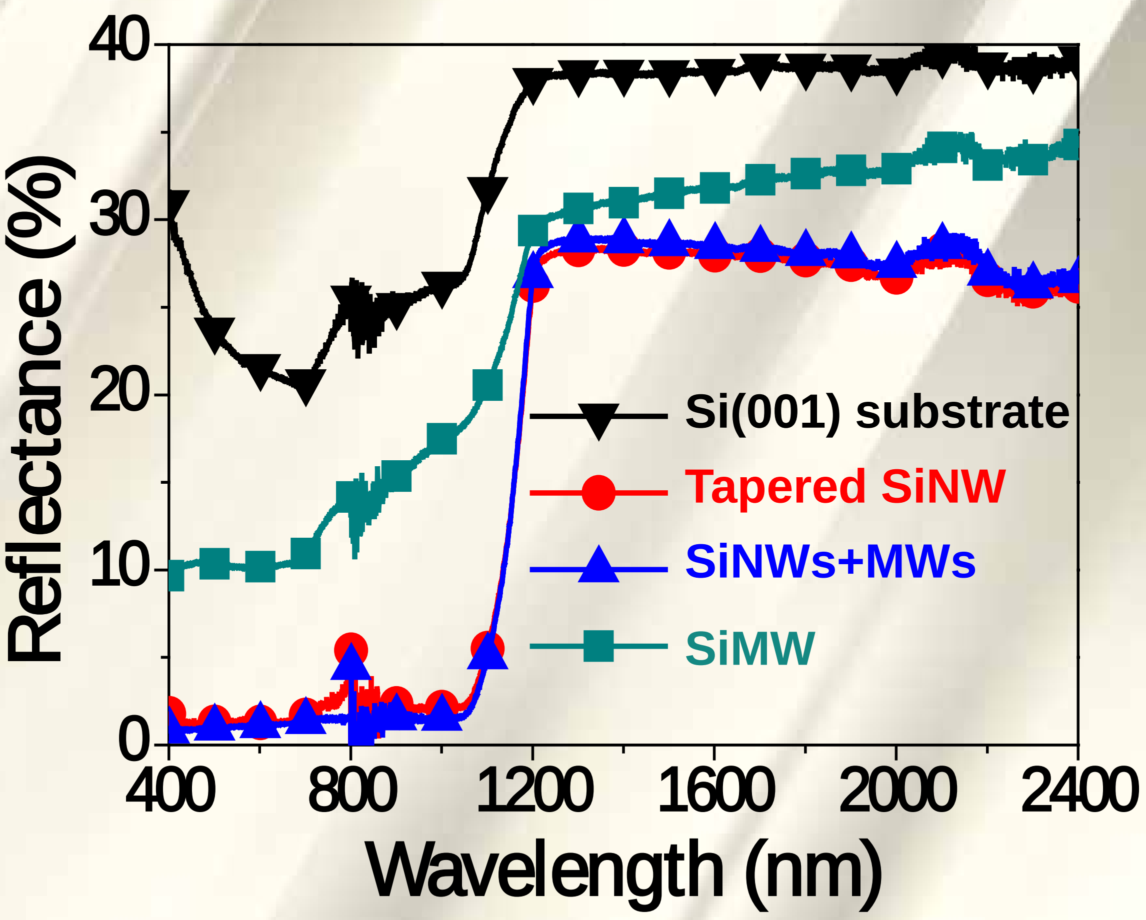




- Electron beam current ↑, dopant contrast ↑
- Contrast can be obtained between 0.5-20 **μ**A

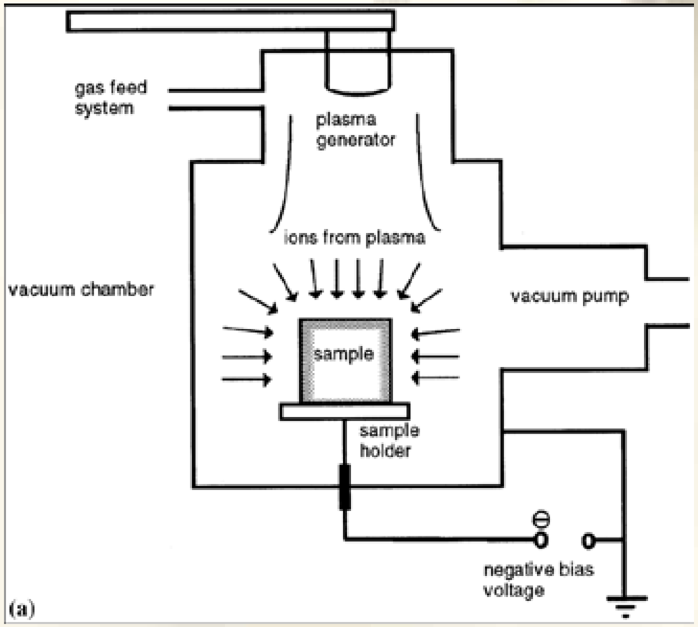
Optical property of various wire morphologies



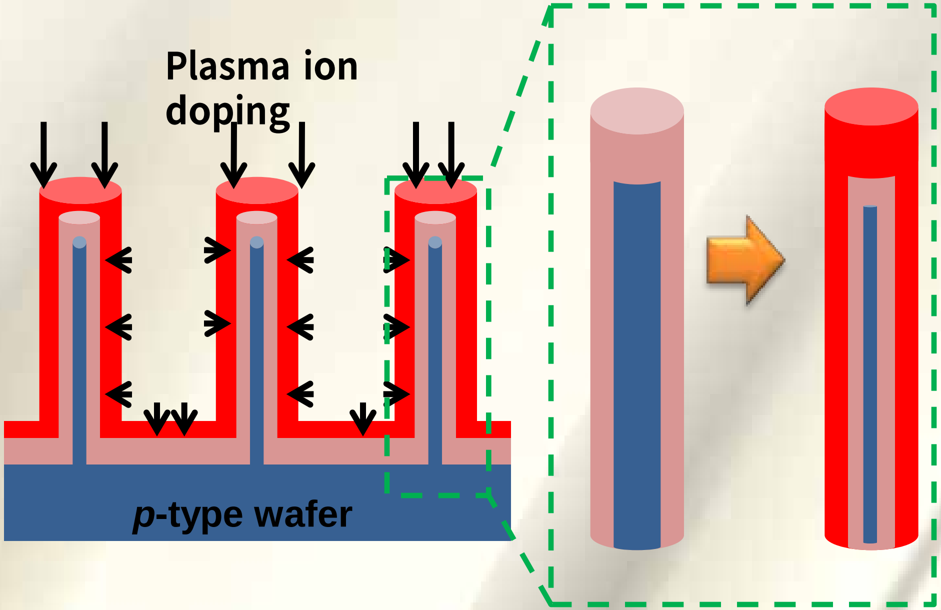


•The optical absorption of SiNWs+MWs structure is almost same as that of tapered SiNWs.

Additional Doping: Plasma Ion Doping (PID)

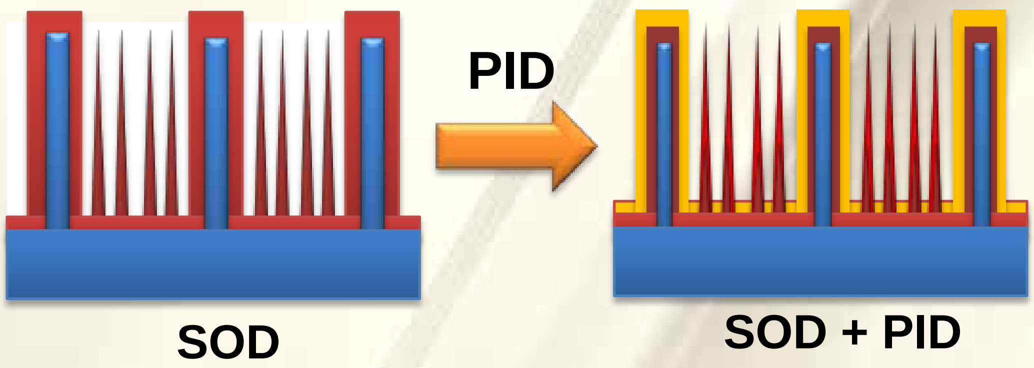


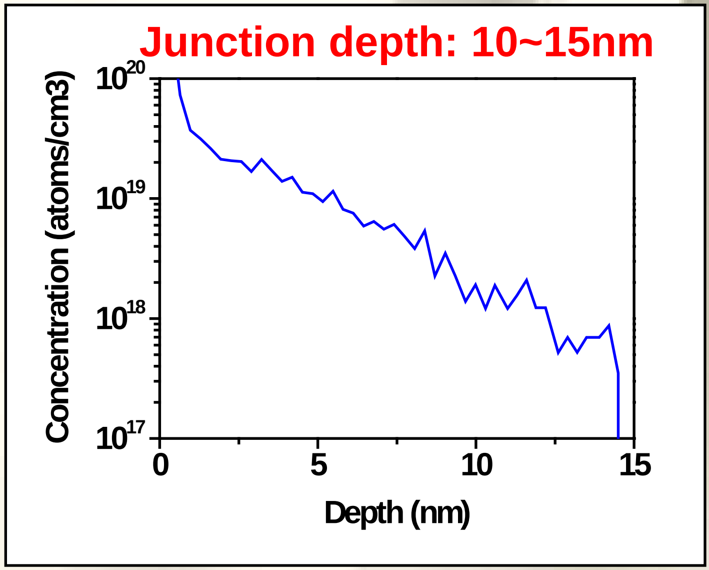
DC bias	Pulsed 1kV
Dopant	PH_3 30 sccm
RF power	1kHz
Time	60s
Annealing	900°C 30sec
Dose	3e15

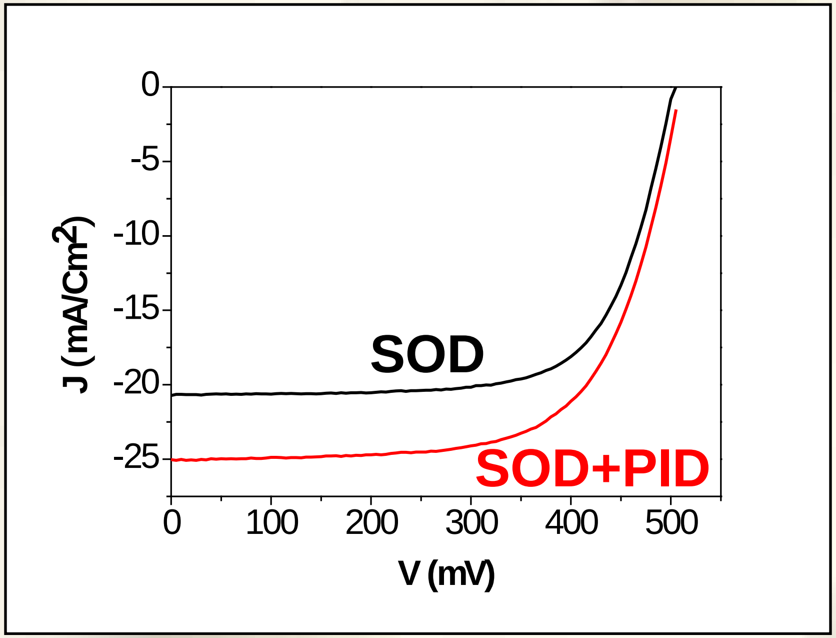


- Intensifying the N+-level of the MW shells while enabling **shallow, conformal doping**

Effect of plasma ion doping with SOD



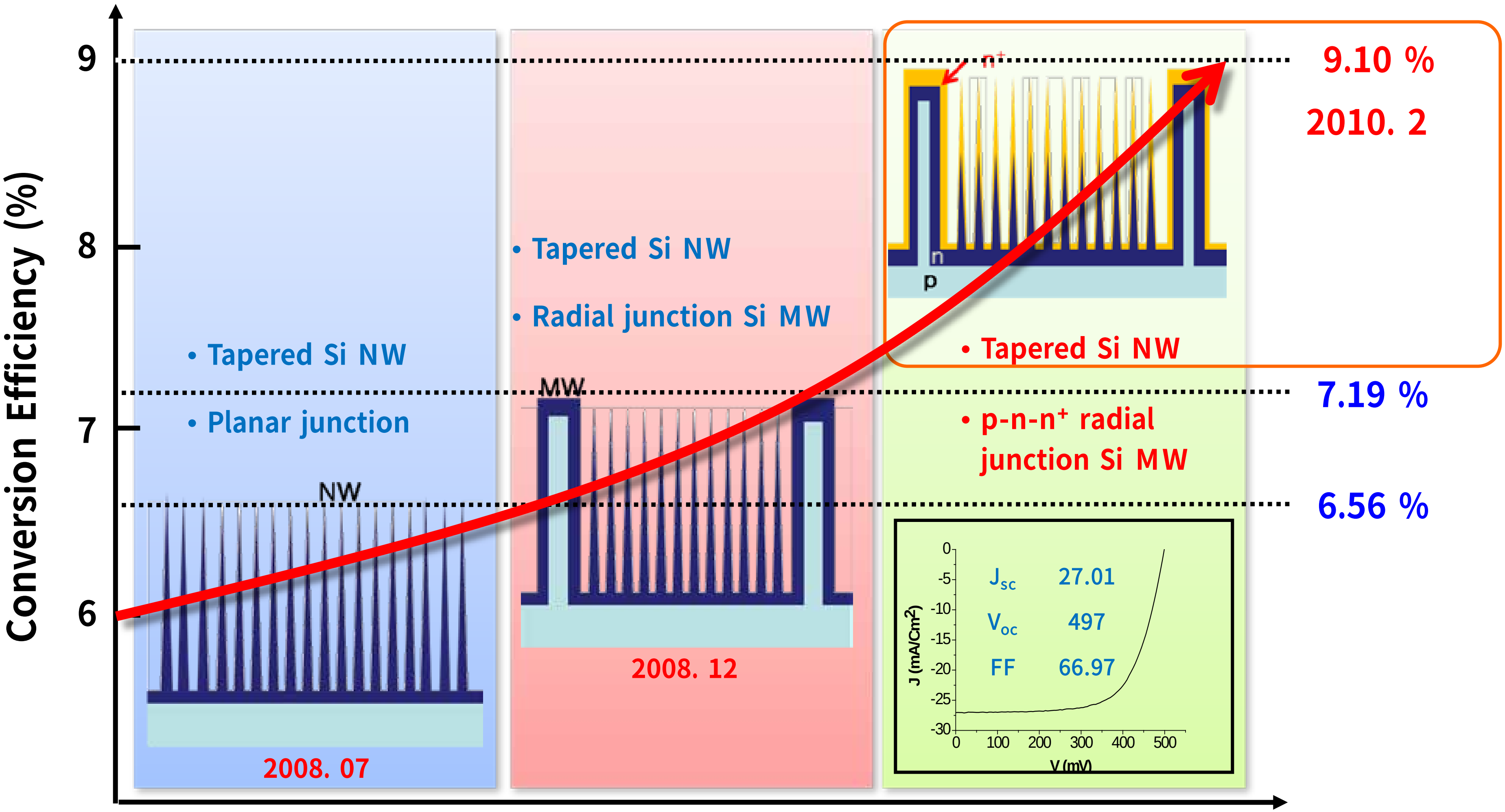




AM 1.5 (1000W/m²)	SOD	SOD + PID
J_{sc} (mA)	20.59	24.89
V_{oc} (mV)	500	509
FF	69.78	66.75
CE (%)	7.19	8.45

- **Additional PID further increases the conversion efficiency by enhancing the n+ doping level of MW shells.**

PV cell efficiency



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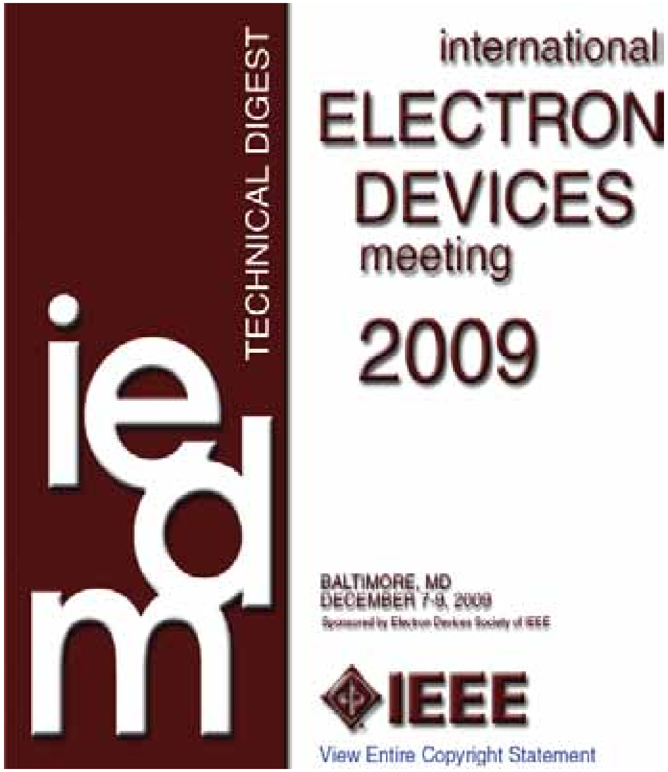

A novel photovoltaic nanodevice based on the co-integration of silicon micro and nanowires prepared by electroless etching with conformal plasma doping

Han-Don Um[1], Jin-Young Jung[1,2], Xiaopeng Li[1], Sang-Won Jee[1], Kwang-Tae Park[1], Hong-Seok Seo[1], Syed Abdul Moiz[1], Sang-Wook Lee[2], Jong-Yeoul Ji[2], Chung Tae Kim[2], Moon Seop Hyun[3], Yun Chang Park[3], Jun Mo Yang[3], and Jung-Ho Lee[1*]

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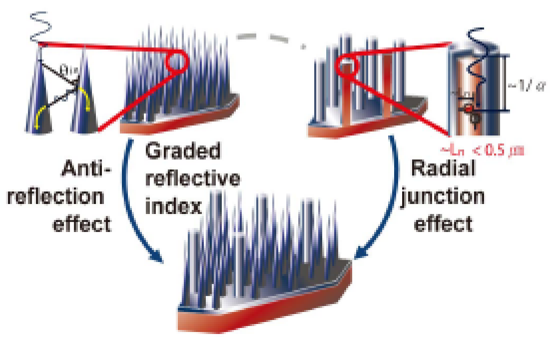


Fig. 1 Conceptual schematic of a novel PV nanodevice based on the co-integration of tapered Si NWs and MWs.

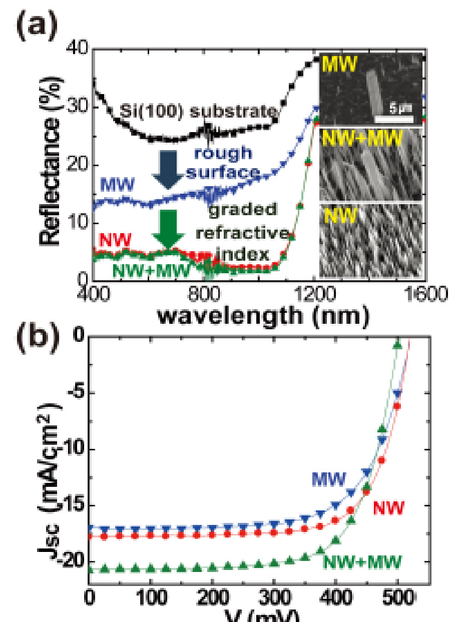
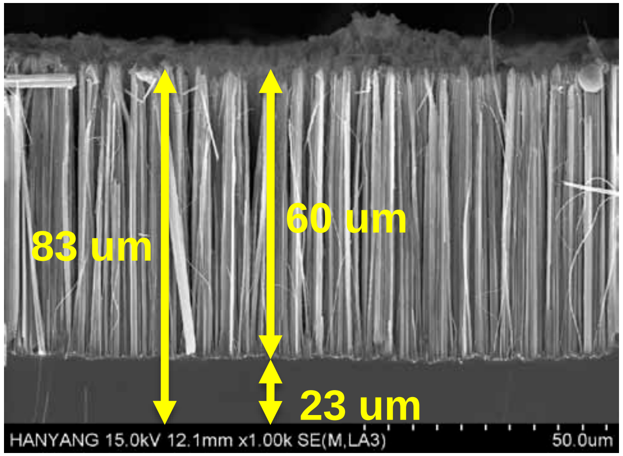
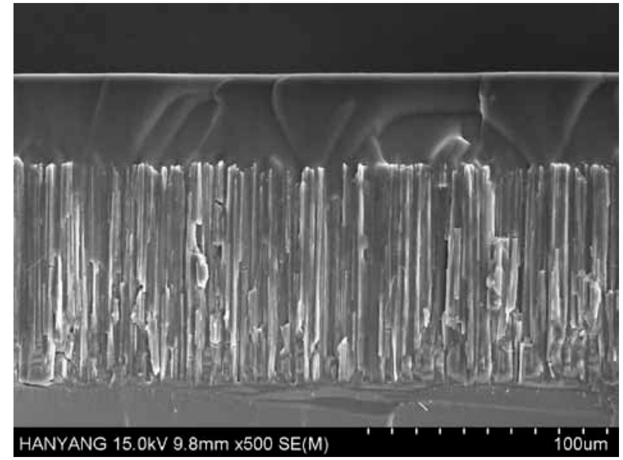


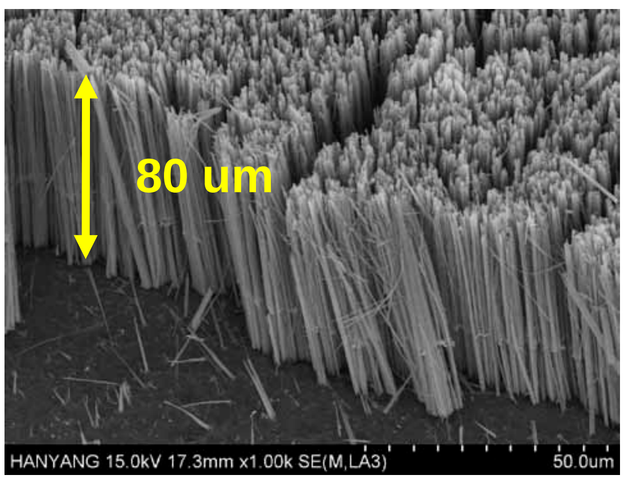
Fig. 8 (a) Optical reflectance data of a polished Si(100) substrate, a sole array of MWs, a sole array of tapered NWs, and a co-integrated structure of MWs and tapered NWs. (b) Their I-V characteristics.

PDMS embedded SiNW array for flexible solar cell

현재 12 X 12 cm²에서 박막화 공정 가능

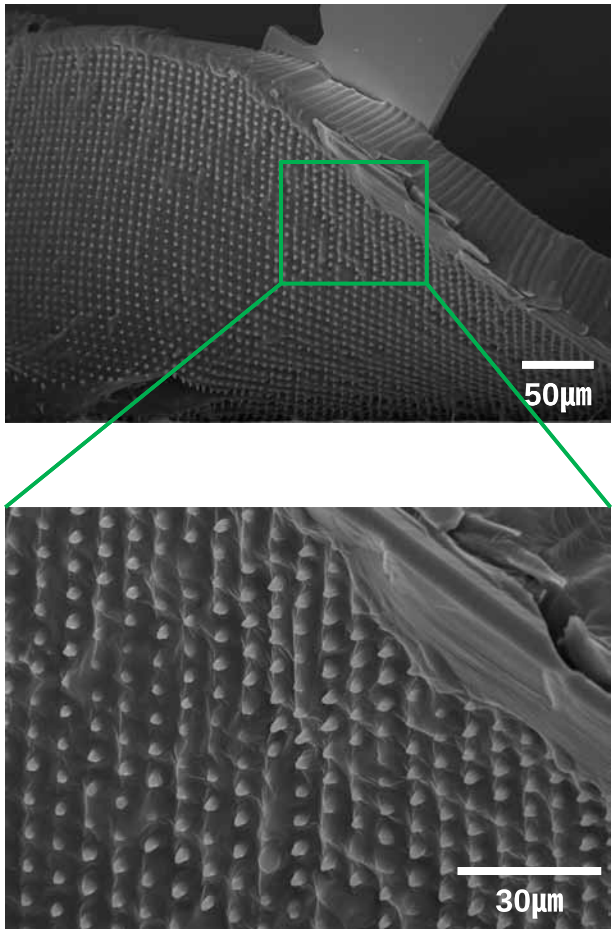




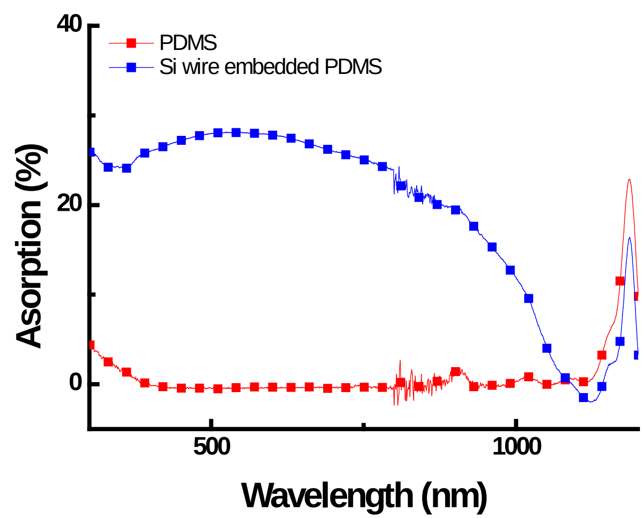


Flexible microwired solar cell

Detachment of PDMS embedded wire array



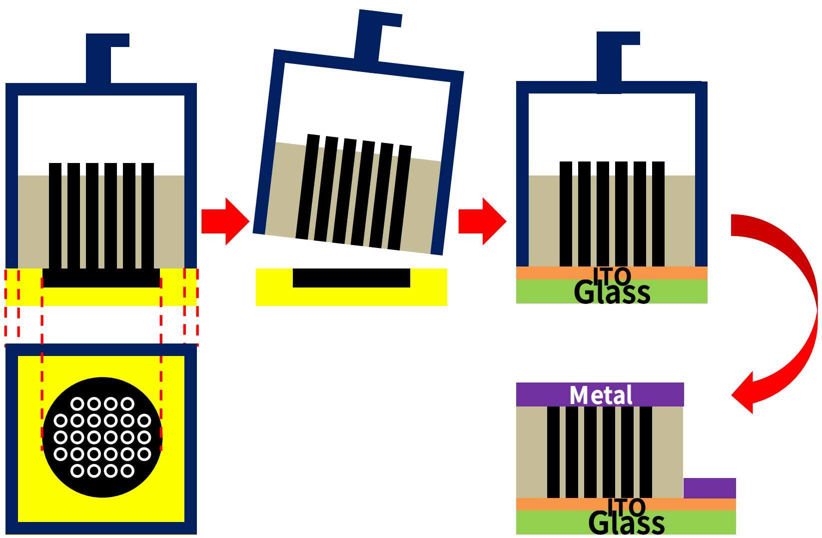
Flexible solar cell application



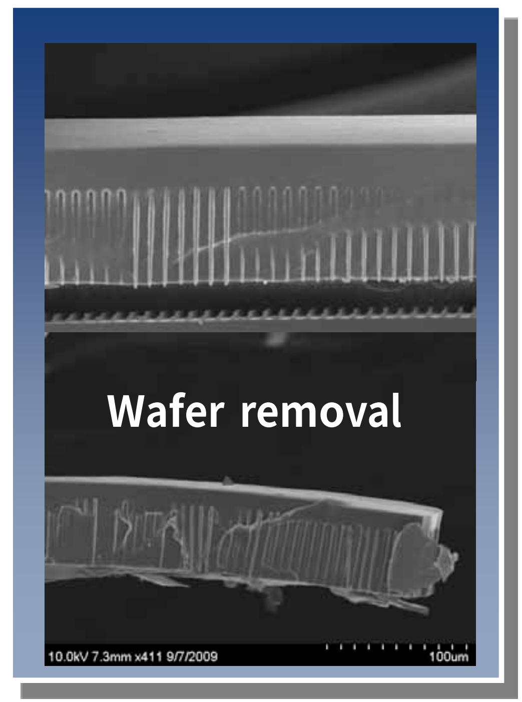
용이한 대면적 박막 구현 및 뛰어난 원가 경쟁력 확보

- Square mold를 활용할 경우, PDMS curing후 대면적 (³ 10X10 cm^2)에서 저비용으로 우수한 박막 탈착이 가능.
- UMG(4N~6N) thin wafer (20~50 ㎜)를 활용한 우수한 원가 경쟁력

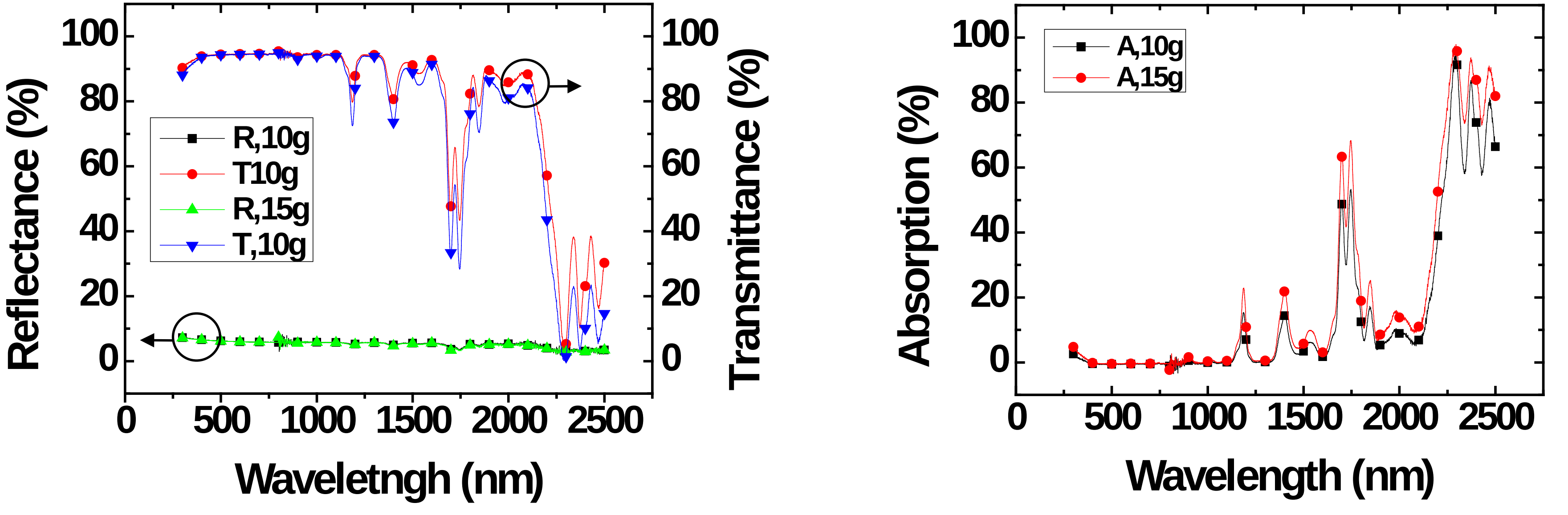
< 대면적 박막 구현>



< UMG thin wafer활용>

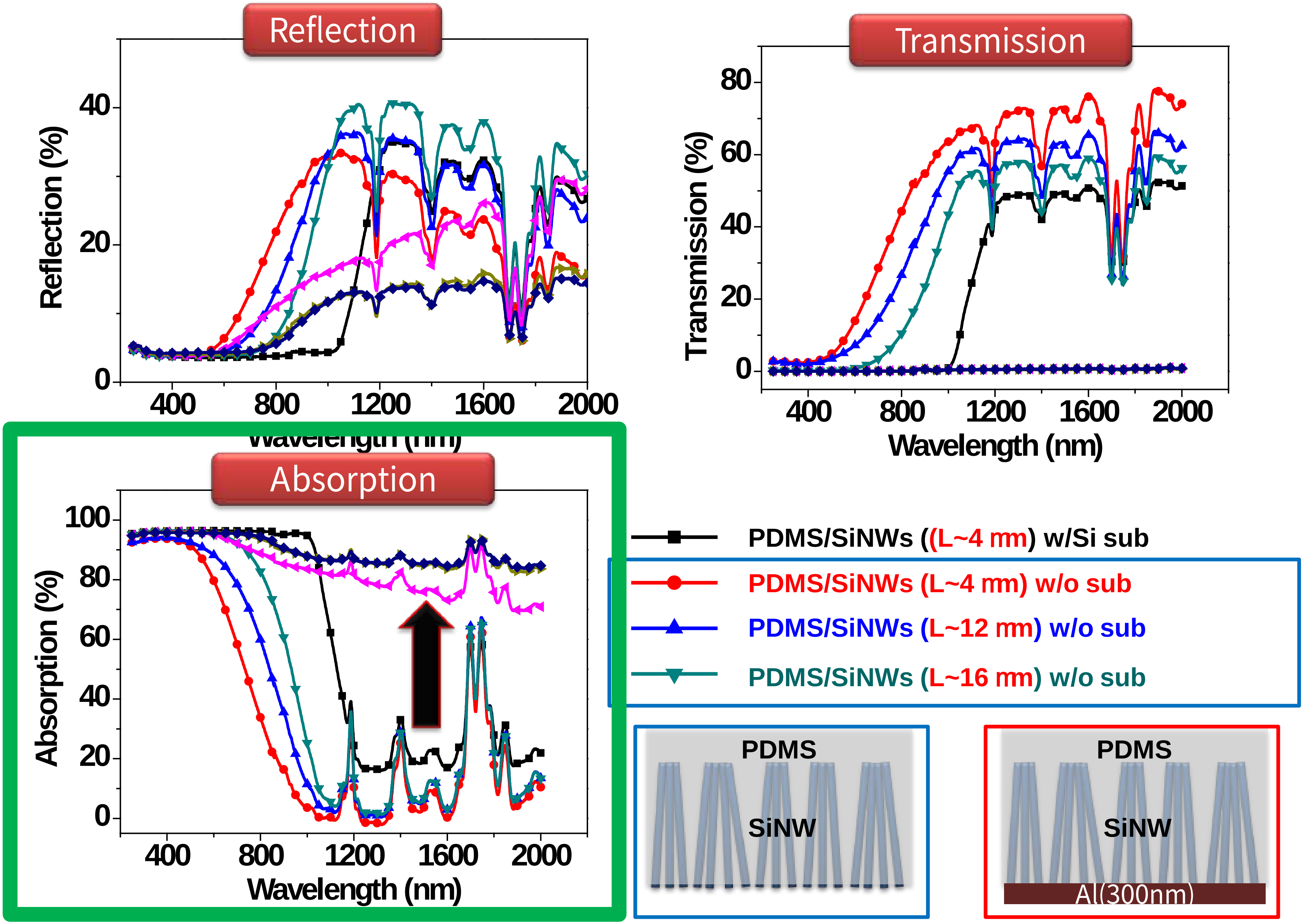


• Optical properties of pure PDMS

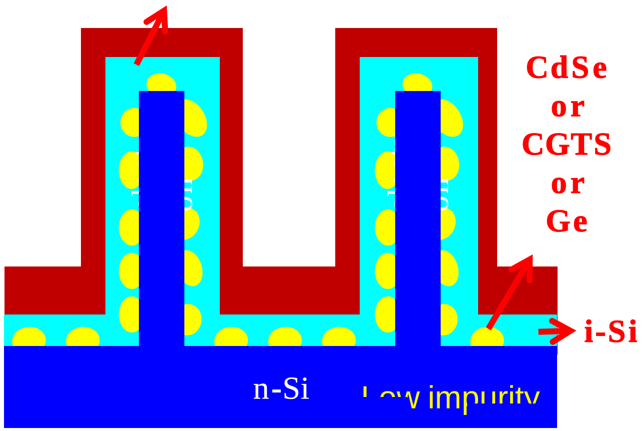


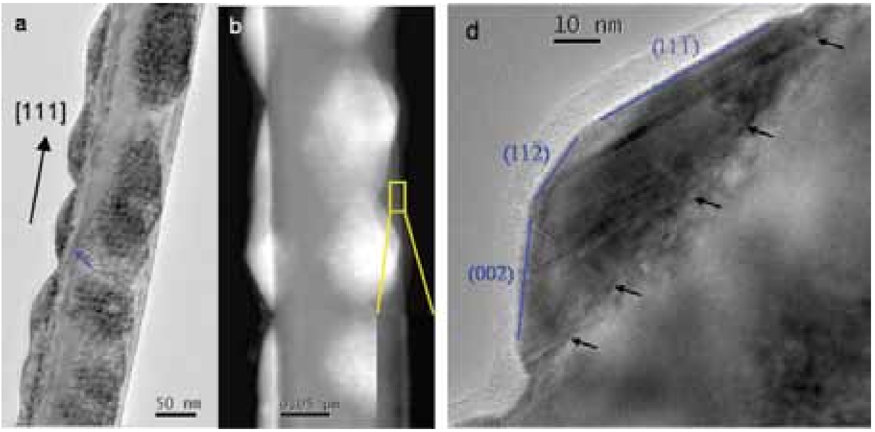
- The reflectance, transmittance, and absorption spectra of PDMS film show its possibility to solar cell application.
- An excellent light absorption of 90% is occurred in the NIR region.
- Accordingly, the incident light wave can easily penetrate through the PDMS film , reaching the Si wire arrays and interacting with it.

Superior IR absorption of wire-embedded thin film PV

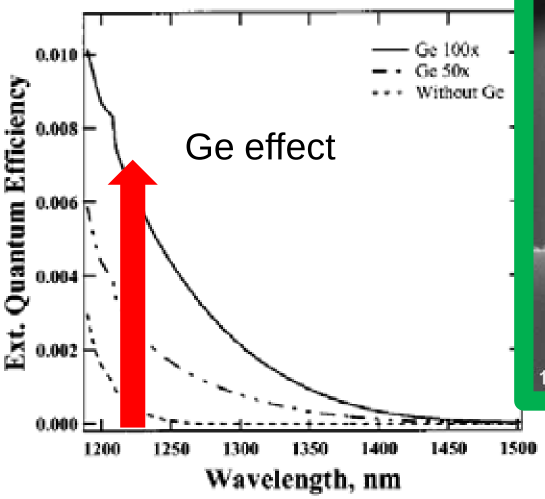


Ge NP decorated Si wired PV

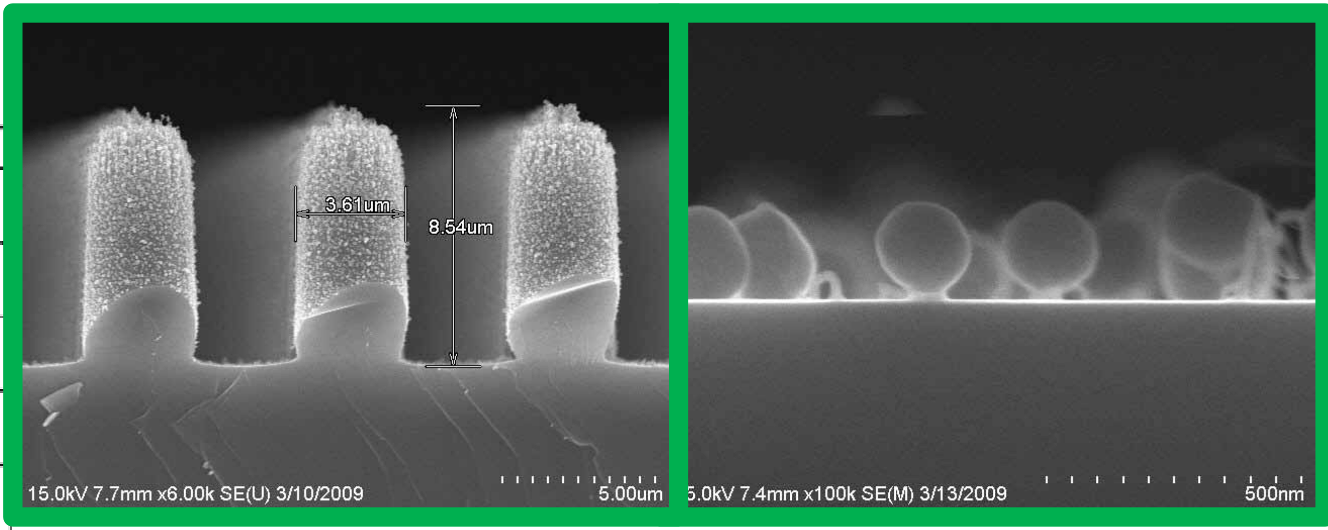




NNLT 5, 1081 (2005)



Appl. Phys. Lett., 83, 1258 (2003)



Ge NP on Si MW (한양대)

Pioneer Research Center (PRC) for Solar Thermal Conversion Nanodevices

- *Towards the nanoconvergence btw wired solarcell (top) and nanostructured thermoelectric (bottom)*

Jung-Ho Lee (PI), Bongyoung Yoo, Jong-Ryoul Kim
Hanyang University

Collaborated with
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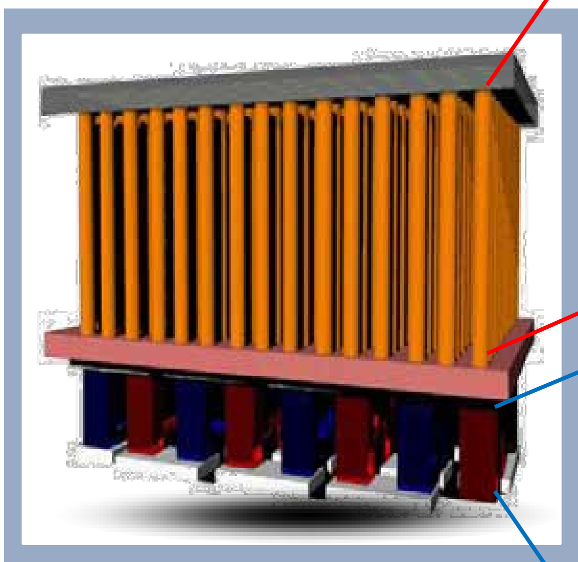
Aims and Scope

- Developing the Unified solar thermal conversion nanodevice based upon low-purity (<99.9999%) silicon with issuing the fundamental key patents

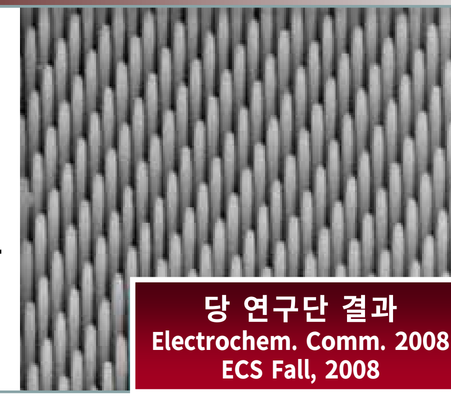
- Cell efficiency >20% for PV module (top), additionally >7% for TE module (bottom)

Device convergence with nanomaterials



Si/SiGe Microwire

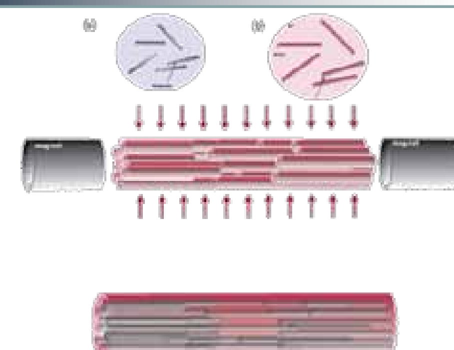
- MW 어레이에 의한 multi-scattering 효과로 태양광 반사 방지막 기능 부여
- MW 내에 radial p-n junction을 만드는 신개념으로 저순도(99.99%) 실리콘을 활용하여, 기존 기술대비 기판 단위면적당 실제 p-n junction 면적의 대폭 증가 가능



당 연구단 결과
Electrochem. Comm. 2008
ECS Fall, 2008

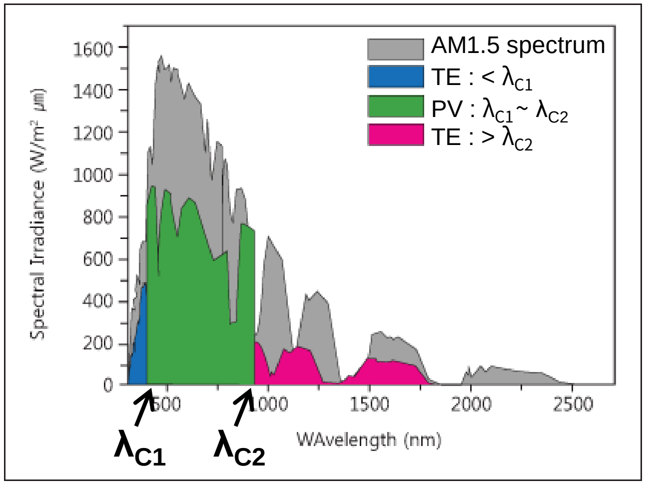
Nanostructured BiSbTe

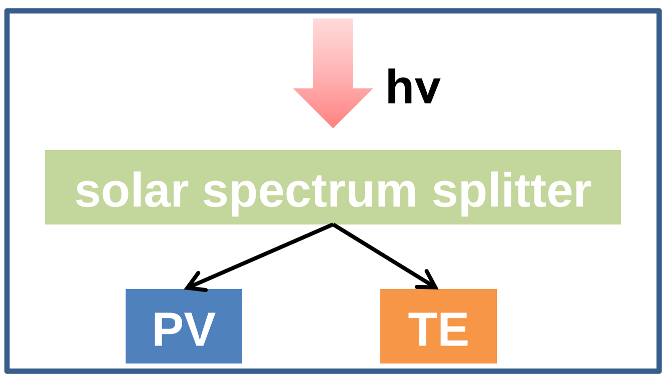
- 금속나노선이 일방향 삽입된 BiTe 나노구조체를 이용하여 낮은 (≤100°C) 온도구배에서 높은 TE 전환율 (ZT^{3} 1.5) 확보 가능



Vertical Device Convergence for PV+TE

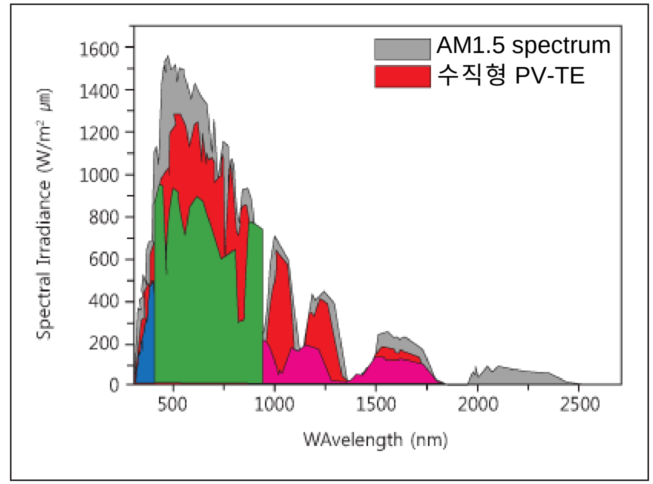
Current PV-TE convergence

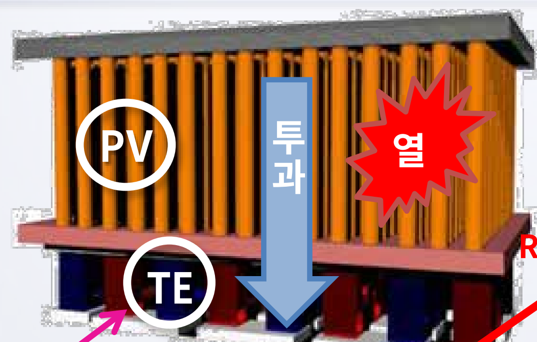




$\eta_{c,total}$ $\eta_{PV} + \eta'_{TE}$

Next-generation version





Recycling thermal loss

Recycling transmission loss

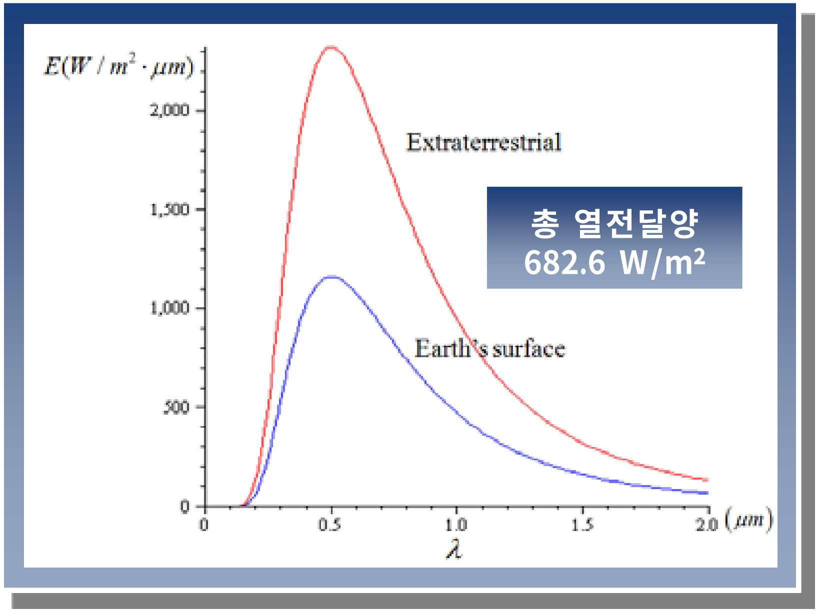
Cooler 역할

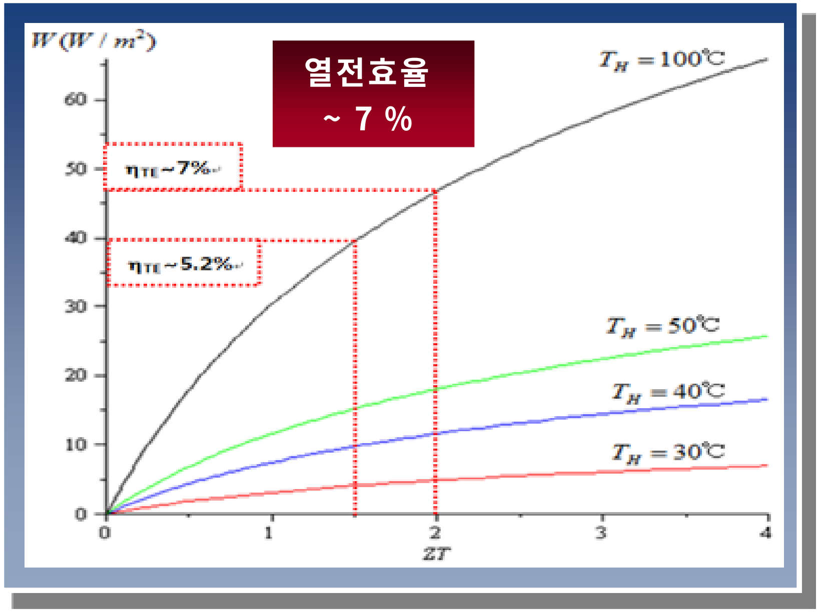
$\eta_{c,total}$ $1.15 \times \eta_{PV} + \eta'_{TE}$

$(\eta'_{TE} > \eta_{TE})$

나노복합 열전소자의 PV-TE 통합소자 내 발전 효율 평가

- 효율 추정 조건 : Hot zone 온도 = 100 °C , Cold zone 온도 = 23 °C
  (ΔT = 77 °C), ZT = 2
- 단위면적당 총 이동 열전달 양은 782.6 W/m²
- T_H=100 °C인 경우에 ZT=2를 갖는 소재를 채용시 ZT에 따른 발전용량은 46 W/m² 이며, 이는 열전효율 ~7%에 대응하는 결과로 도출됨





연구단 구성 및 전문성

세부추진분야	연구원구성	
WG1 **Device Convergence**	• 이정호: 한양대 • 김동욱: 이화여대 • 손영수: 대구가톨릭대 • 조용우: 한양대	PV & TE device의 융합을 위한 산학연 반도체 소자 및 공정 전문가
WG2 **PV device and Measurement**	• 조형균: 성균관대 • 김영규: 경북대 • 김재현: 대구경북과학기술원 • 김종렬: 한양대	Si wired solar cell 제작 을 위한 태양전지, 유무기합성 및 Si 나노구조 전문가
WG3 **TE device and Measurement** (註) * 신진연구자 전체15명 중 10명	• 이규환: 재료연구소 • 오민욱: 한국전기연구원 • C. Yu: Texas A&M Univ. • 유봉영: 한양대 • N. V. Myung: UC Riverside •임동찬: 재료연구소	BiTe nanostructured TE소자 제작을 위한 BiTe 열전소자, 측정, 유기, 전기화학 산학연 전문가

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Thank you for your attention!