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Opportunities and Challenges for Nanoelectronic Devices and Processes

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Status Quo for "Moore" and "More Moore"

- **CMOS Scaling is not coming to an end**
  - **45 nm is happening**
  - **32 nm well on its way**
  - **22 nm will happen**

- **Major ongoing transformation of scaling caused by power and power/density**

- **End of frequency scaling of single core processor**
  - **No "10 GHz" microprocessor (with the ~100 W cooling limit)**

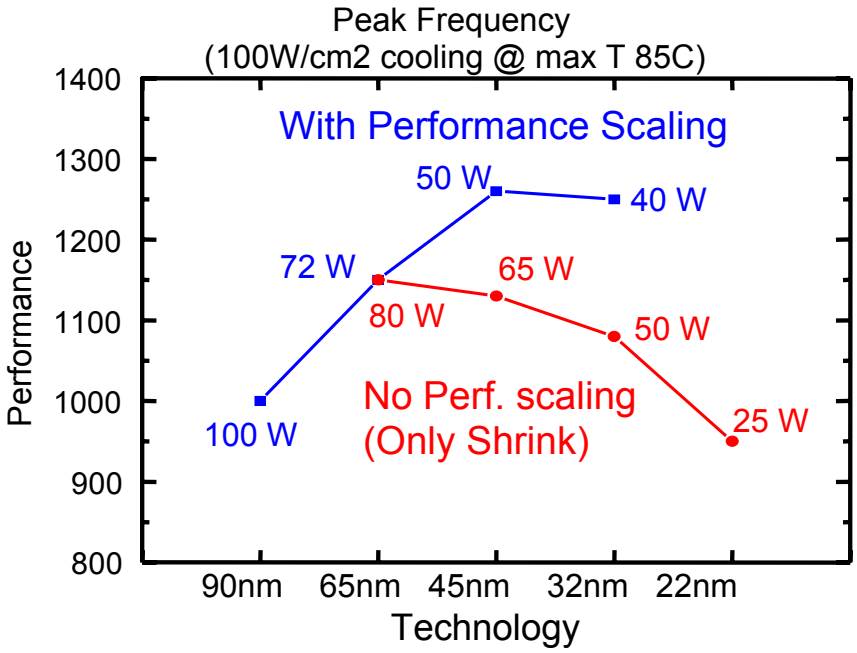
- **System performance based on multi-low-power cores and accelerators**
  - **Move away from frequency scaling**

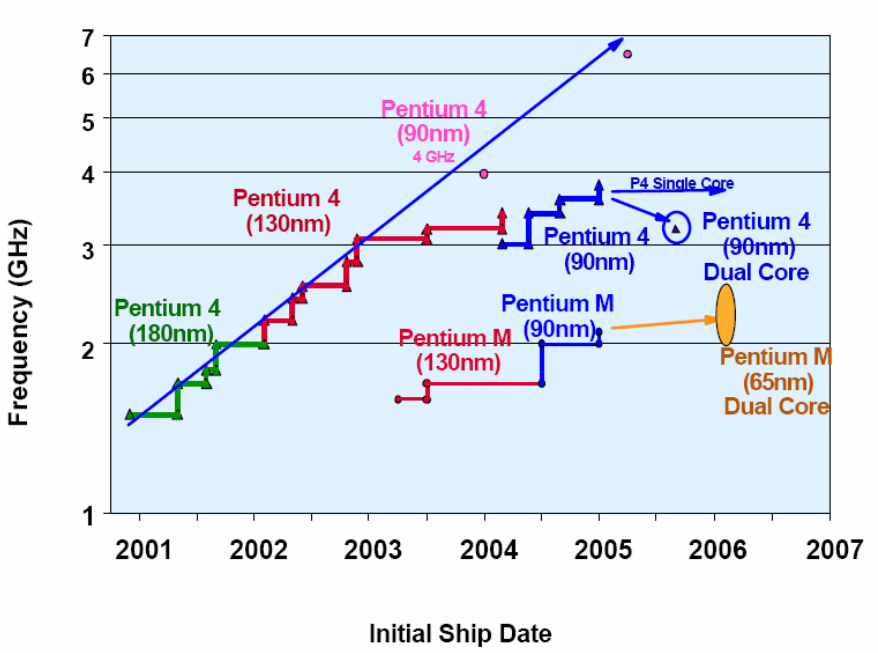
- **How many "Moore" generations?**
  - **As long as we have affordable lithography**

G. Shahidi, IBM

Paradigm Shift: Hitting the Cooling Limit

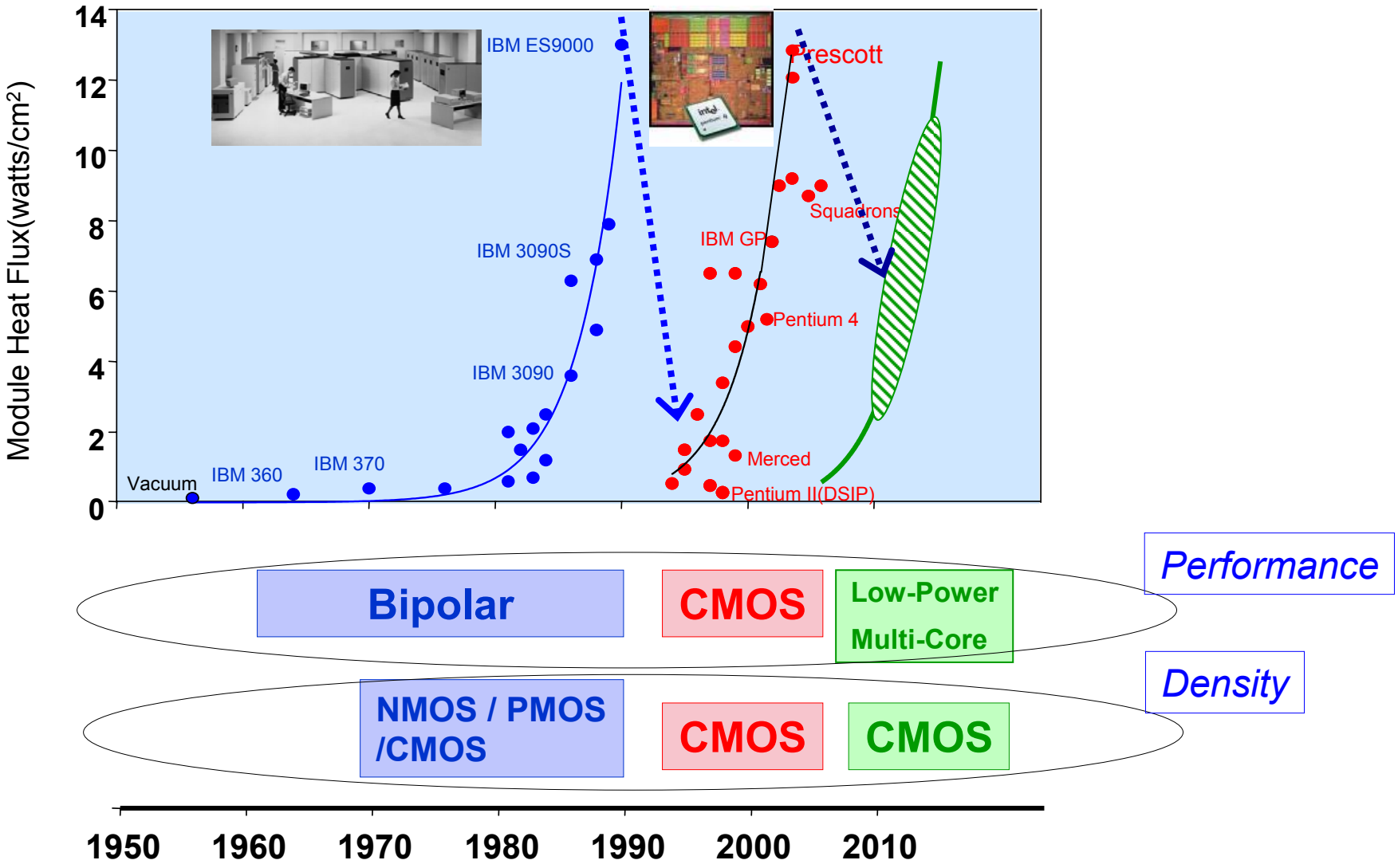
- Moving a high power chip to the next node (with limitation on cooling and maximum T rise), actually will slow it down





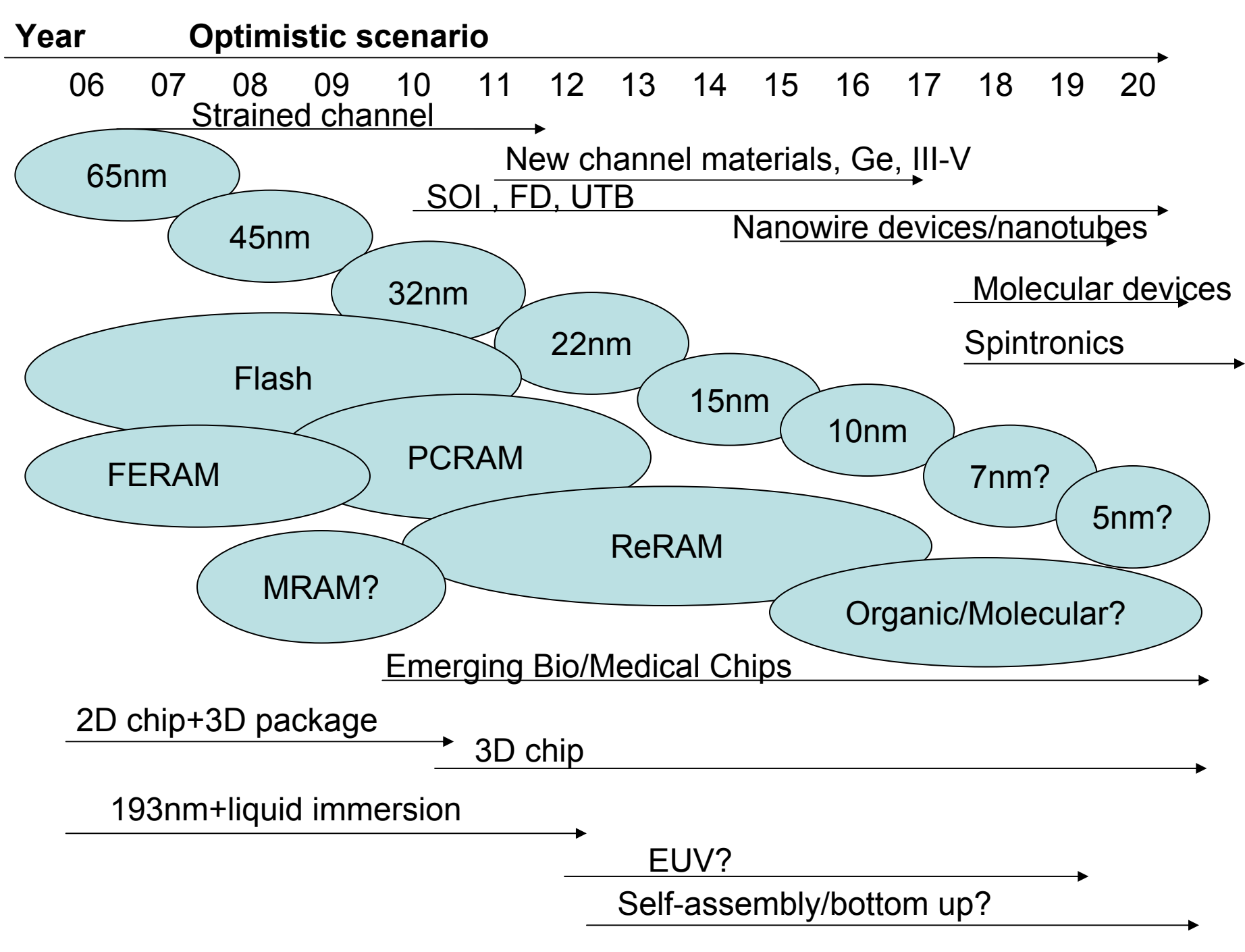
End of frequency scaling @ ~4 GHz (with 100 W cooling)?

System Performance from Multi-Cores



"Beyond Moore" On-going Trends

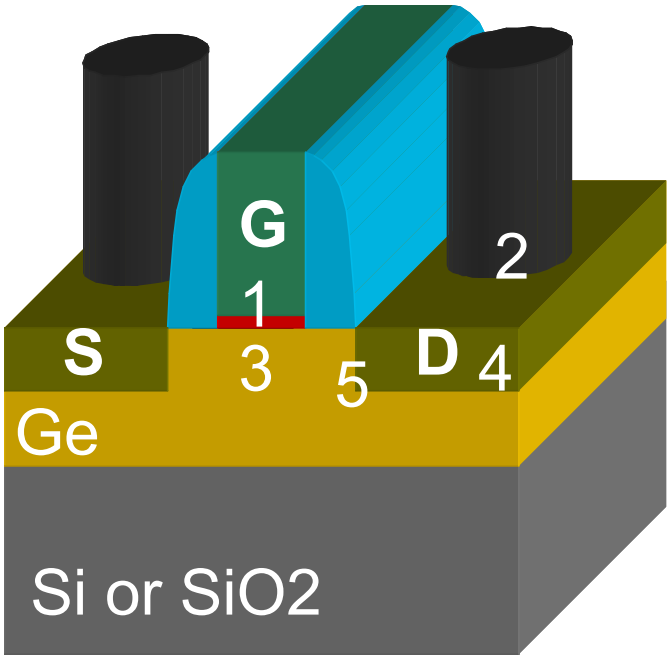
- **Nanoelectronics: Ge, III-V channel to nanowire/nanotubes and more**
- **Nano-bio/medical: Bio-sensing, imaging**
- **Energy: nanowire solar, nanotube hydrogen storage**
- **Environmental sensing: Sensor network, gaseous molecules sensing, ocean, air…**
- **Fusion of nanoelectronics and nanomechanical: New switches and memories**


Year
Optimistic scenario
06 07 08 09 10 11 12 13 14 15 16 17 18 19 20
Strained channel
65nm
New channel materials, Ge, III-V
SOI , FD, UTB
45nm
Nanowire devices/nanotubes
32nm
Molecular devices
22nm
Spintronics
Flash
15nm
10nm
PCRAM
FERAM
7nm?
5nm?
ReRAM
MRAM?
Organic/Molecular?
Emerging Bio/Medical Chips
2D chip+3D package
3D chip
193nm+liquid immersion
EUV?
Self-assembly/bottom up?

High mobility channel Ge and its issues

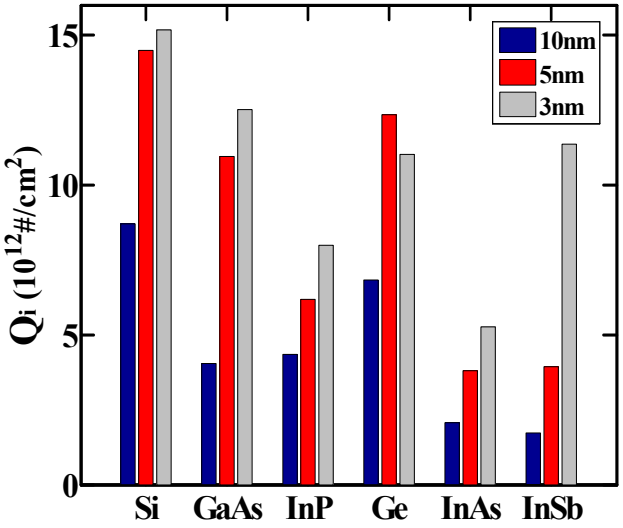
- Advantages
  - High electron/hole mobility
  - Compatibility to Si LSI
  - Lower temperature process
  - Possible V_{dd} scaling
- Process and device Issues
  1. Poor interface property of Ge MOS gate
     - Loss of Q_{ch} and m degradation
  2. Strong Fermi-level pinning at metal/Ge contact
     - Increase contact resistance
  3. Small electron mobility gain
     - Require mobility booster
  4. Poor N-type dopant activation
  5. Band-to-band tunneling leakage

	Si	Ge
Electron μ (cm^2/Vs)	1600	**3900**
Hole μ (cm^2/Vs)	430	**1900**
Band gap (eV, 300K)	1.12	**0.66**
Dielectric constant	11.9	**16**

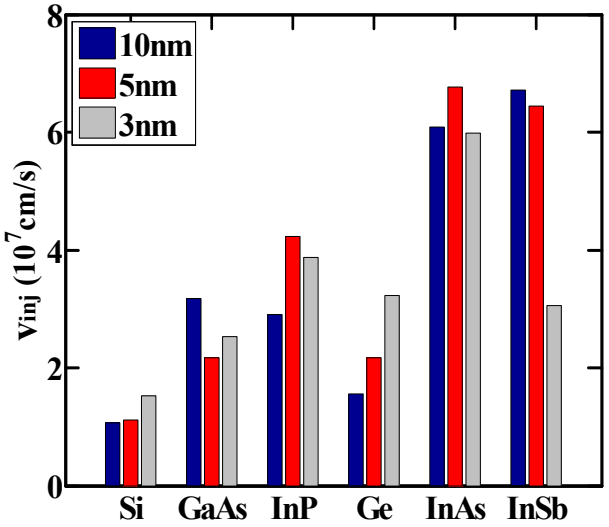


NMOS Performance Comparison Simulation

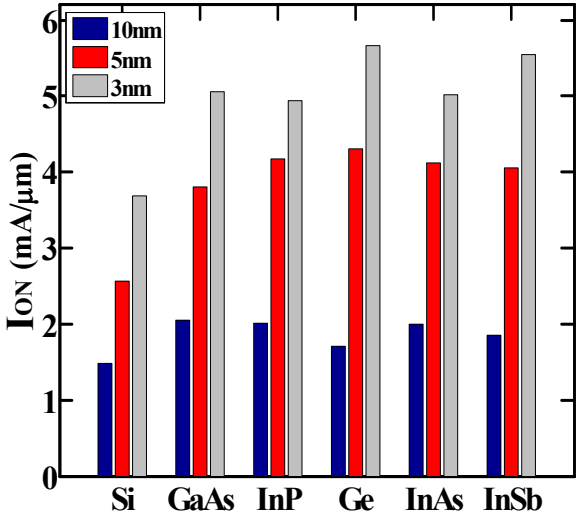
Channel Charge (Q_i)

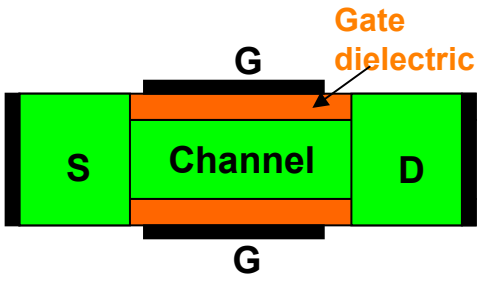


Injecion Velocity (V_{inj})



On current (I_{ON})





L_G=15 nm
T_{OX}=0.7 nm
V_G=0.7V

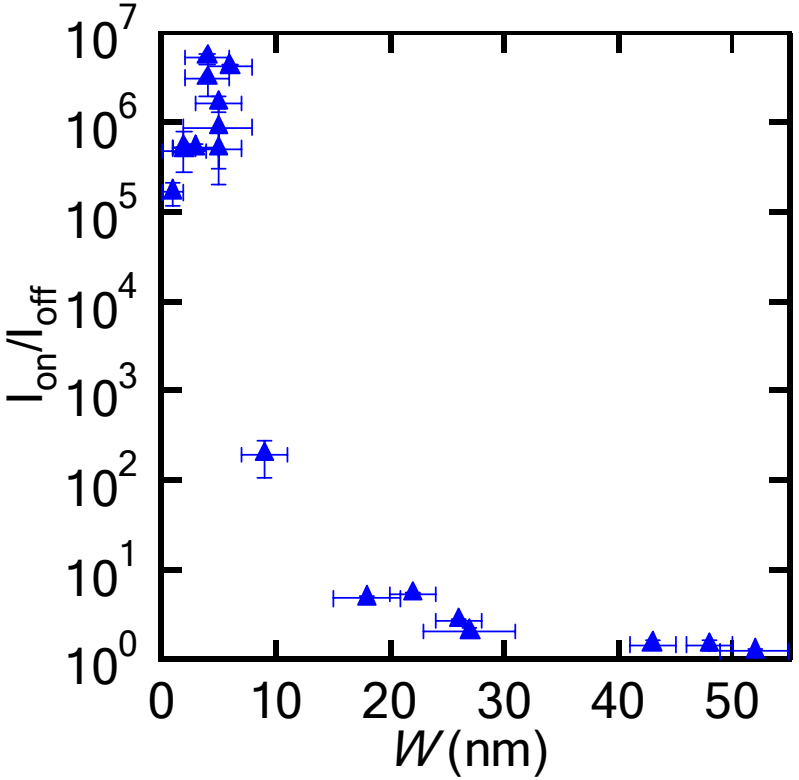
- Si high Q_i low V_{inj}
- III-V low Q_i high V_{inj}
- Ge reasonably high Q_i and V_{inj} has highest I_{ON}
- Effect of strain is being modeled

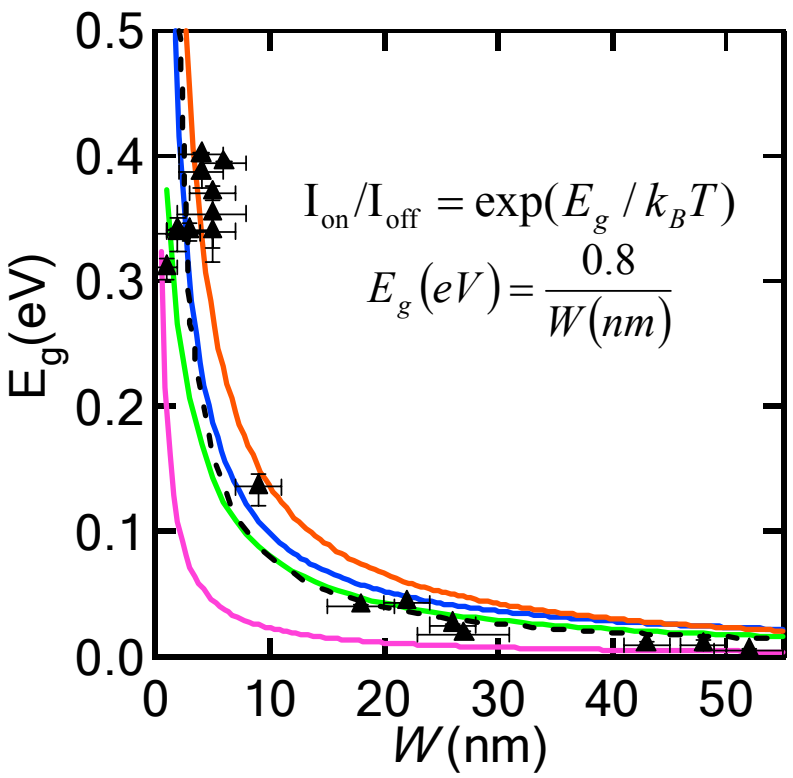
Kim, Krishnamohan & Saraswat, IEEE DRC 2008

Non-silicon high mobility channel approaches

- It will fulfill the needs for “higher speed and lower power consumption”
- High mobility materials-gate insulator interface is the biggest issue
- Ge option may provide an opportunity for on-chip optical interconnect; at least for detector, and maybe for transmitter
- Integration density would stay with Si VLSI trend line (ITRS)
- Preferential application on top of the Si platform looks rational option to go

ON/OFF & Bandgap vs. width for GNRs

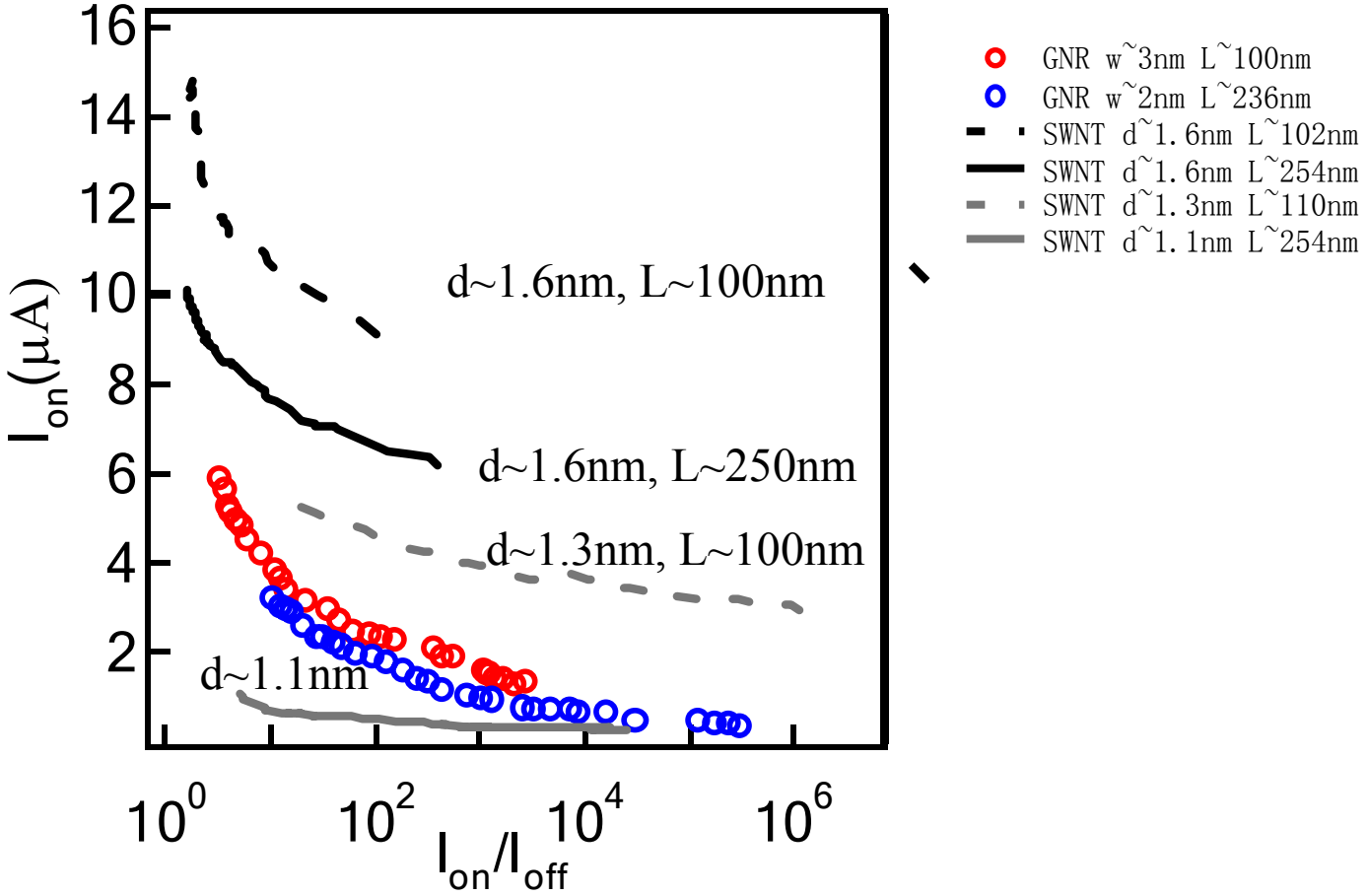




- All (> 40) sub-10nm GNRs measured thus far are semiconducting with high on/off switching at 300K

H. Dai, Stanford, 08

Graphene ribbon vs. Carbon Nanotube



- High on/off GNR comparable to~1.2nm SWNT FETs
- GNR FETs comparable to high performance SWNT FETs (d~1.4-1.5nm) remains illusive

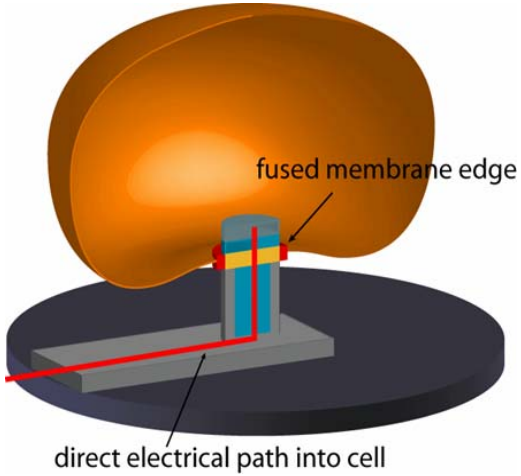
H. Dai, Stanford, 08

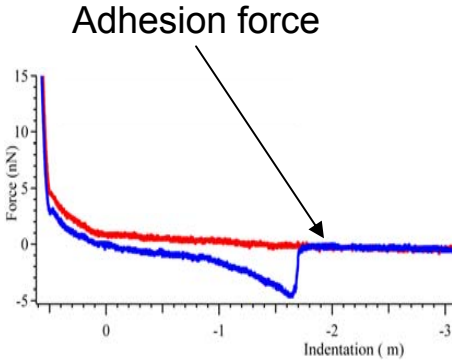
Integration Challenges of CNT, GNR etc

- Enough performance advantage over other options as individual devices
- A large variety of tunability for the band structure for a number of applications
- Questions for controlled growth for nanowires and nanotubes still remain without sacrificing integration density
- No top down lithographic technology for the geometry ranges of GNR
- Variability

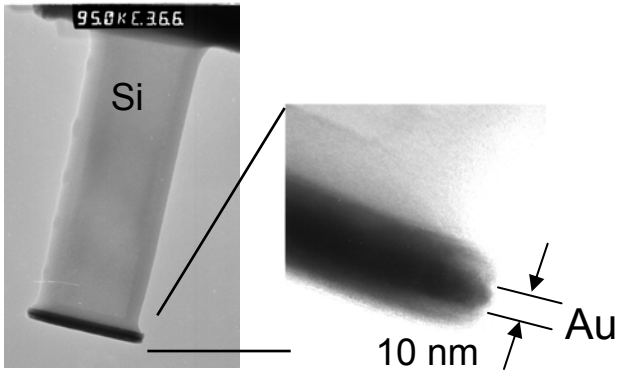
Integration of Electronics into Cells

- nanoscale-functionalized probes at the end of AFM cantilever tips that can directly integrate into a cell membrane.
- “stealth electrodes” do not cause membrane damage, and specifically attach to the core of the lipid bilayer.
- future work will involve fabrication of planar arrays of the devices for on-chip electrophysiological measurements.





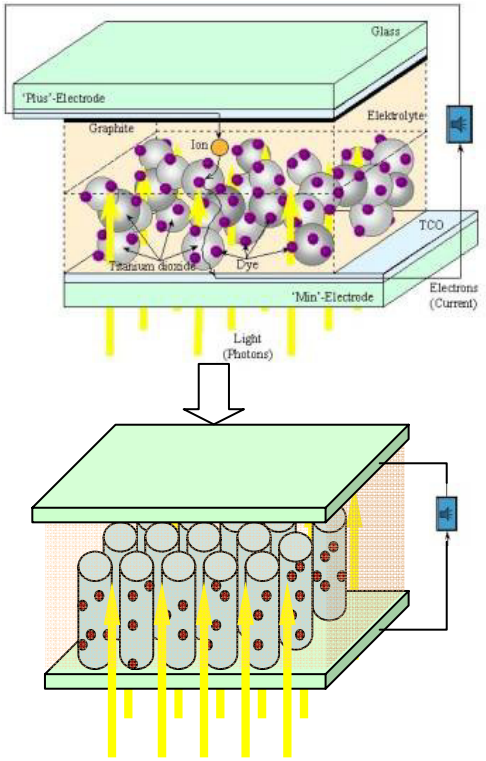
AFM force measurements of the tip interaction with the bilayer.



A nanoprobe tip.

Professor Nicholas Melosh,
Department of Materials Science and Engineering, Stanford University

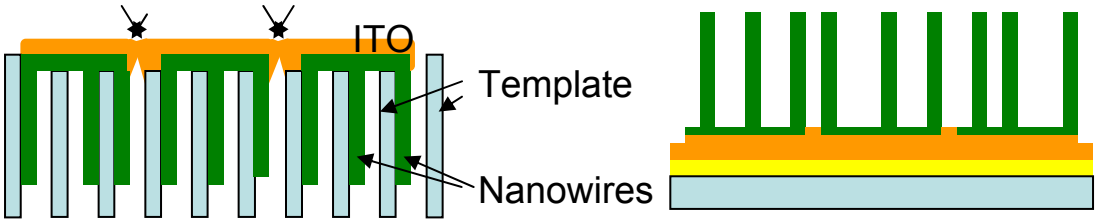
Nanowire Dye-Sensitized Solar-Cells



Dye-sensitized solar cell is one of the most promising third generation solar cells. Using semiconductor nanowires array, as the electron conducting material to replace nanoparticle film, can achieve both a large surface area and a low intrinsic resistance as well as an improved energy conversion efficiency.

The idea of this project is: First, using templated Sol-Gel method to grow high aspect ratio and high density TiO_2 nanowire array; Secondly, providing bonding of the wire array to a transparent and conductive layer by "after-growth" deposition of materials like ITO onto the back of the nanowire array; Then, dissolving the template following attaching the sample onto a substrate; Finally, this substrate can serve as the anode of the dye-sensitized solar cell.

The above nanowire fabrication method can exceed VLS or CVD in aspect ratio and density, and exceed powder based porous array deposition in minimized grain boundaries existing in the electron diffusion paths.



Sputtering ITO

After Dissolving Template

Ying Chen and Yoshio Nishi

Summary

- A large variety of opportunities in revolutionary “nano” spaces, from traditional electronics to bio/medical, energy and environment
- Manufacturing strategy is still missing and challenges in “variability”, “reproducibility”, “cost” and “reliability” requires strong attentions