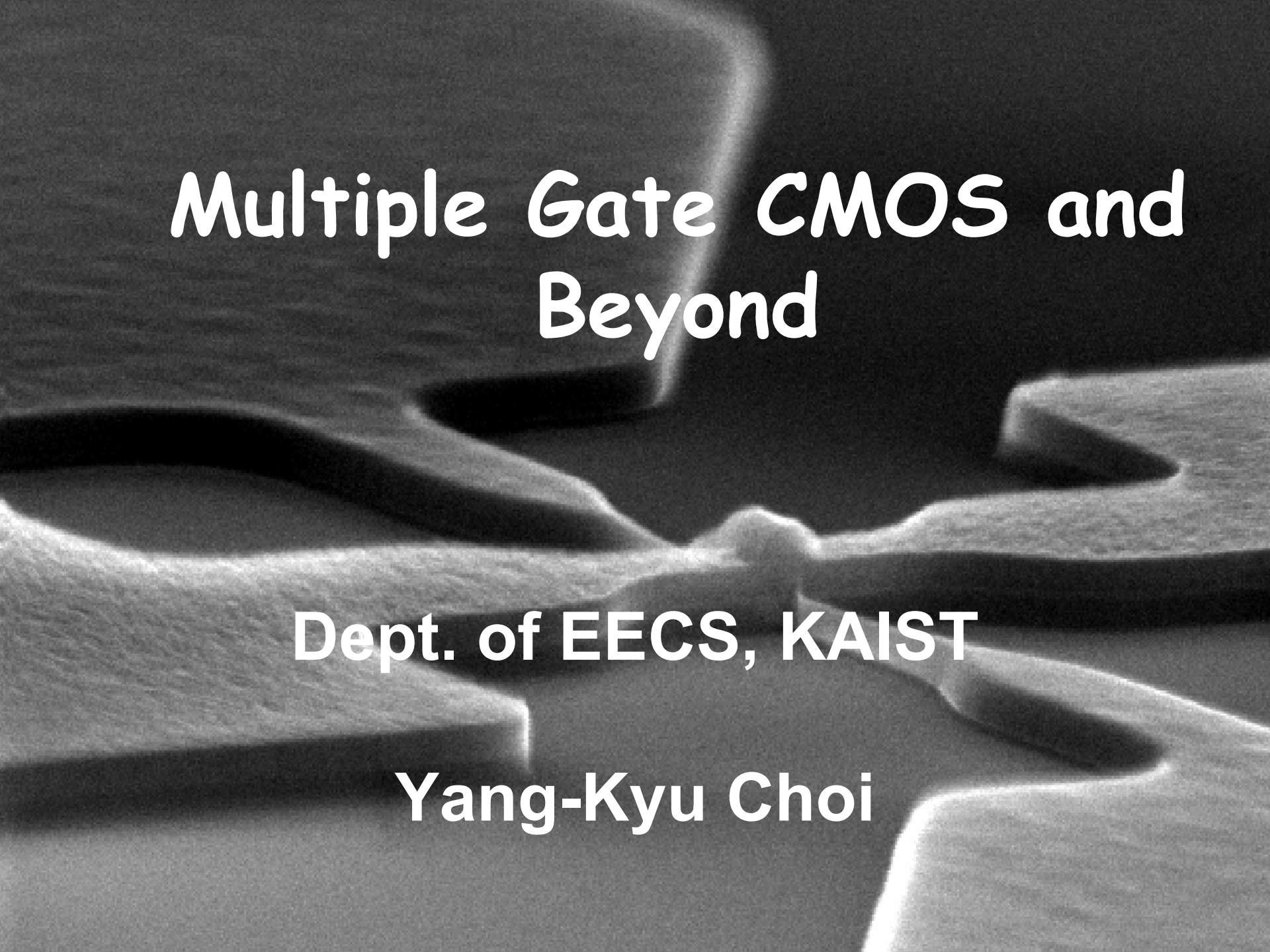


Multiple Gate CMOS and Beyond

Dept. of EECS, KAIST

Yang-Kyu Choi

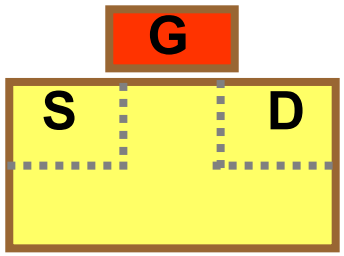
Outline

1. Ultimate Scaling of MOSFETs
   - 3nm Nanowire FET
   - 8nm Non-Volatile Memory Device

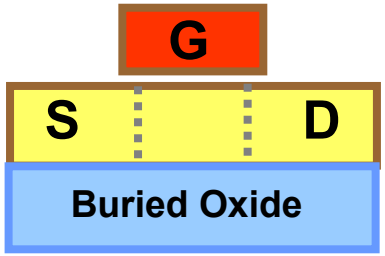
2. Multiple Functions of MOSFETs

3. Summary

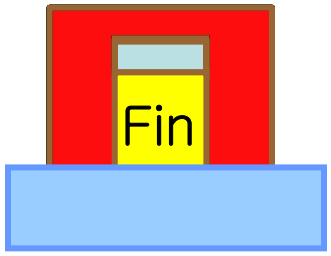
CMOS Evolution Scenario



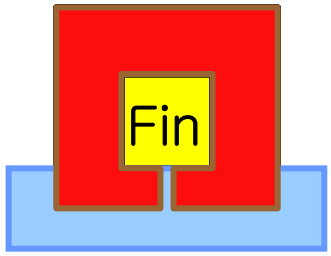
Bulk-single gate



SOI single gate

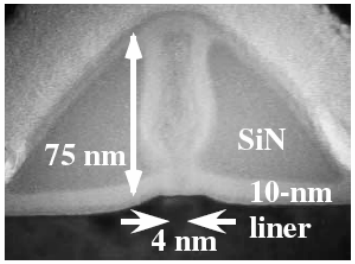


Double gate

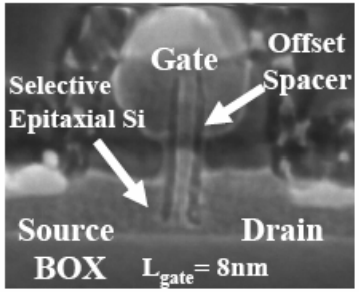


Ω-gate

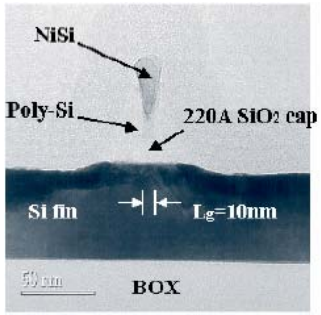
All-around



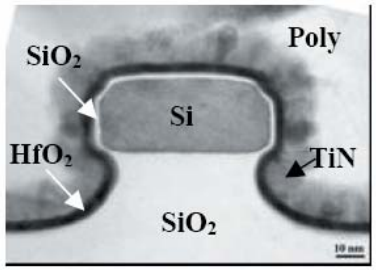
L_G=4nm
NEC
IEDM 2003



L_G=8nm
IBM
IEDM 2003



L_G=10nm
AMD/Berkeley
IEDM 2003



L_G=10nm
LETI
VLSI 2005

No report for Sub-50nm

This Work

ITRS Roadmap

		2006	2008	2011	2013	2020
L_G (nm)		28	22	16	13	5
EOT (nm)	Bulk SG	1.1	0.9	0.5		
	DG			0.8	0.6	0.5
$I_{sd,leak}$ (μA/μm)	Bulk SG	0.15	0.2	0.32		
	DG			0.1	0.11	0.11
$I_{d,sat}$ (mA/mm)	Bulk SG	1130	1570	2490		
	DG			1899	2220	2981

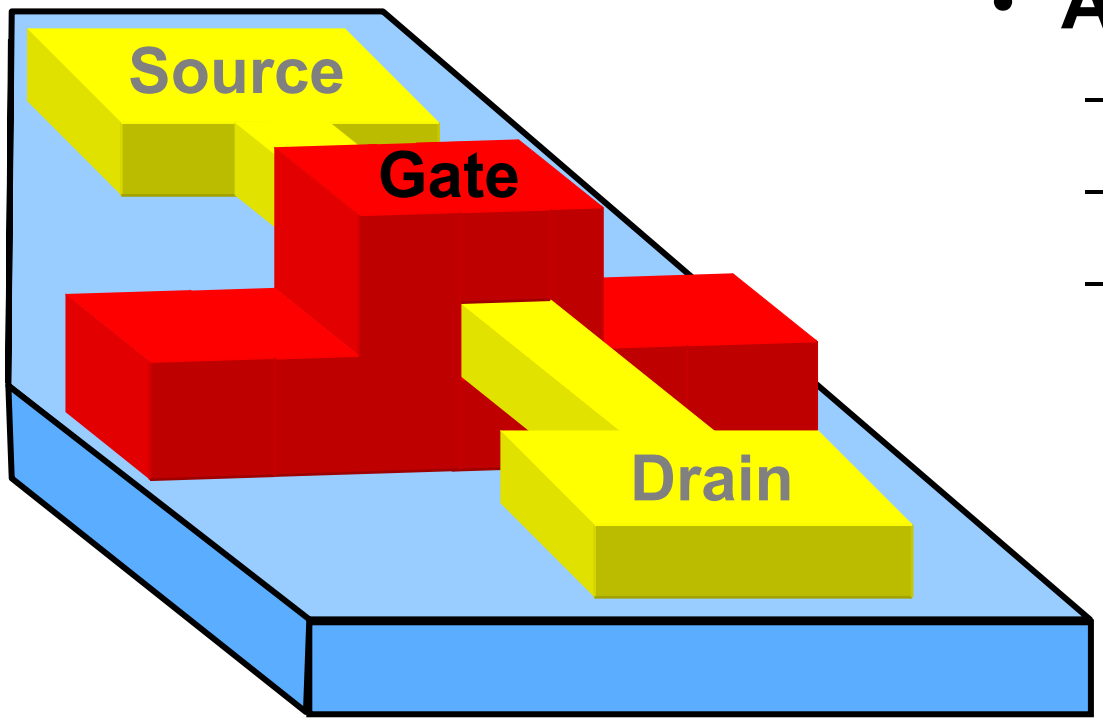
Source: ITRS 2005 roadmap

Solution exist

Solution being pursued

No known solution

All-Around Gate (AAG) FinFET

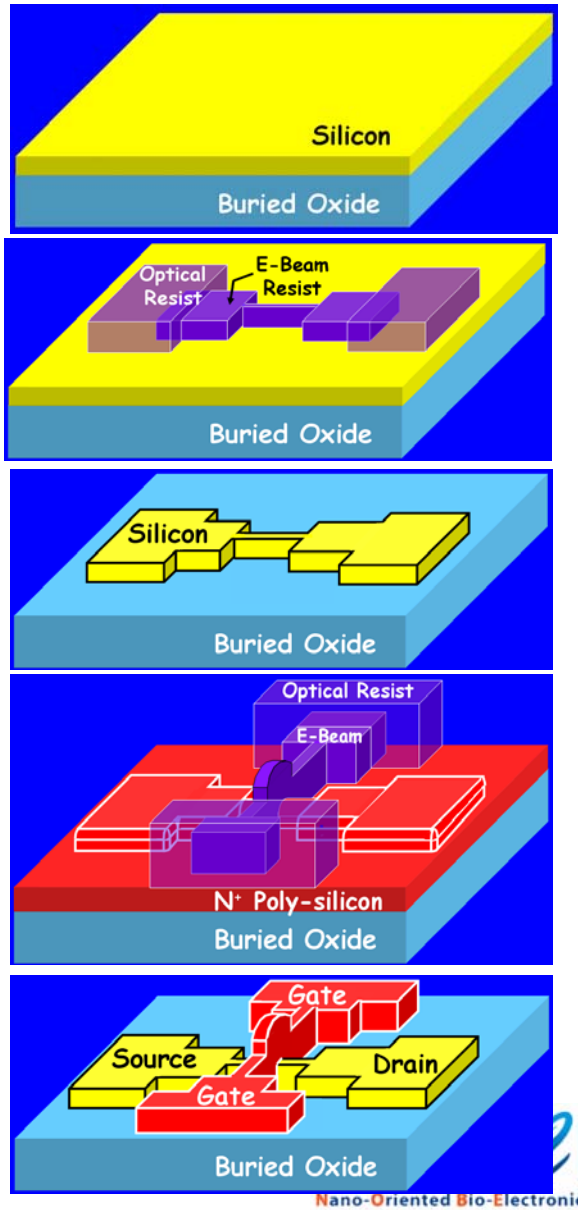


- **AAG-FinFET**
  - L_G=3nm
  - W_{Fin}=3nm
  - EOT(HfO_2)=1.2nm

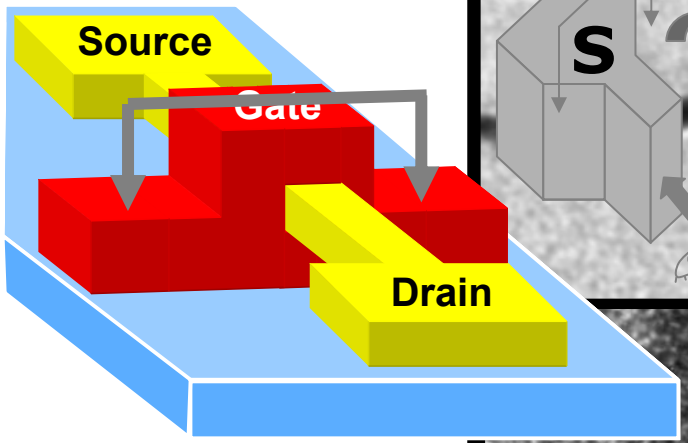
- **To fabricate sub-5nm silicon transistor, All-Around Gate (AAG) FinFET was proposed.**

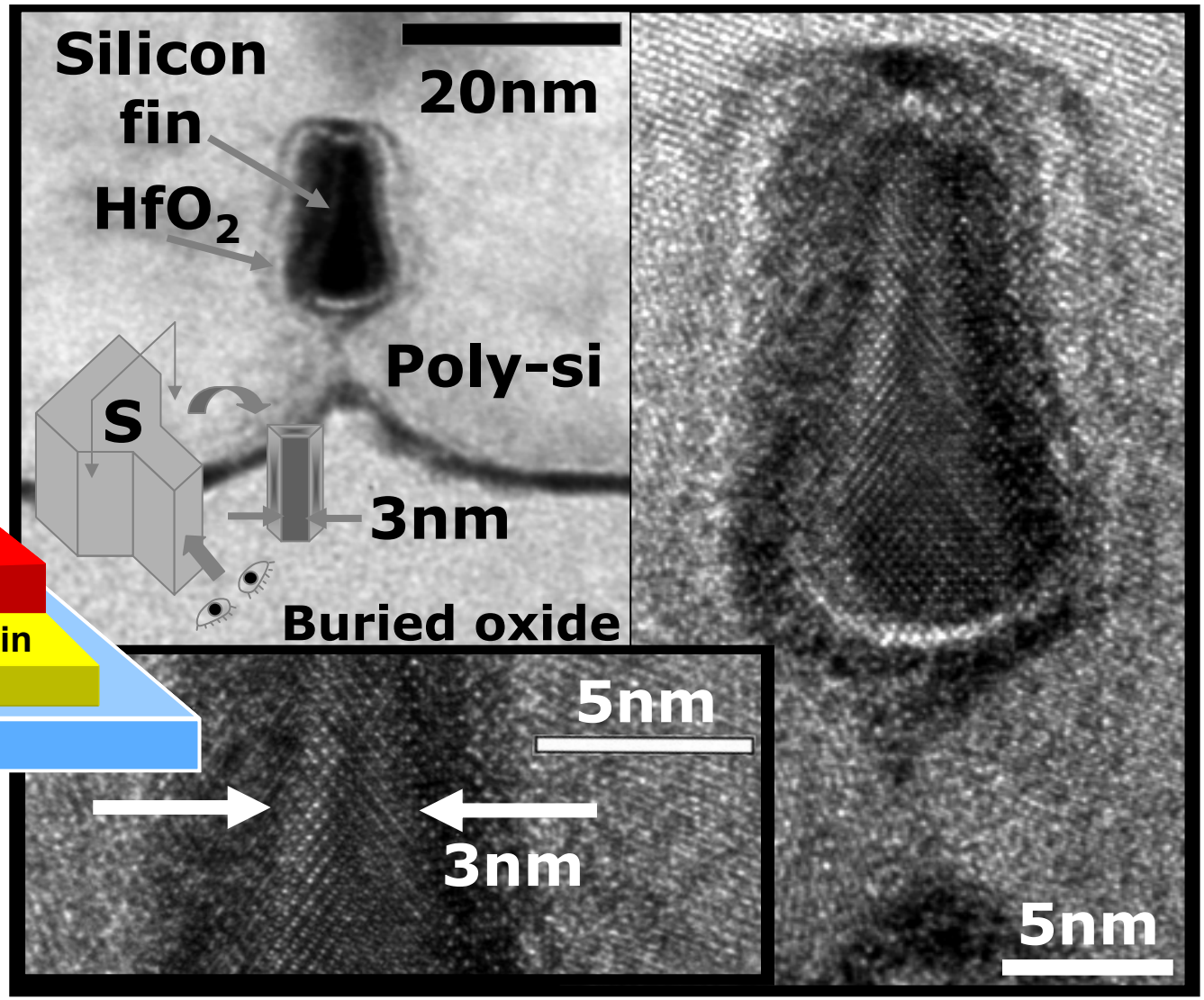
Process Flow of AAG-FinFET

- (100) SOI wafer
- Silicon body thinning
- Fin patterning (dual-resist)
- Sacrificial oxidation
- Gate dielectric (HfO_2)
- Poly-silicon deposition
- Gate patterning (dual-resist)
- Spacer formation
- Source/Drain implantation
- Spike annealing (1000°C)
- Forming gas annealing (450°C)



3nm AAG FinFET: Silicon-Fin



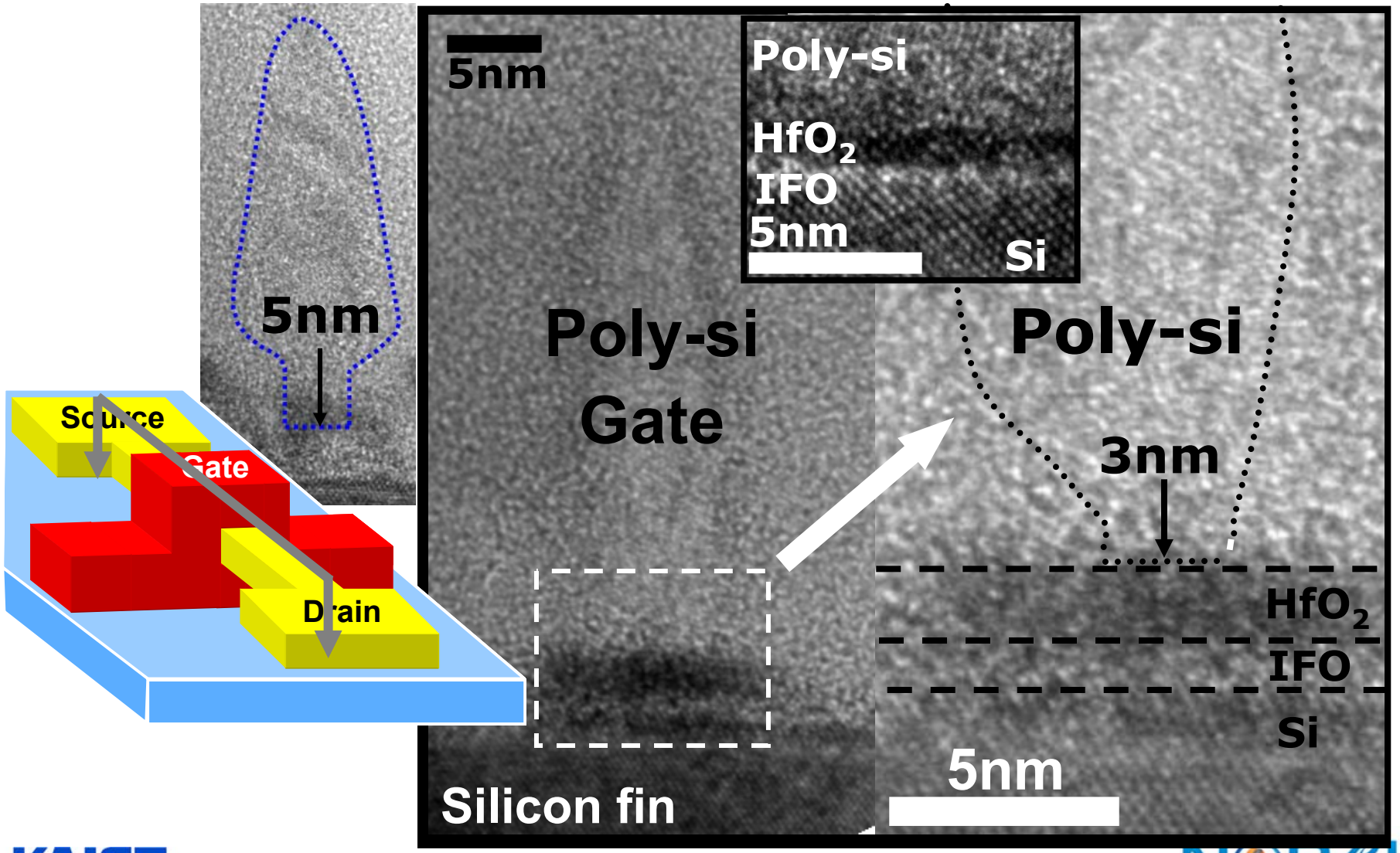


Y.-K. Choi et al., VLSI, 2006

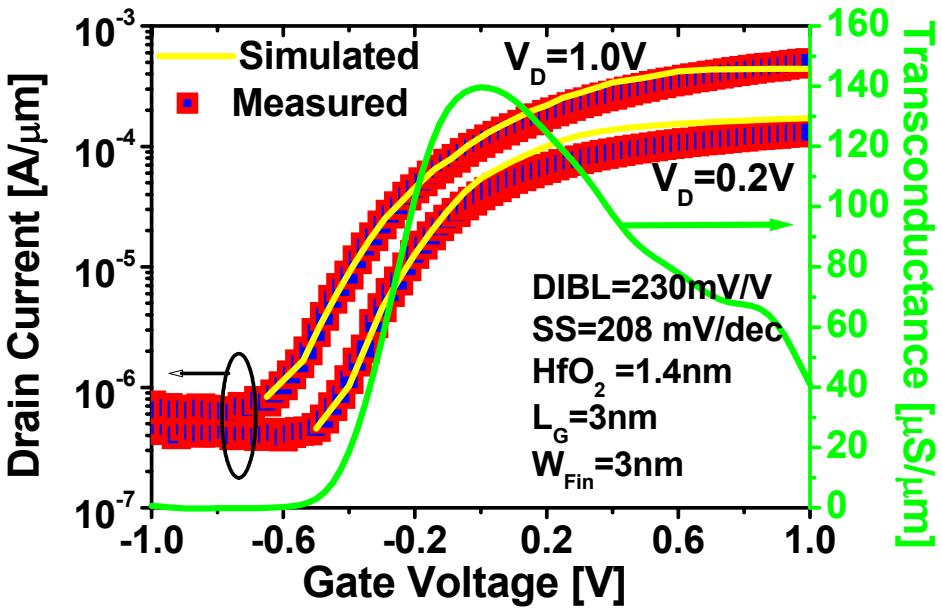
KAIST

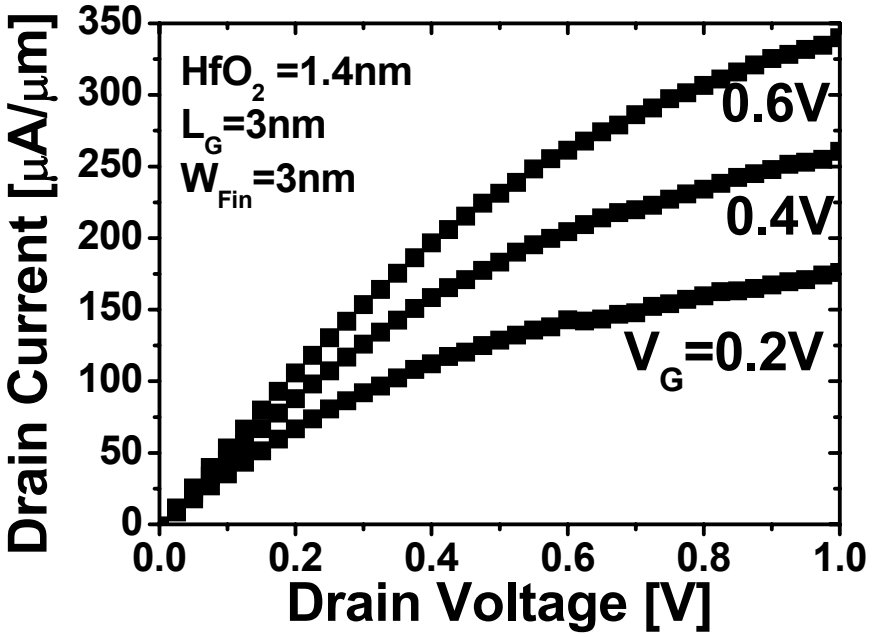
NOBEL Nano-Oriented Bio-Electronics Lab

3nm AAG FinFET: Gate



I-V of 3nm AAG FinFET





- Large DIBL and SS due to thick EOT
  - ITRS requirement: 0.5nm EOT for DG

Fundamental Limit of Scaling

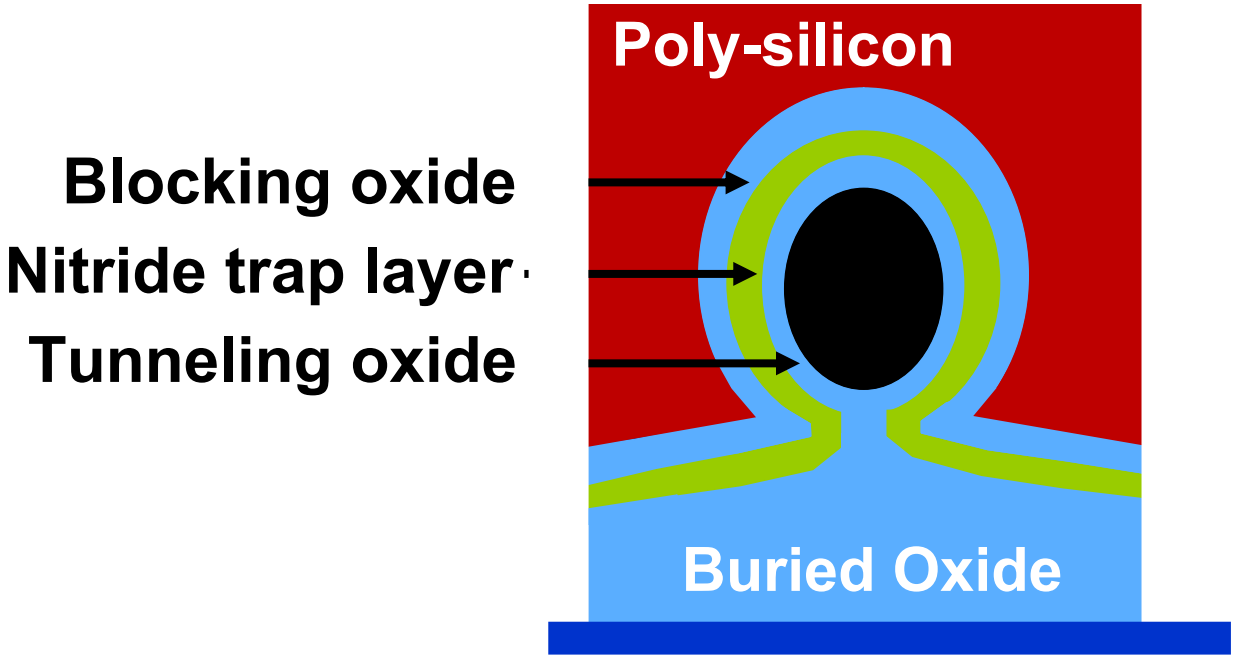
- **Device scaling limit (Operating at 300K)**
  - ***Heisenberg*'s uncertainty principle**
  - ***Shannon - von Neumann - Landauer* (SNL) expression**

$$x_{\min} = \frac{\hbar}{\Delta p} = \frac{\hbar}{\sqrt{2m_c E_{bit}}} = \frac{\hbar}{\sqrt{2m_c k_B T \ln 2}}$$
$$= 1.5nm \quad (T = 300K)$$

Fabricated 3nm all-around gate FinFET is approaching to this fundamental limit.

Nanowire Structure

- **Silicon nanowire non-volatile memory structure for ultimate scaling**



8nm Non-Volatile Memory

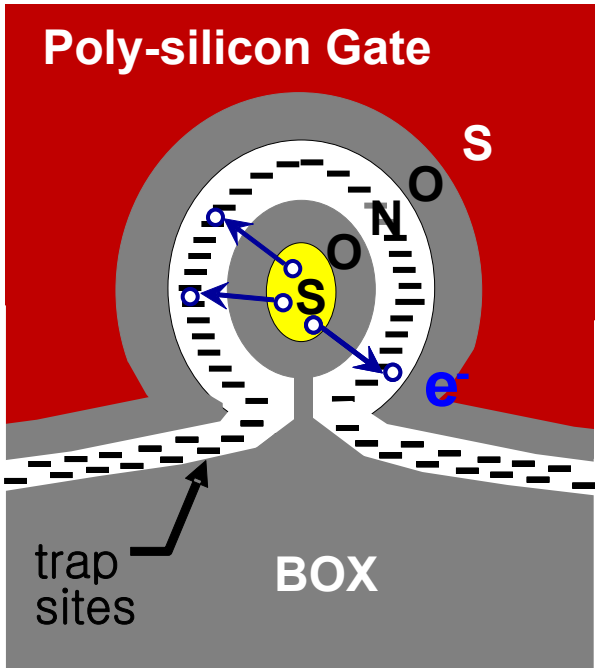
Omega-shape gate

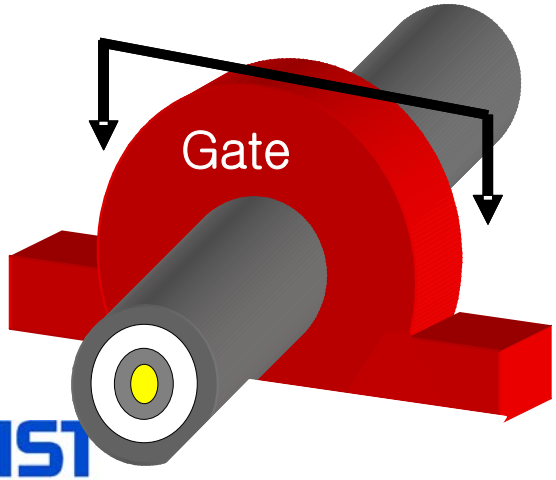
ONO-structure

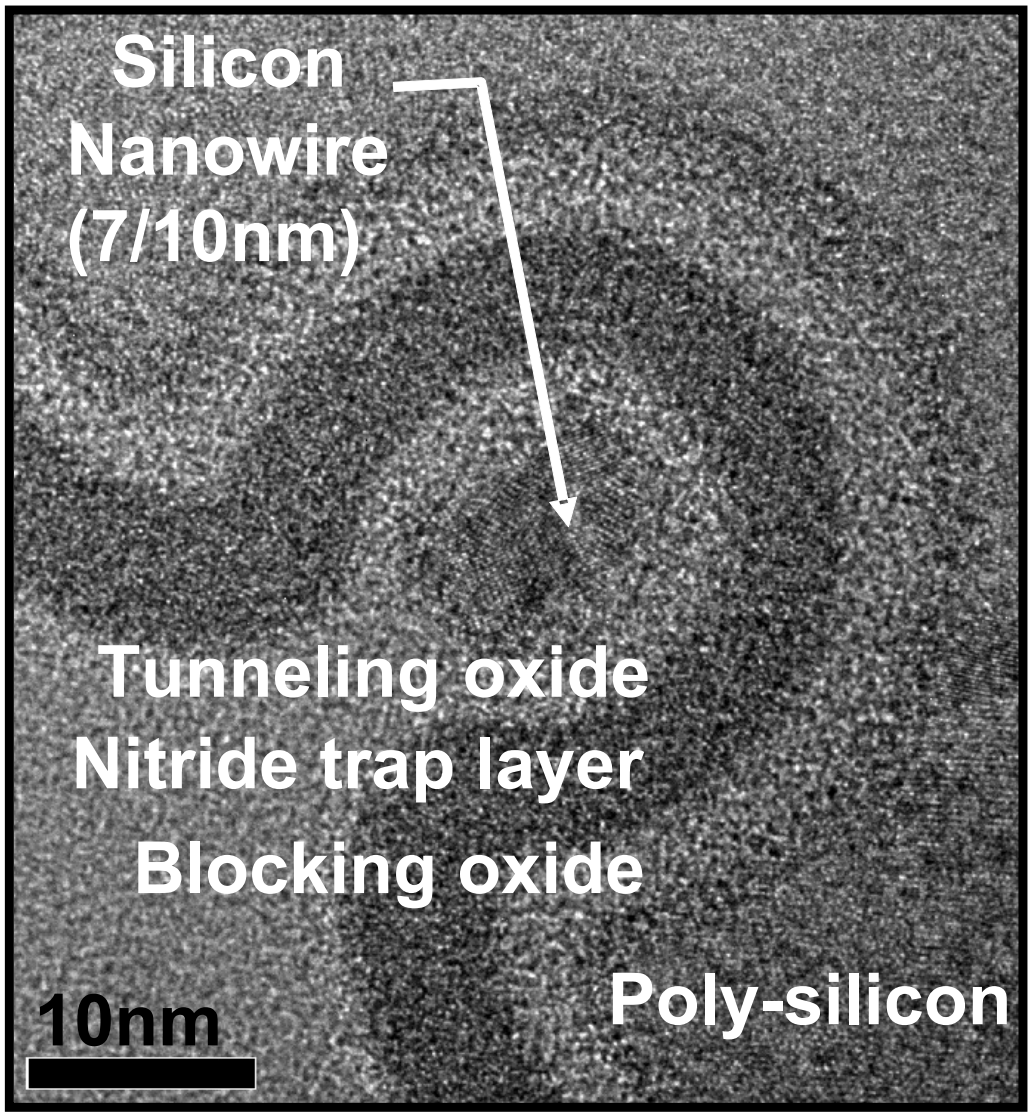
KAIST

NOBEL Nano-Oriented Bio-Electronics Lab

8nm Si Nanowire NVM





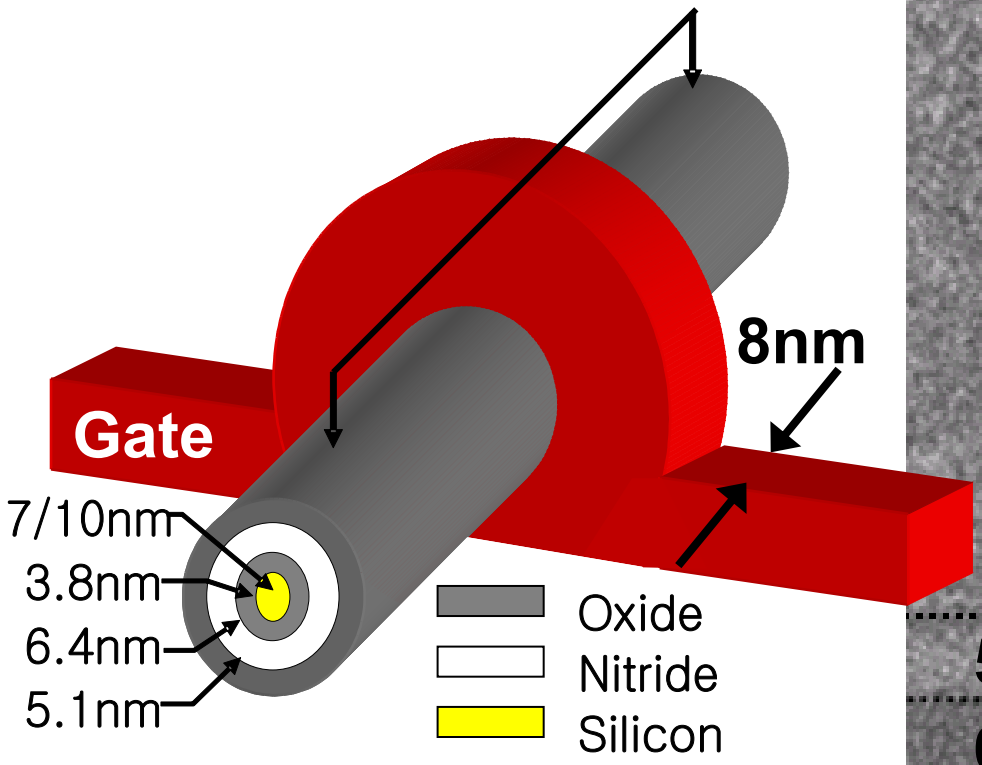


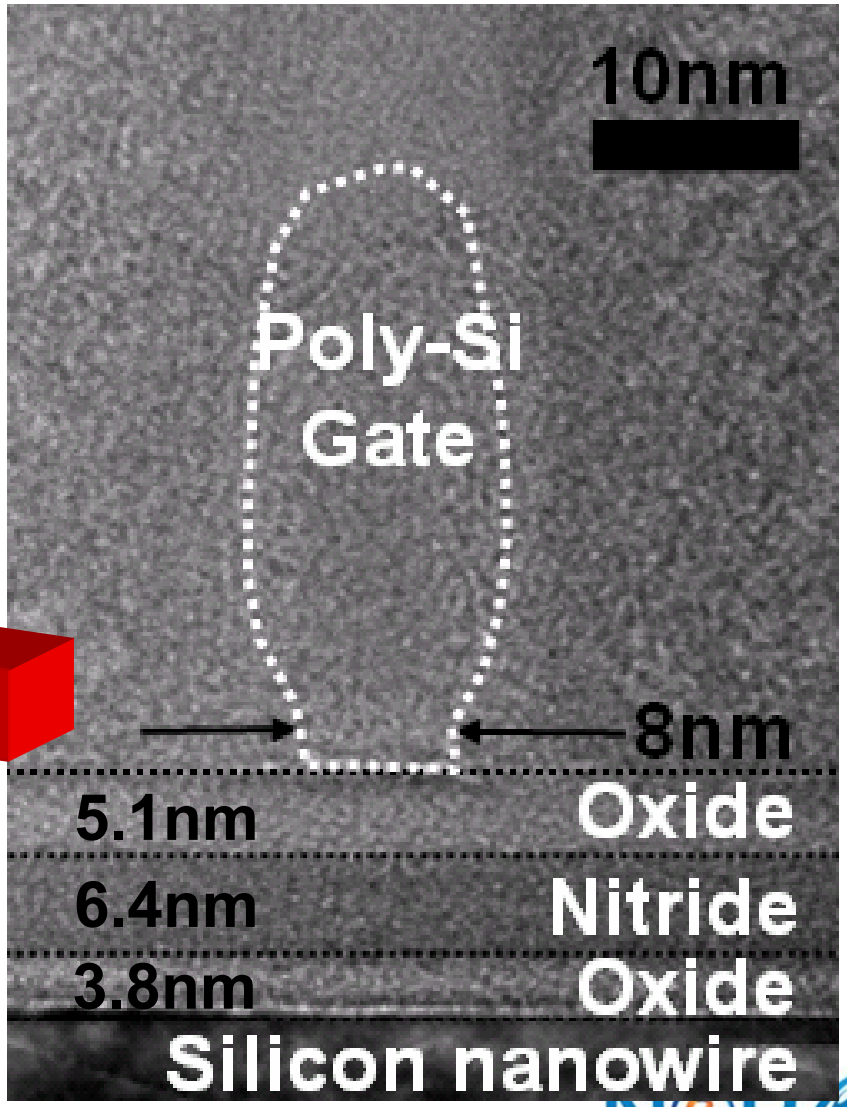
Y.-K. Choi et al., VLSI, 2007

KAIST

NOBEL Nano-Oriented Bio-Electronics Lab

8nm Si Nanowire NVM



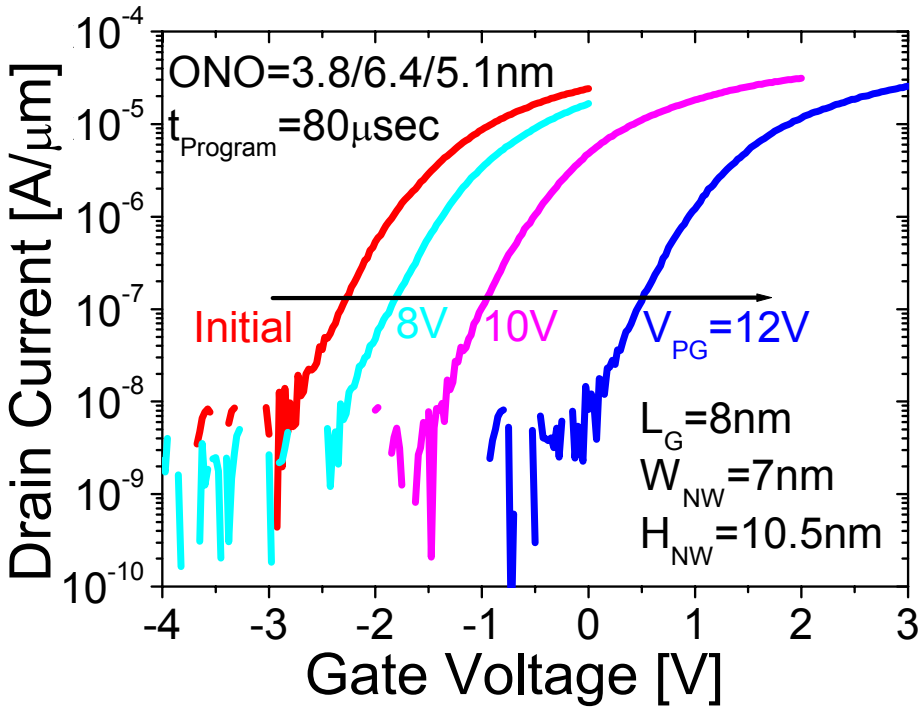


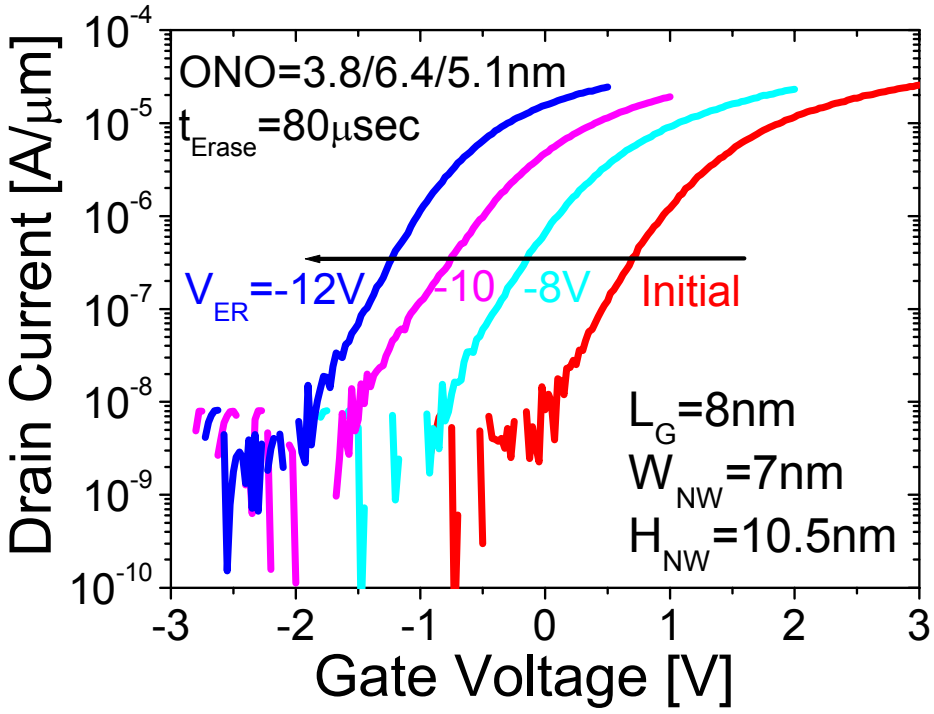
T_{ONO}=15nm > L_G=8nm

KAIST

NOBEL Nano-Oriented Bio-Electronics Lab

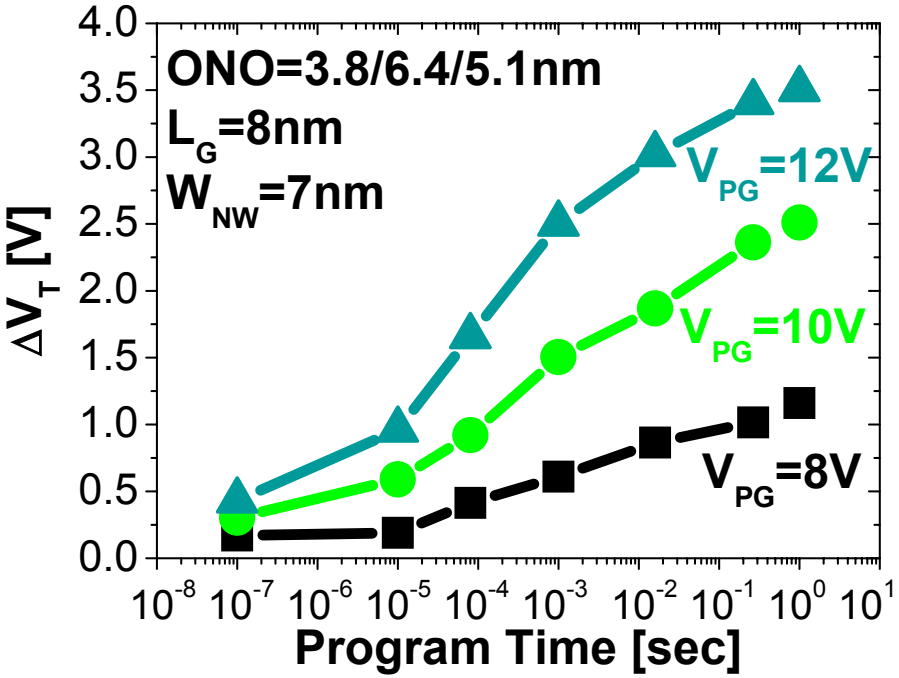
8nm Silicon Nanowire NVM with ONO

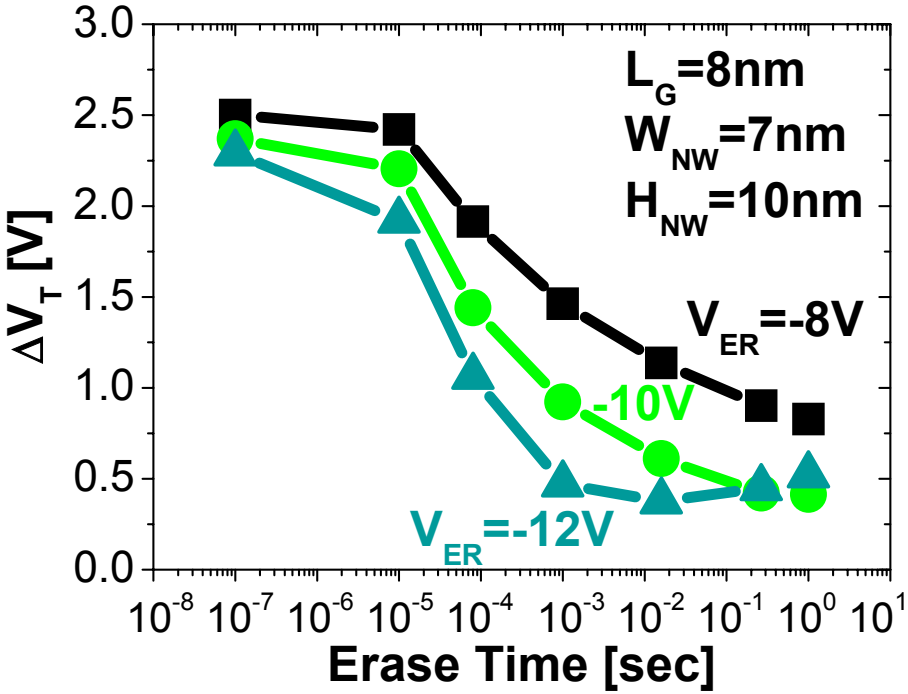




- **8nm L_G with 7nm W_{NW} using ONO-structure**
  - **Acceptable electrical performance by omega-gate**
  - **Wide hysteresis shows the probability of multi-level NVM**

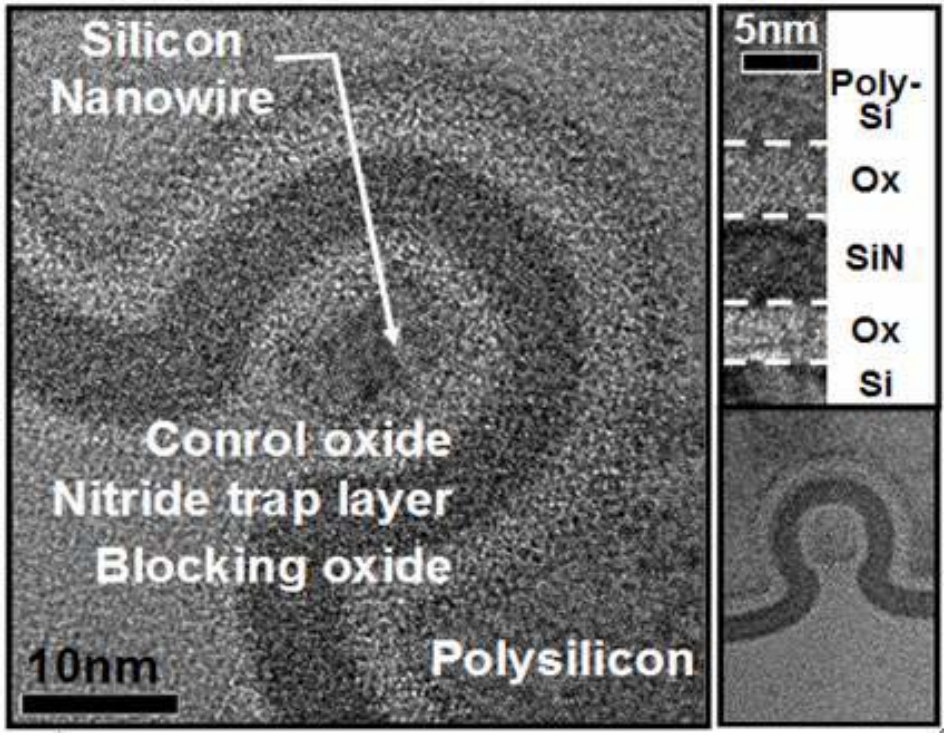
8nm Si Nanowire Memory





- **8nm NVM: V_T window = 2V**
  - **Program @ +12V/1msec, Erase @-12V/1msec**

Scaling Limit in NVM



Y.-K. Choi et. al., VLSI 2007

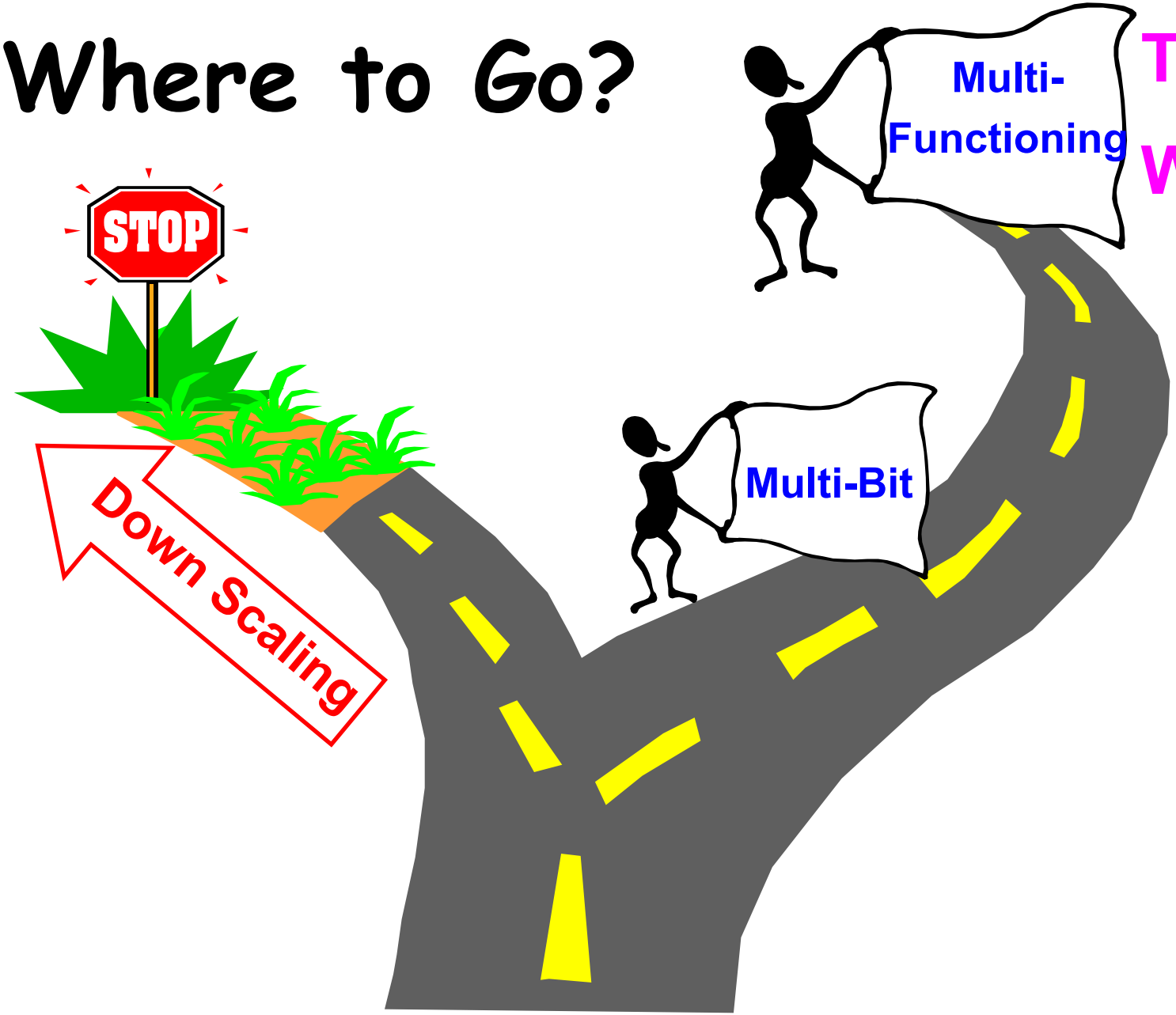
- Ultimately scaled NVM
- Nanowire + SONOS

$T_{O/N/O}$=15nm > L_g=8nm

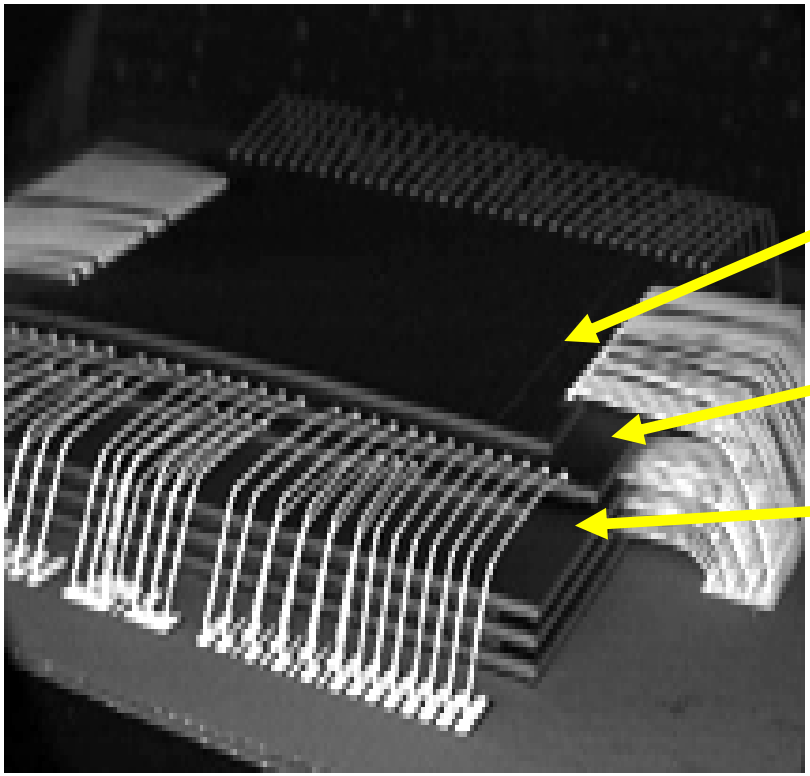
Scaling Limit !

- Close to end-point of semiconductor memory

Where to Go?



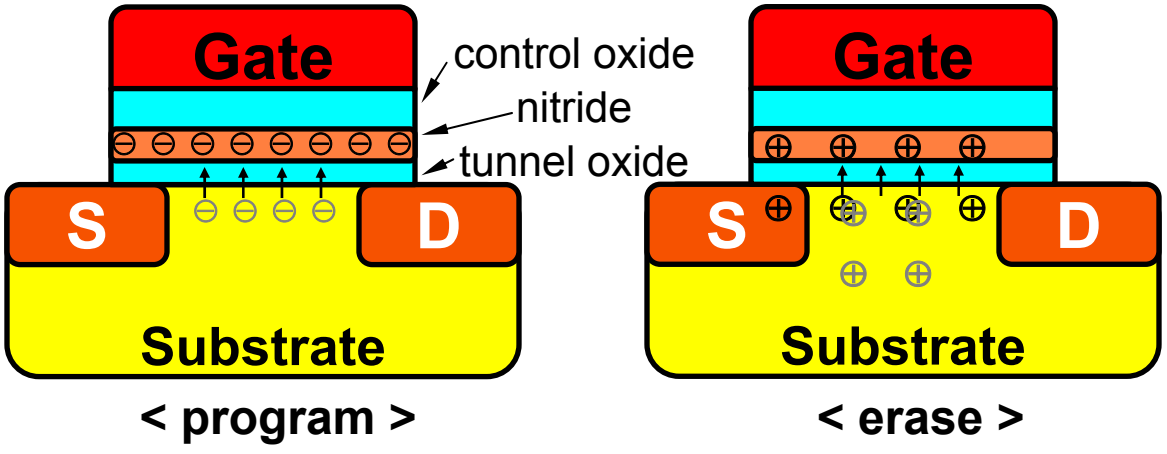
Example of Fusion Memory
(System in Package)



- Increased volume
- Complexity in assembly
- Chip-to-chip interference

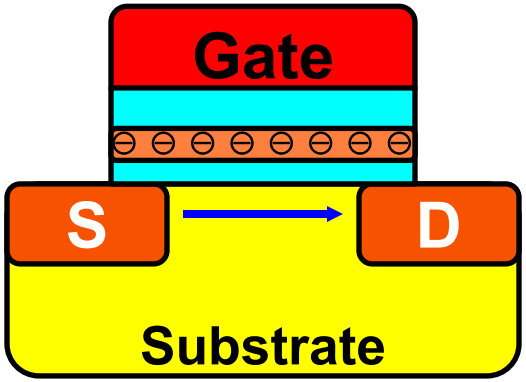
Wafer level fusion !!

Principal of SONOS Flash Memory

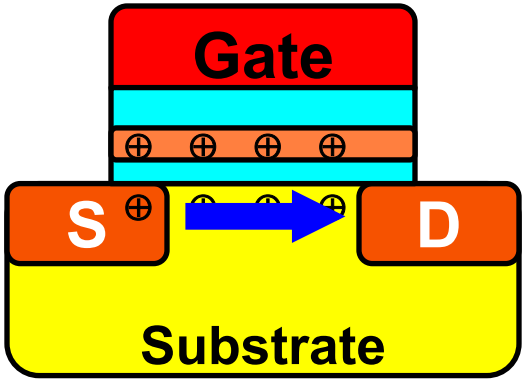


< program >

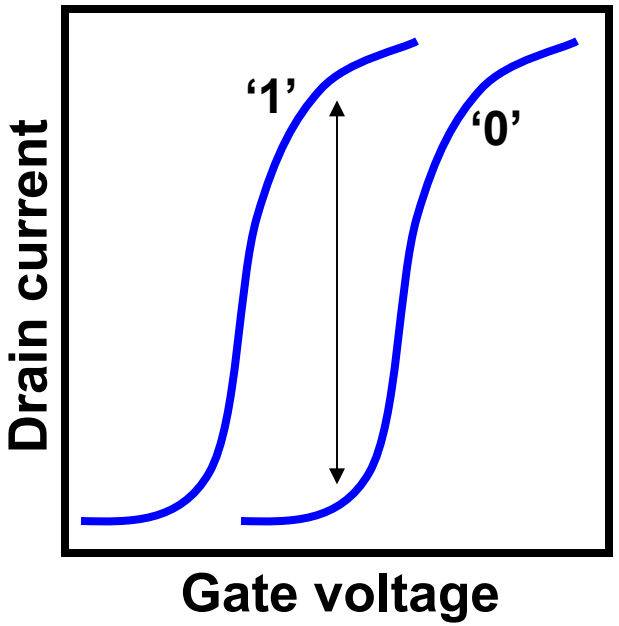
< erase >



< read '0' >



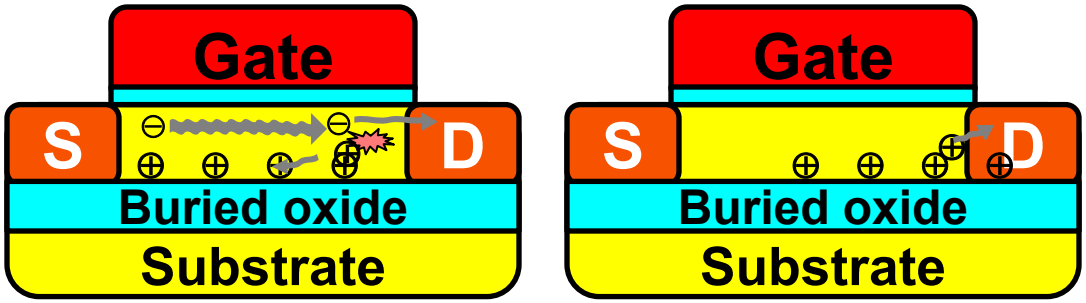
< read '1' >



Features of flash

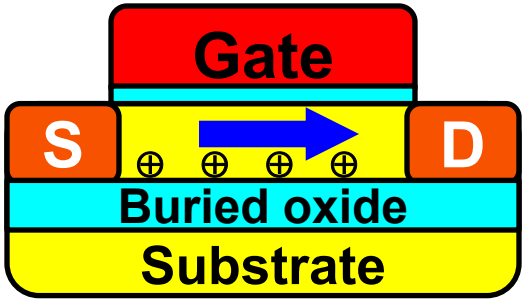
- High density ↑
- Non-volatile ↑
- Speed ↑

Principal of Capacitorless DRAM

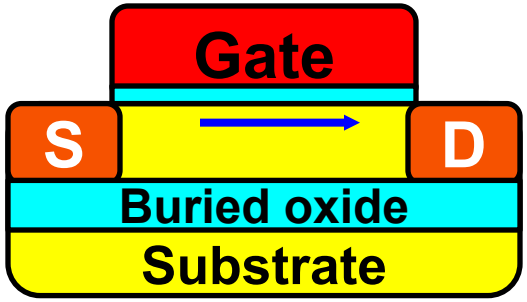


< program >

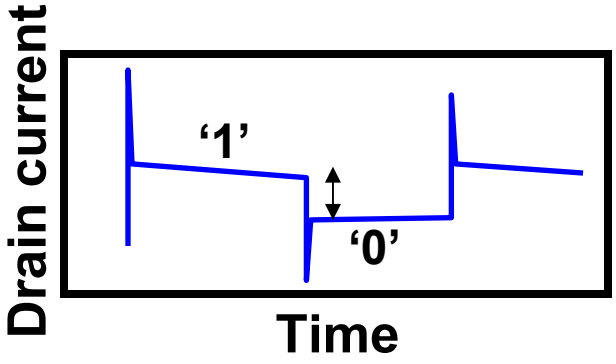
< erase >



< read '1' >



< read '0' >

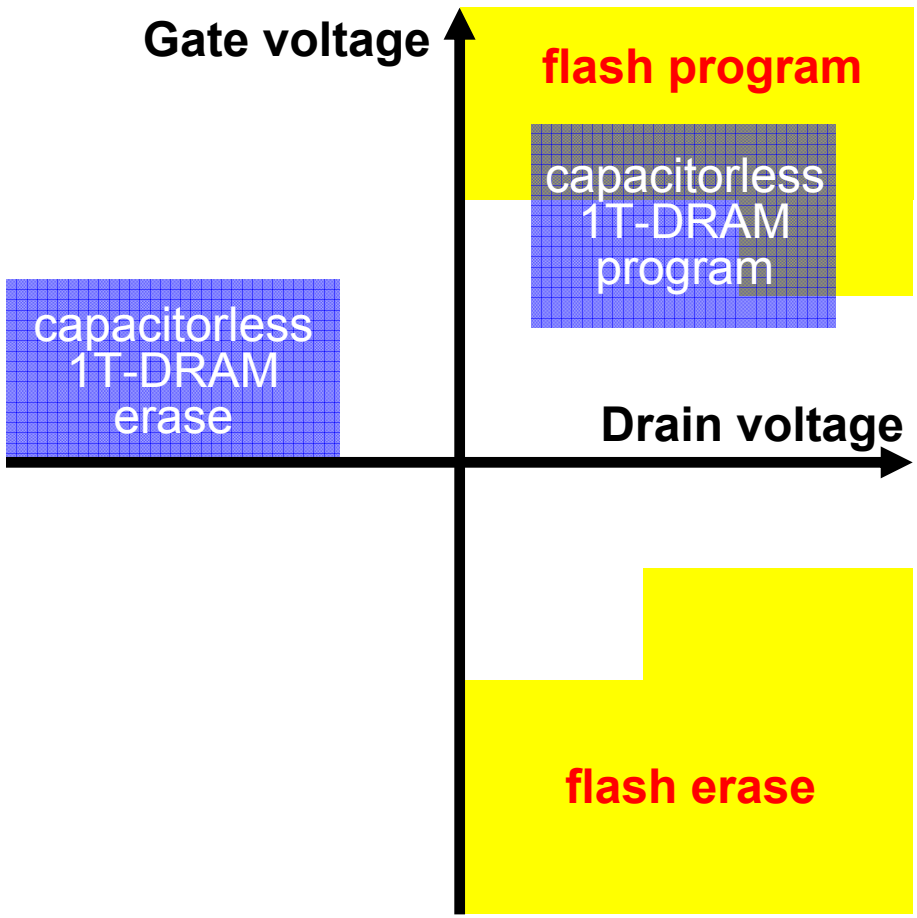


Source : IEEE spectrum Dec. 2008

Features of 1T-DRAM

- High speed ↑
- 2x denser than 1T/1C DRAM ↑
- 5x denser than SRAM ↑
- Volatile ↓

Basis of URAM Operation (1)



Flash Memory Mode

- Program : FN tunneling/HEI
- Erase : FN tunneling/HHI

(High gate & drain voltage)

Capacitorless 1T-DRAM Mode

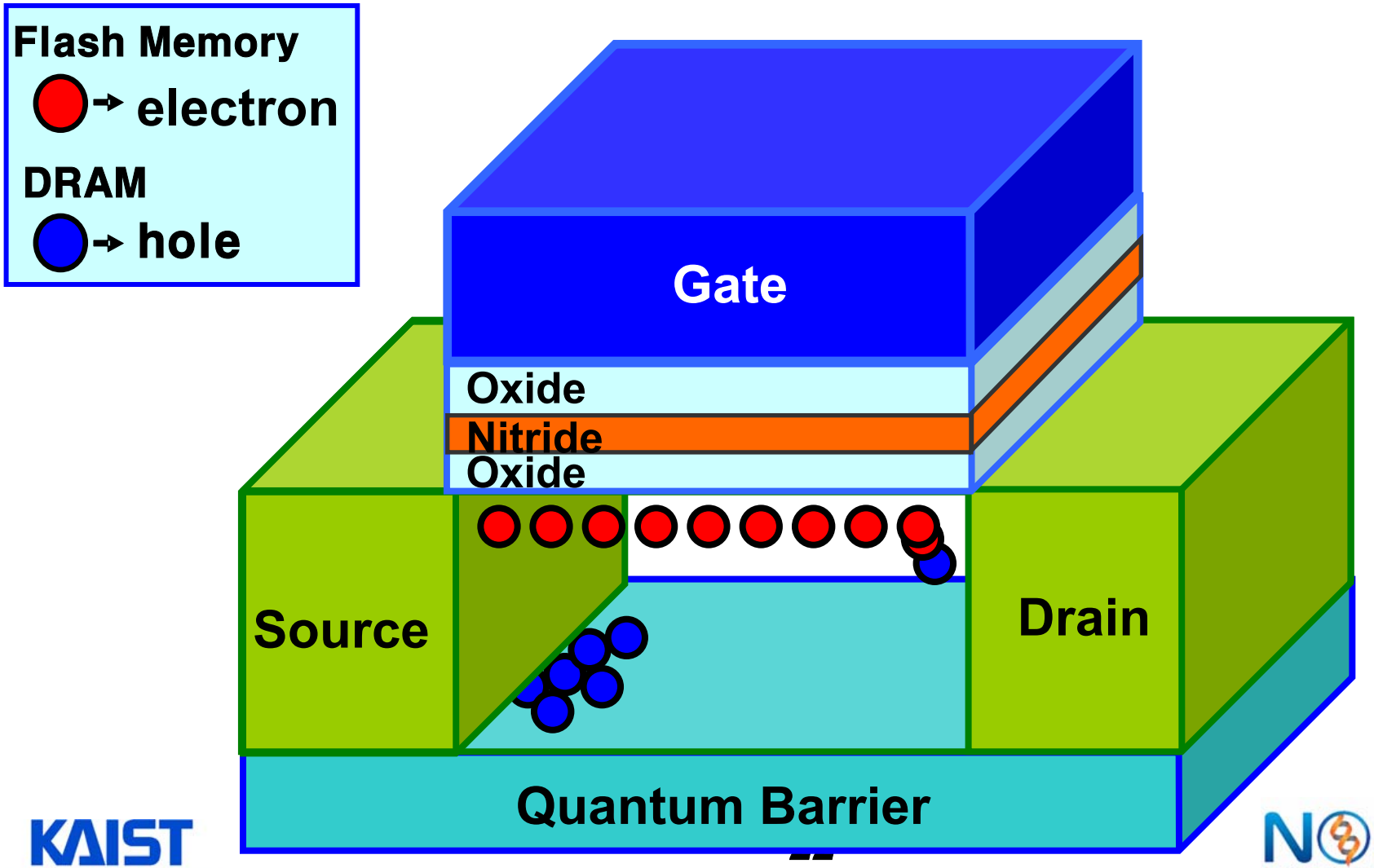
- Program : Impact ionization
- Erase : Forward junction current

(Low gate & drain voltage)

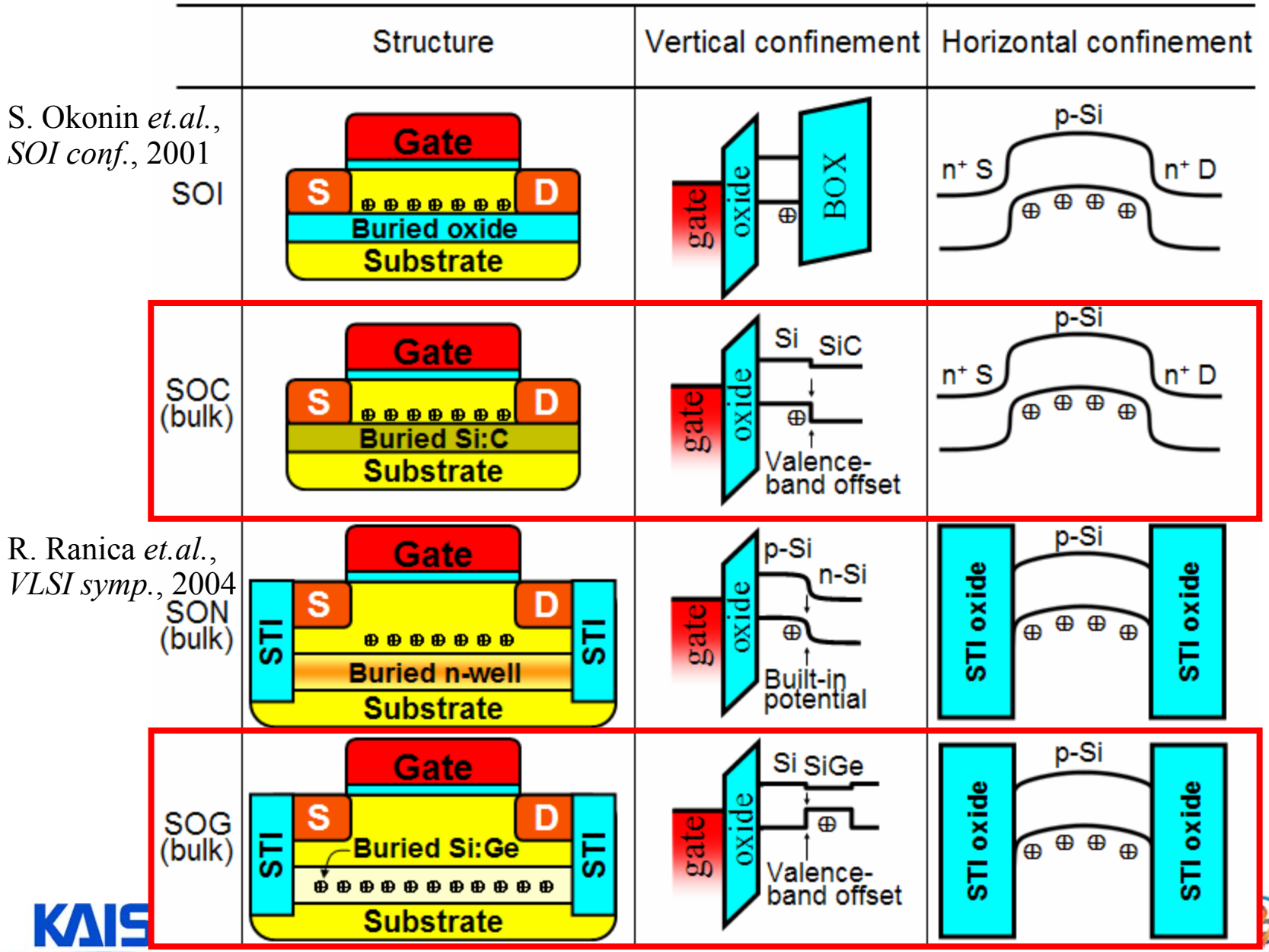
Disturbance Issue

- Periodical refresh

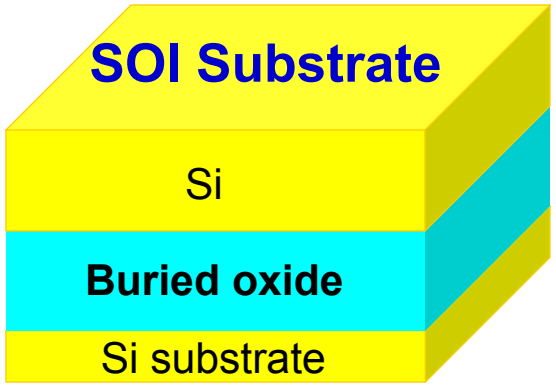
Multi-Function (URAM) Operation



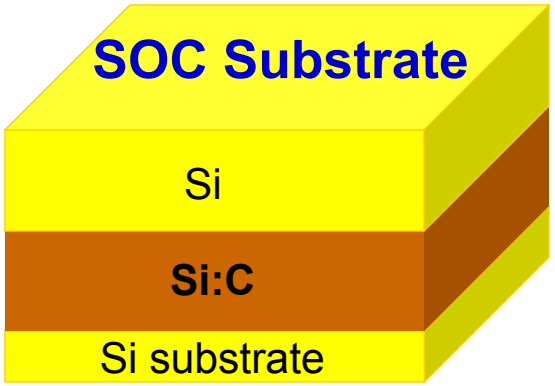
Family of URAM



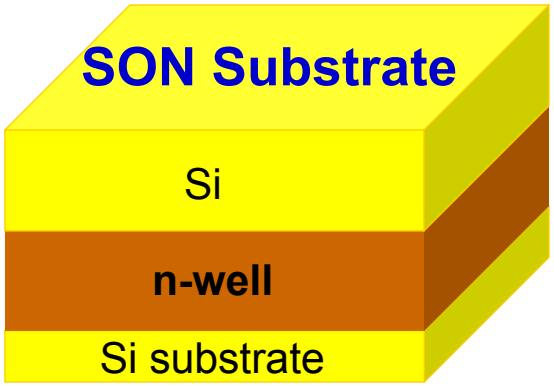
Process Flow (1)



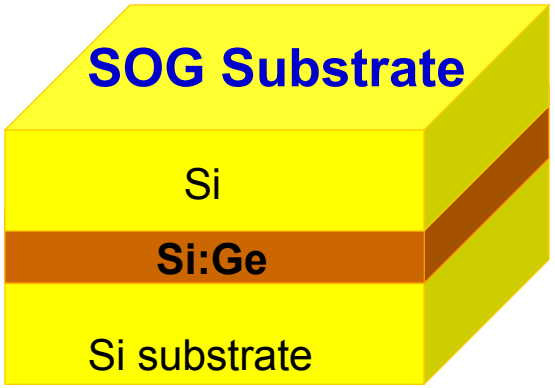
- Initial SOI substrate



- Initial bulk substrate
- Si:C epitaxial growth
- Si epitaxial growth

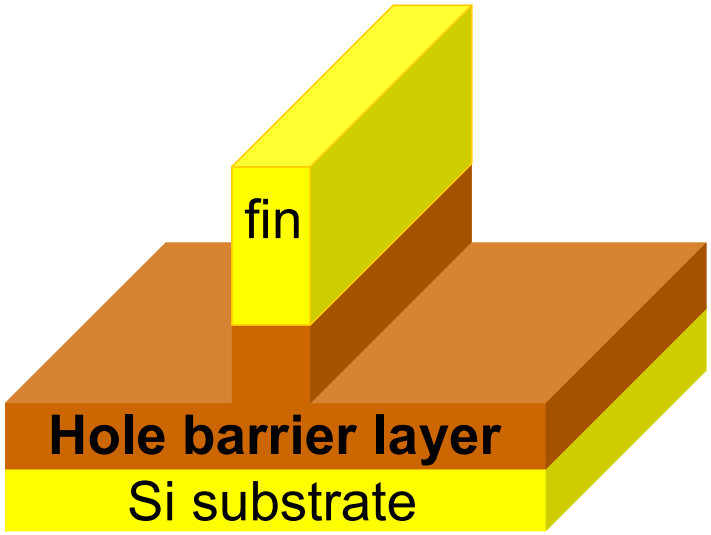


- Initial bulk substrate
- Buried n-well implantation
- p-body implantation

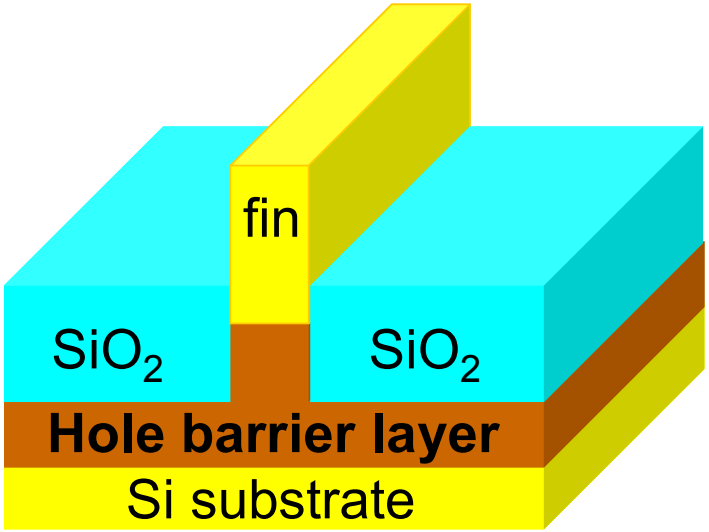


- Initial bulk substrate
- Si:Ge epitaxial growth
- Si epitaxial growth

Process Flow (2)

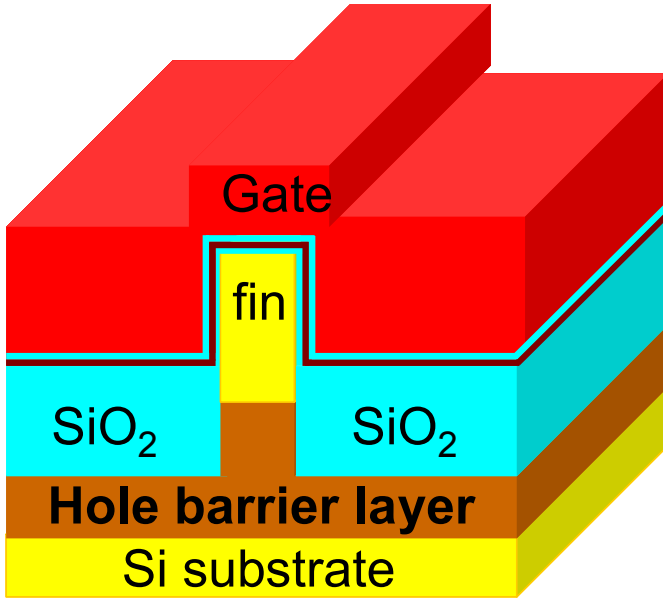


- Puntch stop implantation
- Active fin lithography
- Photoresist trimming
- Fin patterning

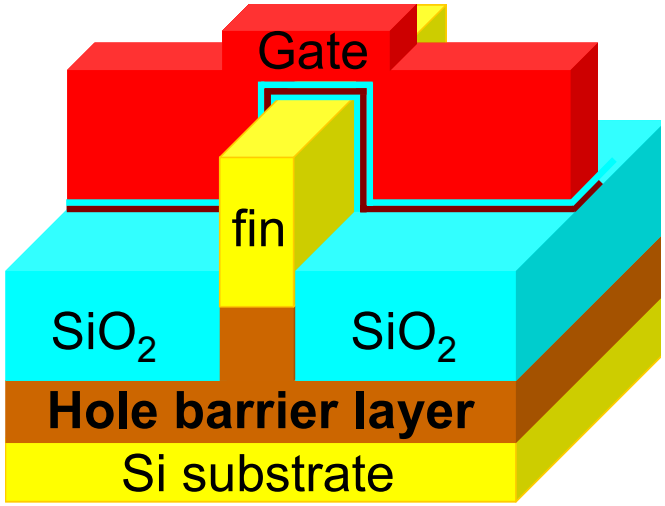


- HDP oxide deposition
- Oxide CMP
- Oxide recess formation

Process Flow (3)

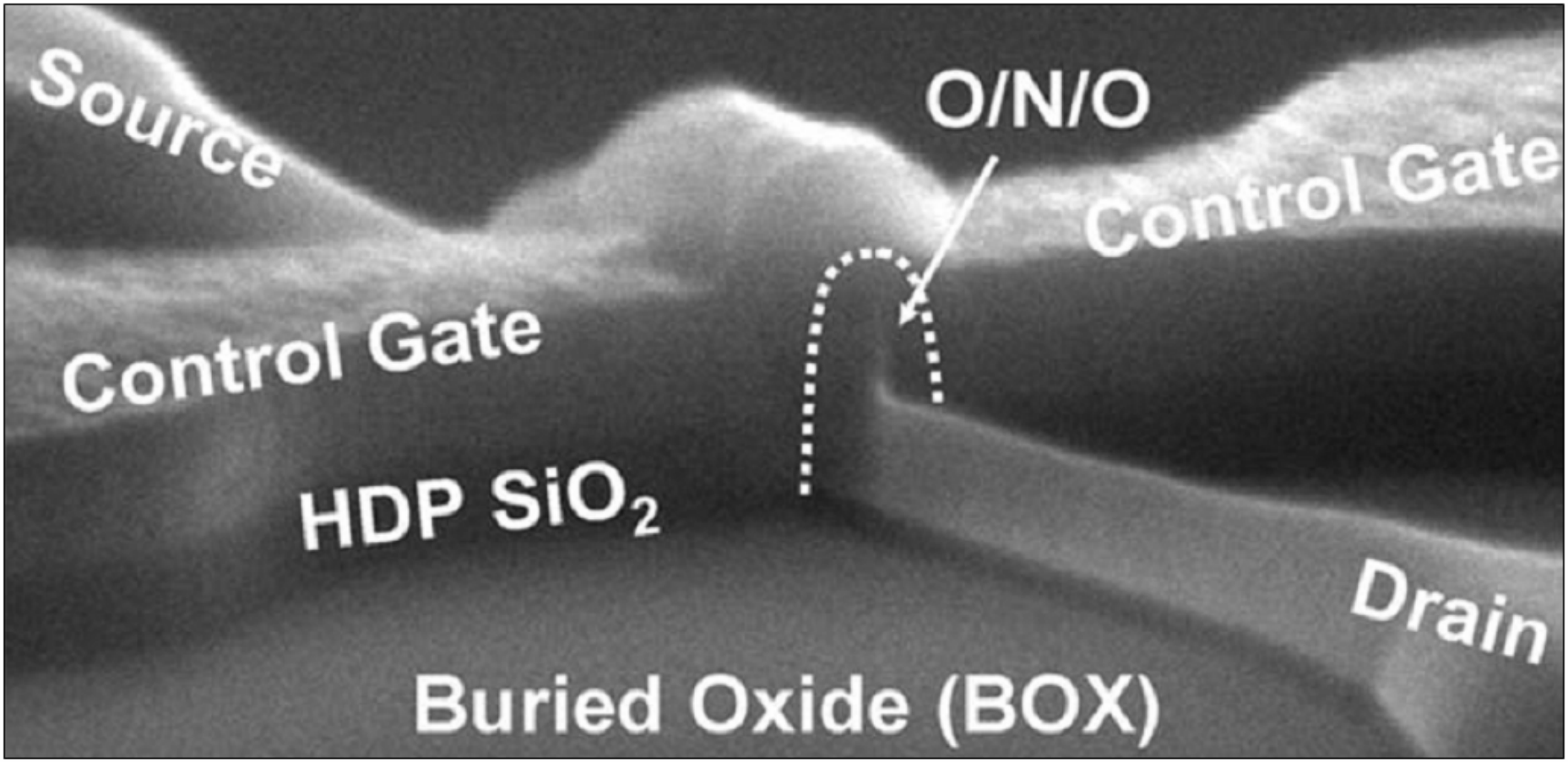


- O/N/O formation
- Poly-Si deposition

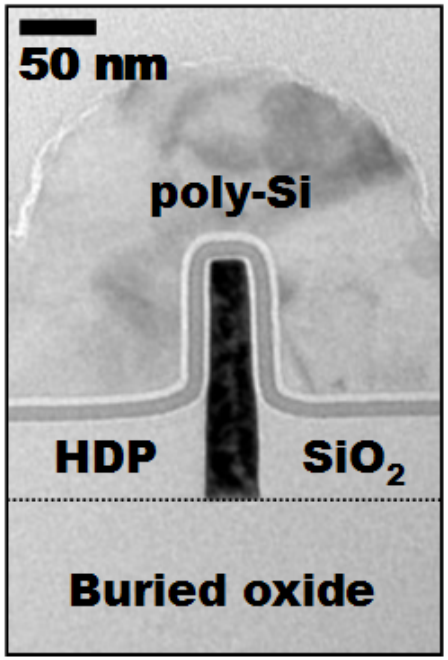


- Gate patterning
- S/D implantation
- Activation
- Forming gas annealing

URAM on SOI

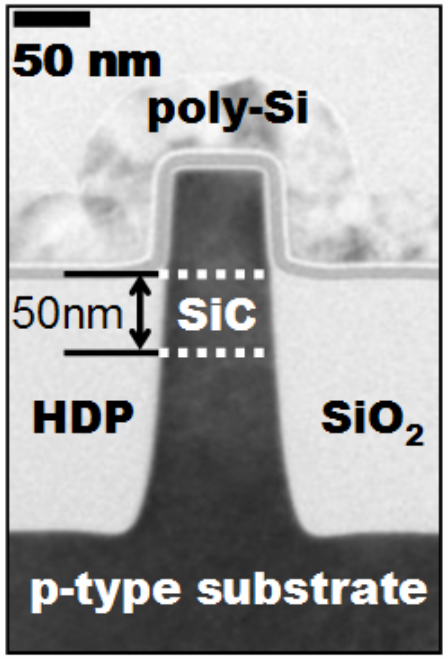

Source
O/N/O
Control Gate
Control Gate
HDP SiO_2
Drain
Buried Oxide (BOX)

Cross sectional view of URAMs



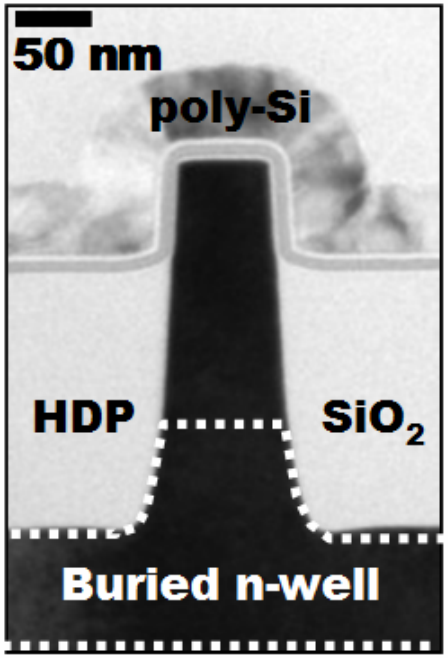
SOI

URAM
on SOI



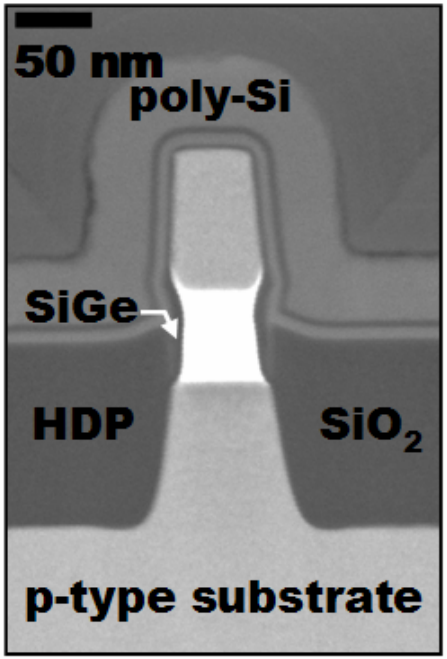
SOC

URAM
on SiC



SON

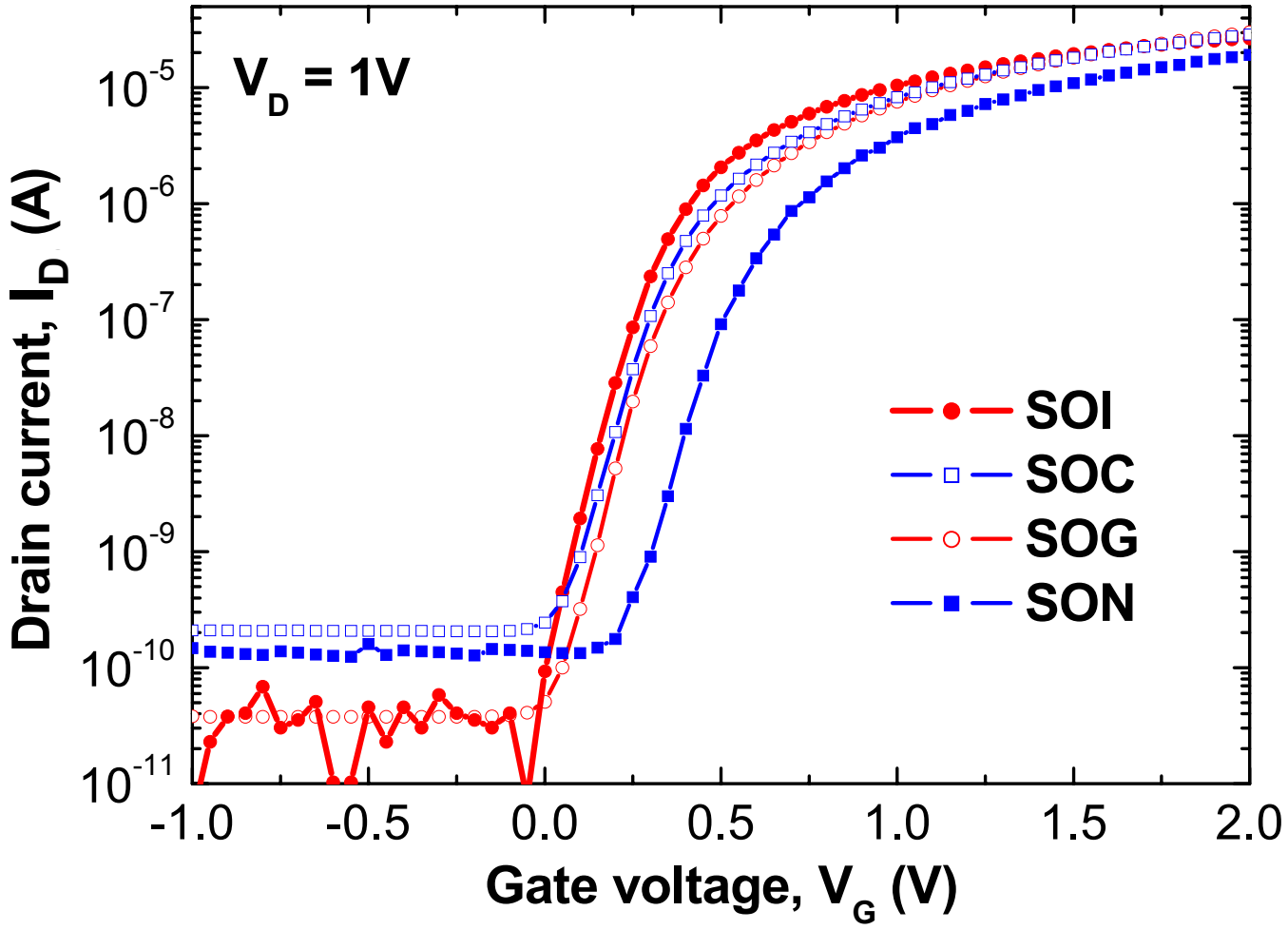
URAM
on
Buried N-well



SOG

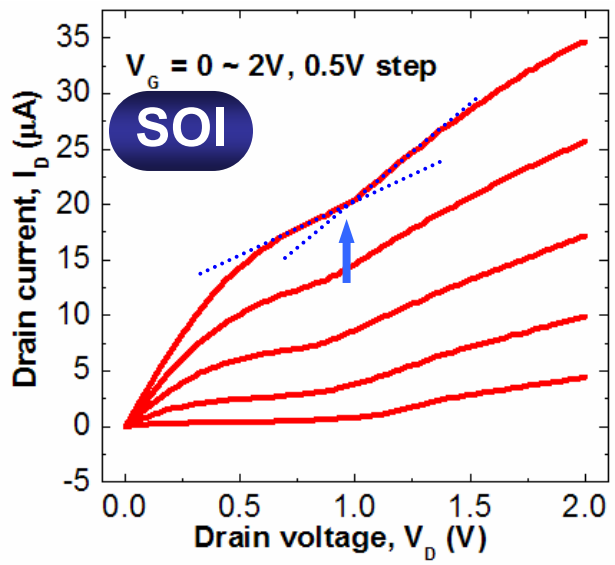
URAM
On SiGe

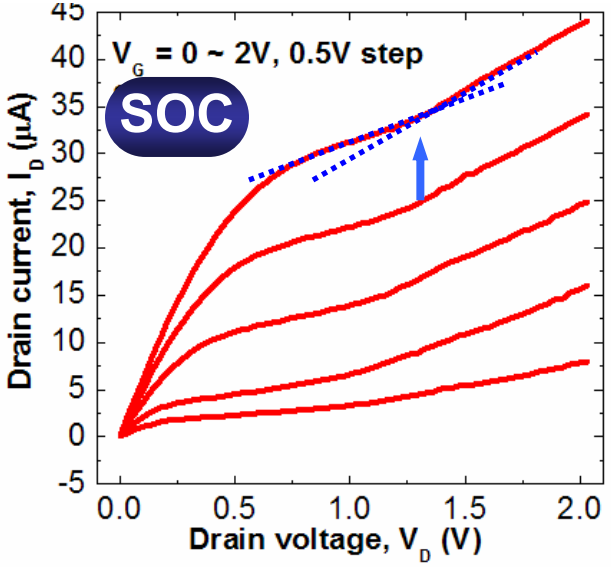
I_D-V_G Characteristics

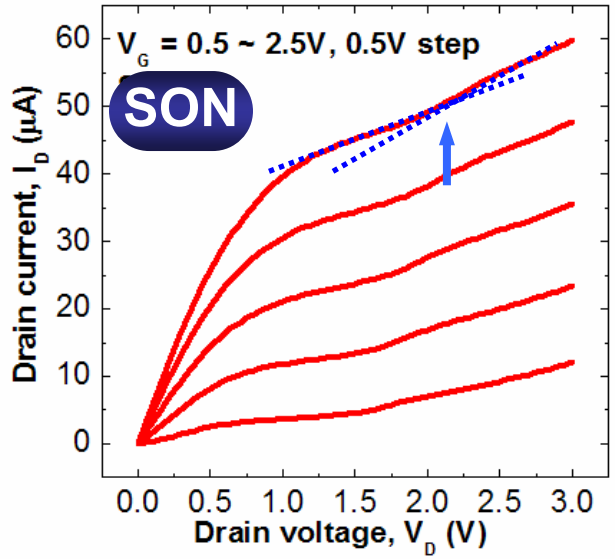


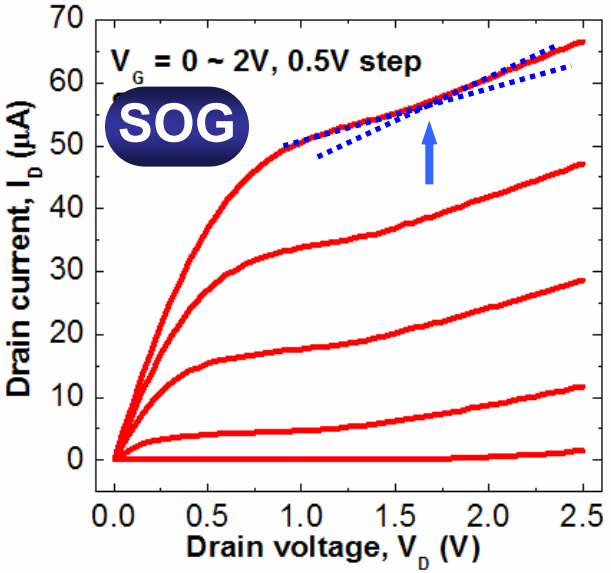
- **Superior device performances are result of the 3D nature.**

I_D-V_D Characteristics (Kink)



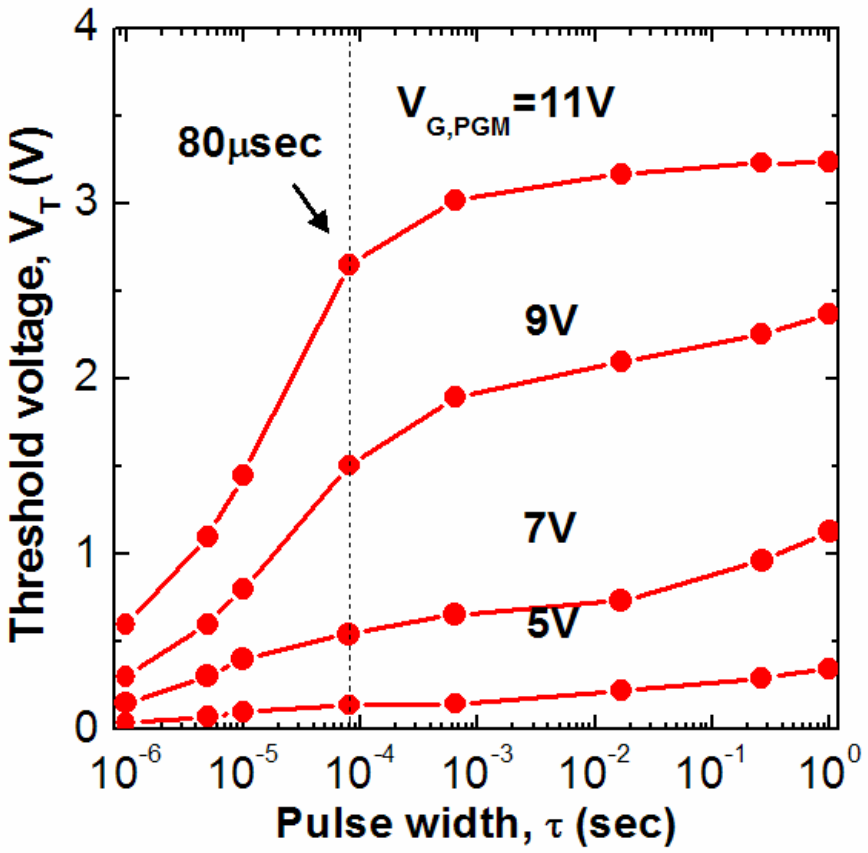




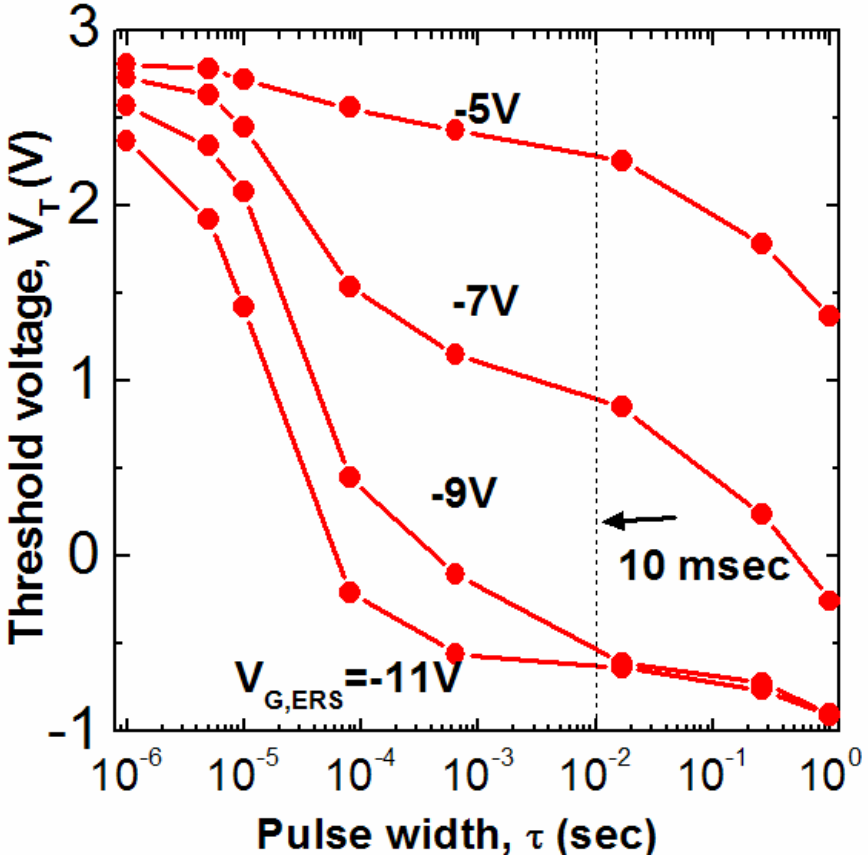


P/E in NVM

Program



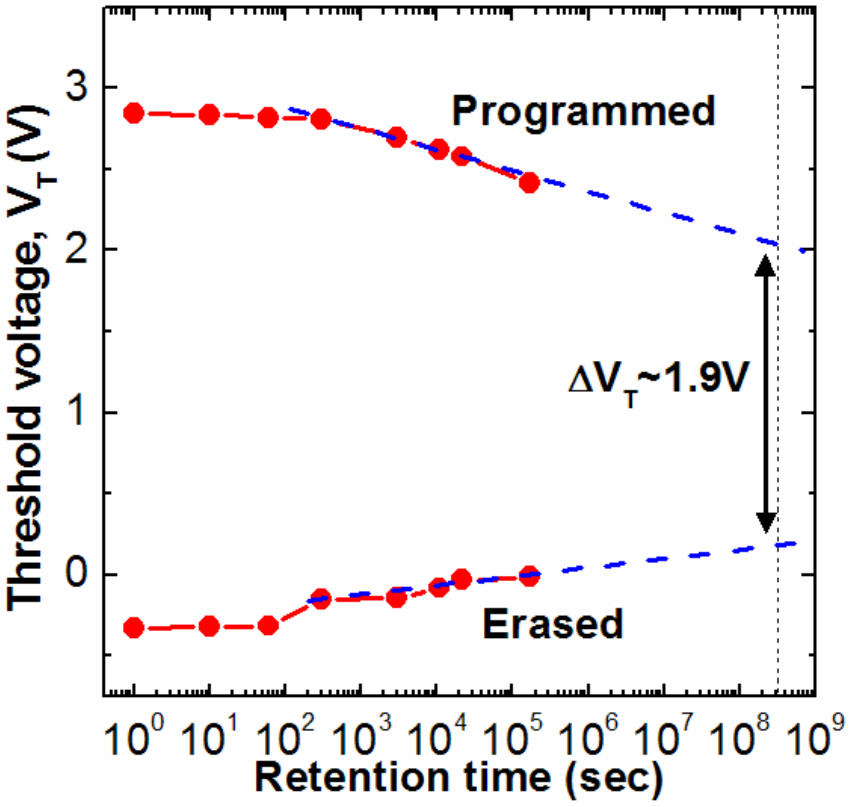
Erase



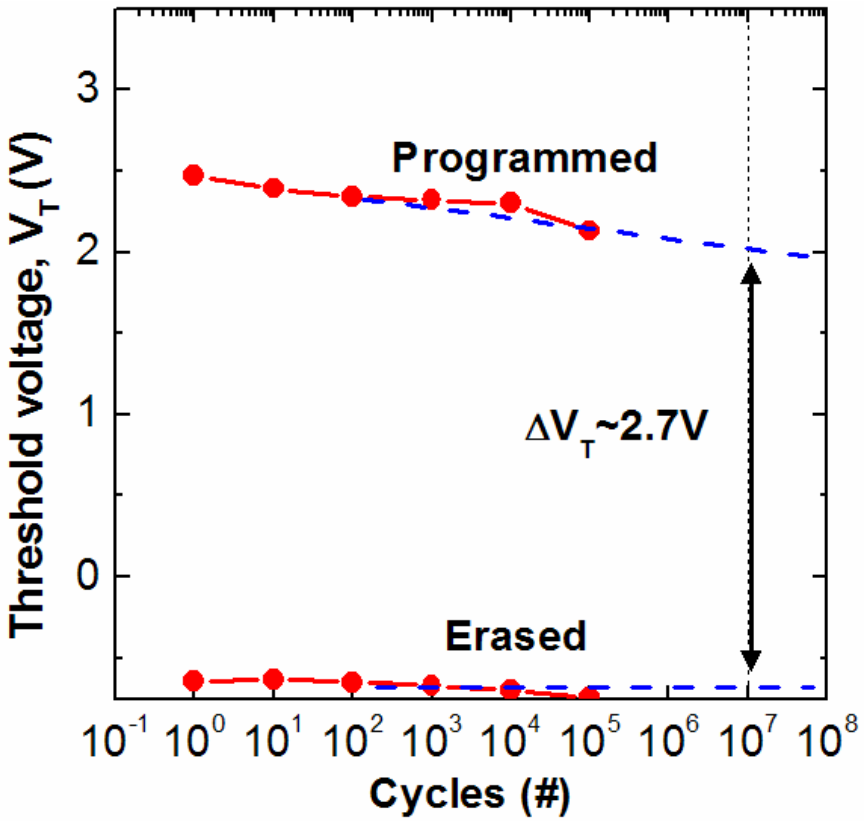
- **P/E sensing windows are acceptable.**

Reliability in NVM

Retention

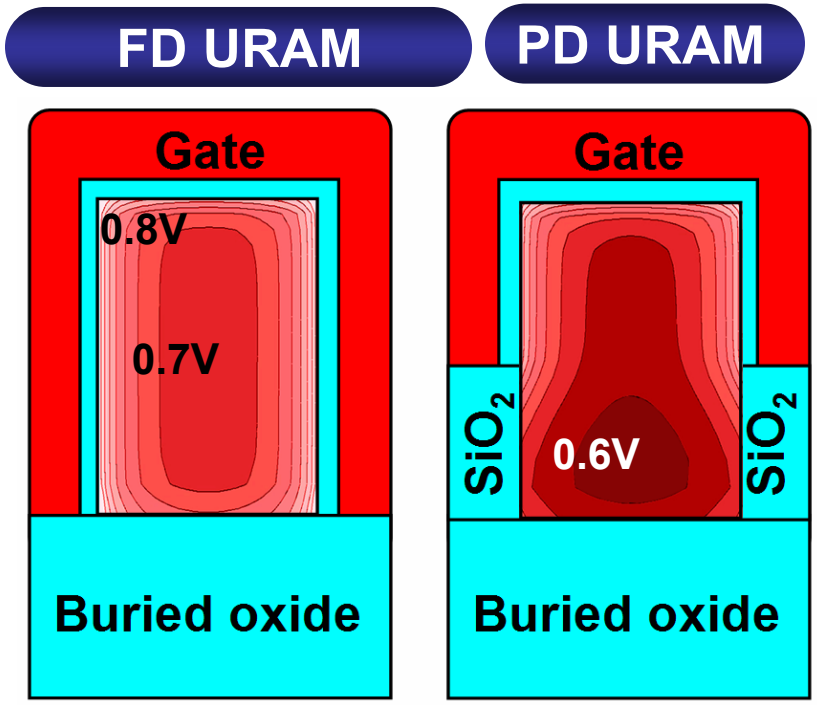


Endurance

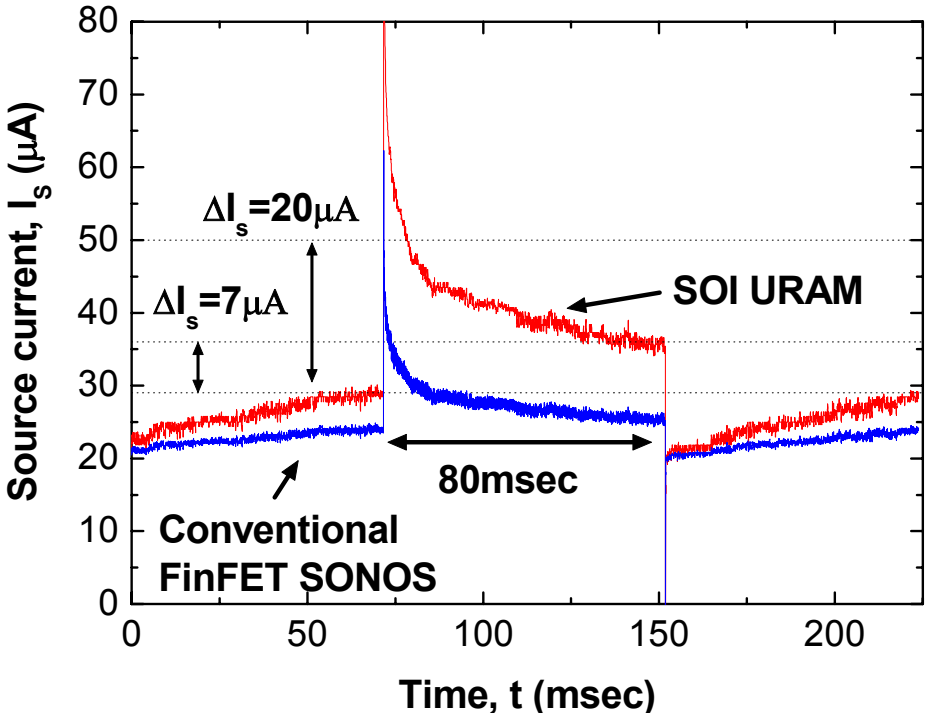


- **Data retention and endurance are acceptable.**

Capacitorless 1T-DRAM in SOI



< Potential Profile >

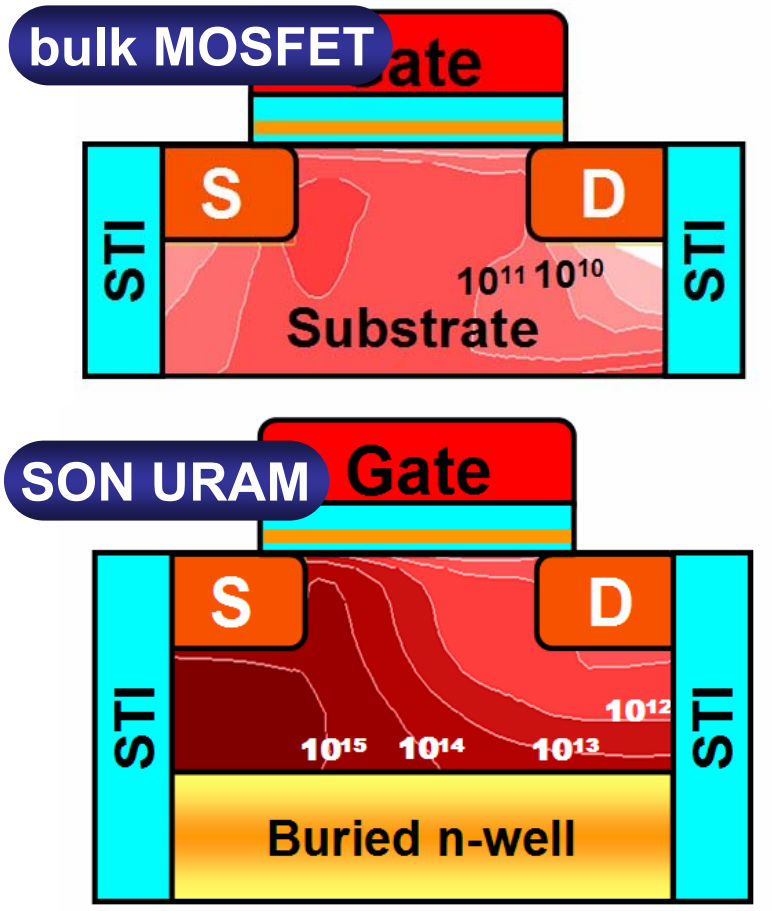


< Measurement Results >

- Proposed SOI URAM exhibits wider sensing current window.

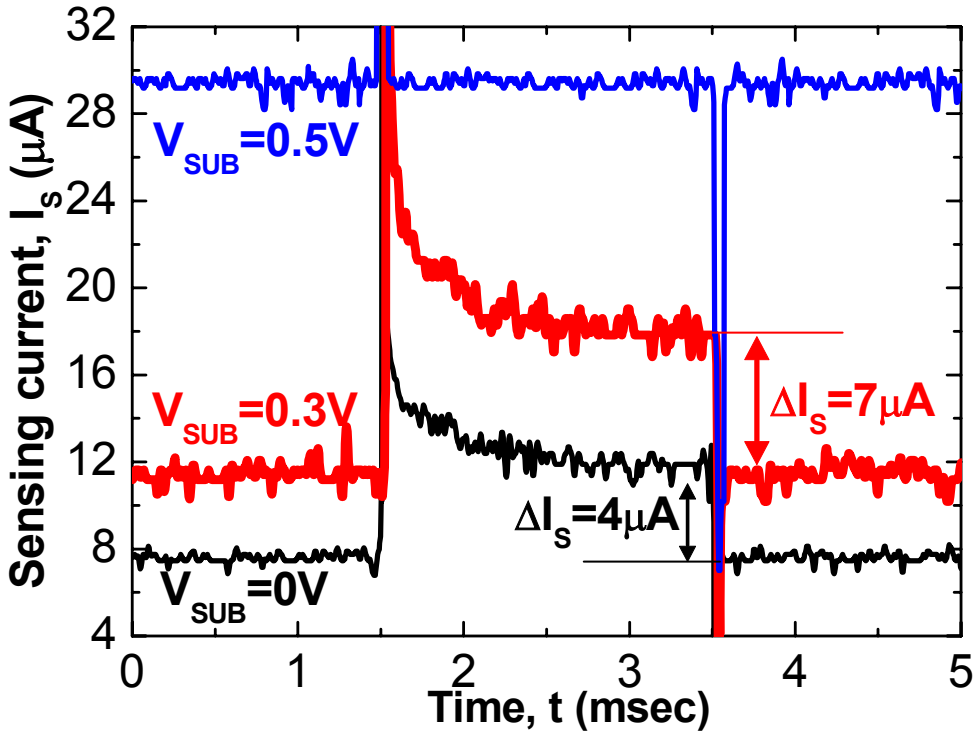
Y.-K. Choi et. al., *IEDM* 2007

Capacitorless 1T-DRAM in SON



< Excess Hole Concentration >

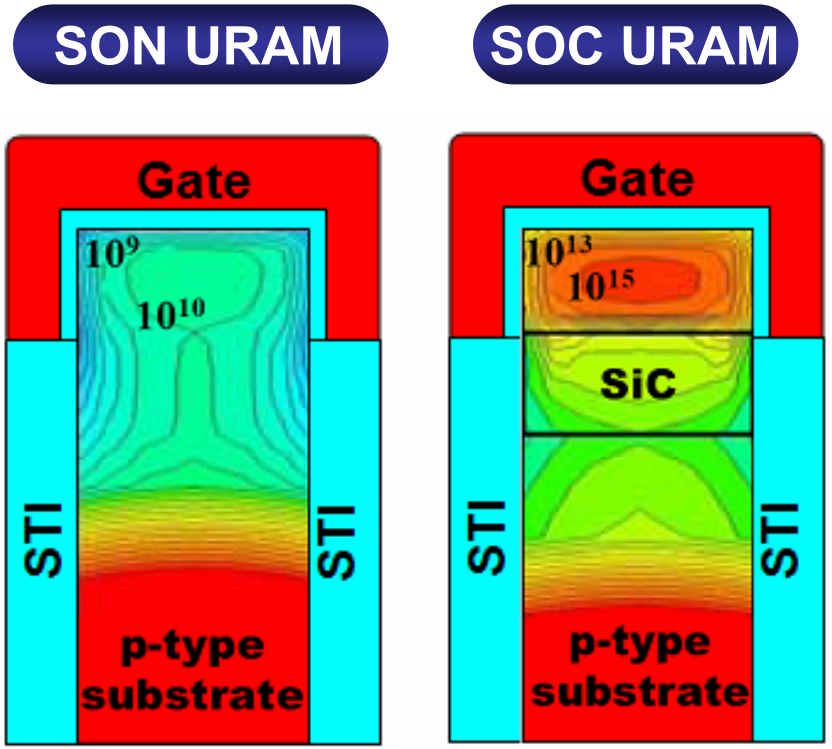
Y.-K. Choi et. al., VLSI 2008



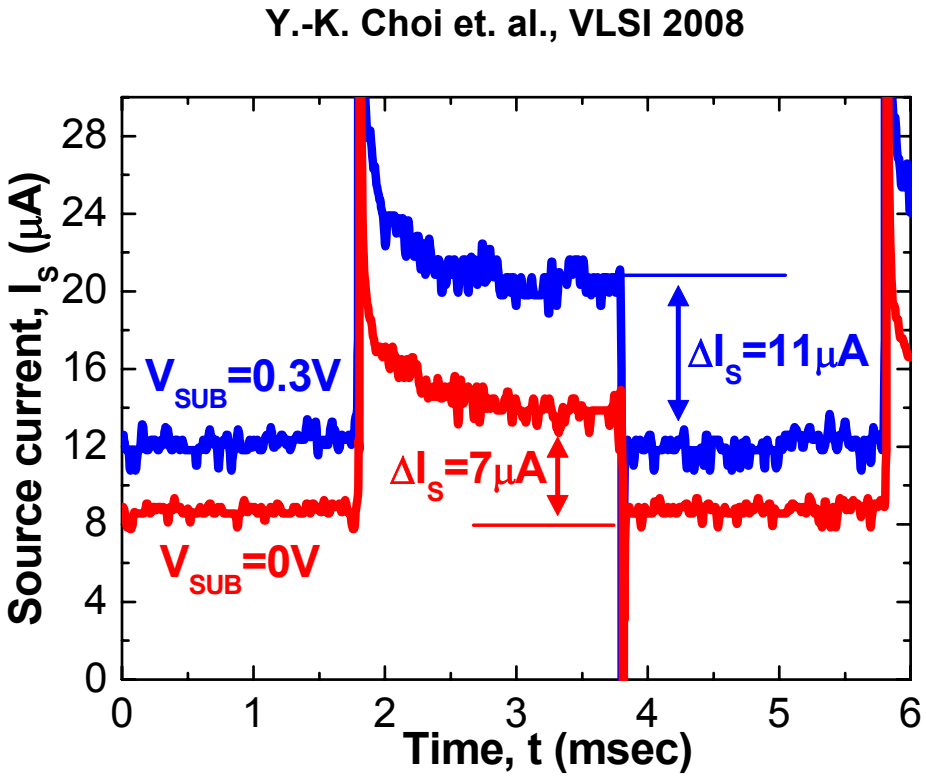
< Measurement Results >

- Capacitorless 1T-DRAM works in SON floating substrate.

Capacitorless 1T-DRAM at SOC



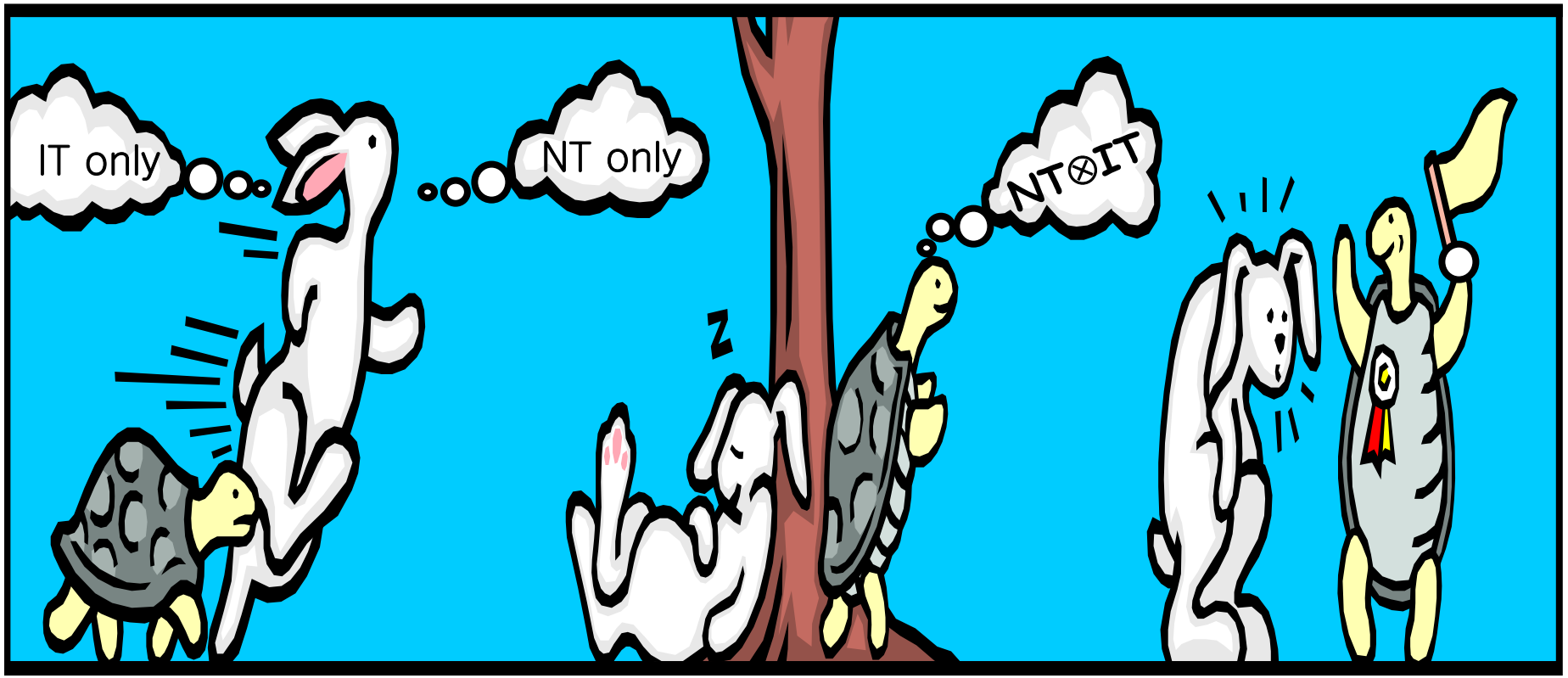
< Excess Hole Concentration >



< Measurement Results >

- Capacitorless 1T-DRAM works in SOC floating substrate.

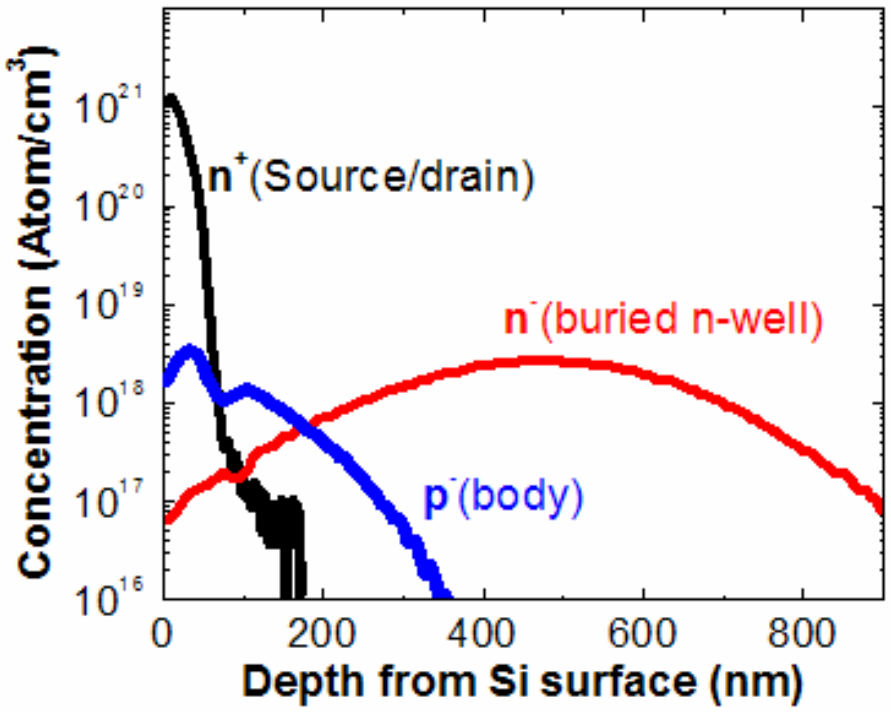
Summary



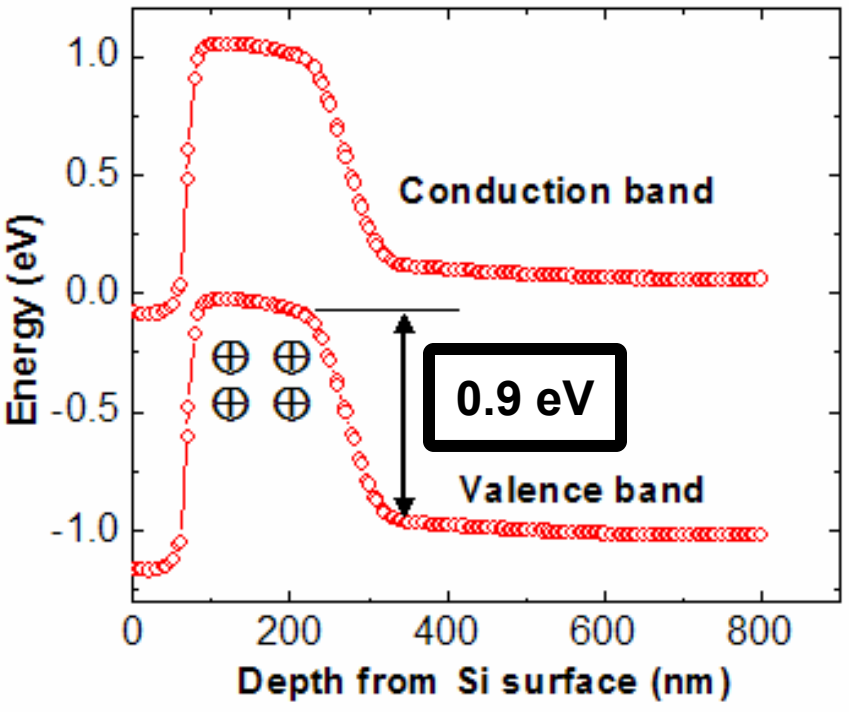
- 3nm MOSFET and 8nm non-volatile memory device were demonstrated.
  → Close to scaling limit.
- Multi-function URAM was demonstrated.
  → Continuously increased density

Built-in Potential for Buried n-well

SIMS profile of the buried n-well



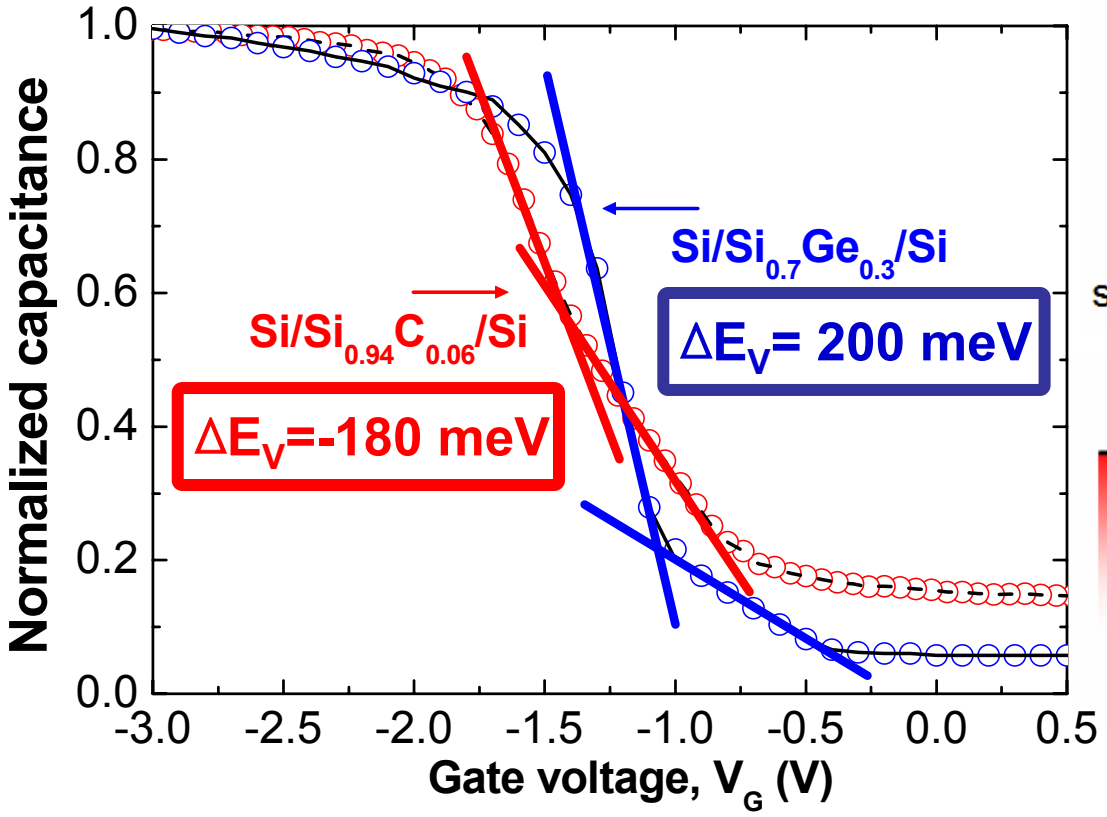
Simulation Result of Energy Band



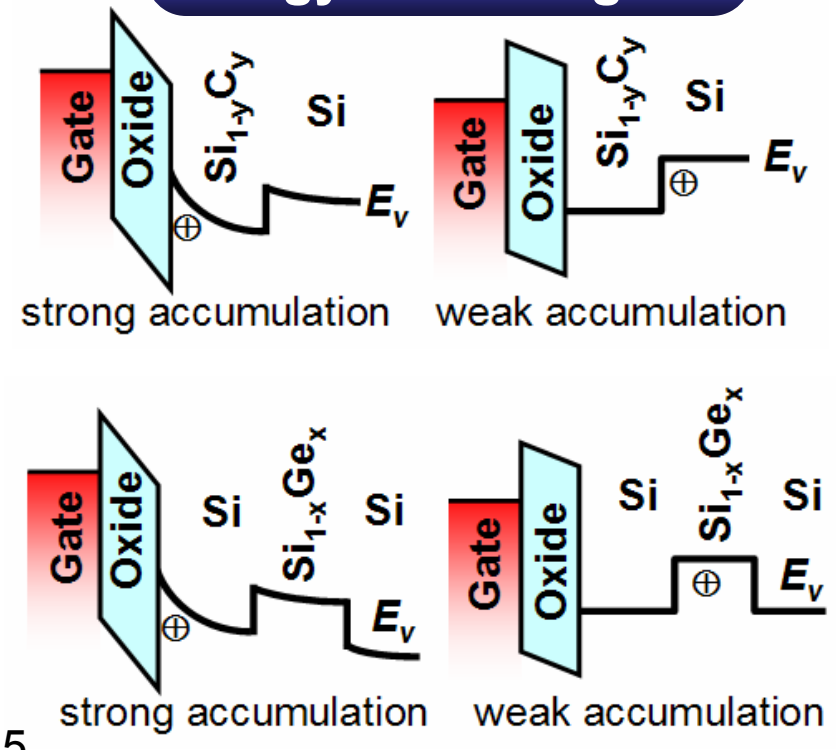
- **Built-in potential confines excess holes.**

Band-Offset for Si:C & Si:Ge (2)

C-V for Band Engineered Substrate



Energy Band Diagram

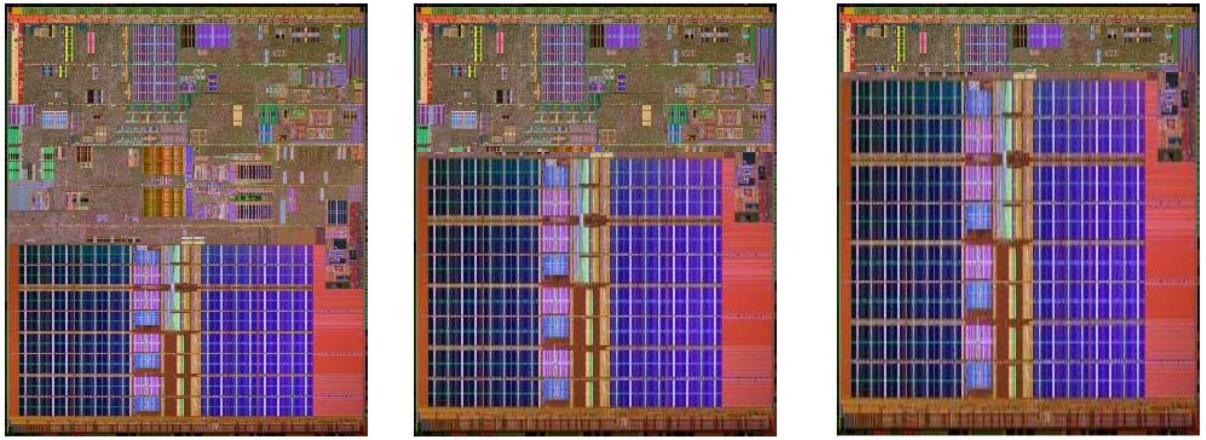


- **Double slopes appear in weak accumulation region.**

Scaling Issue
(Why capacitorless DRAM?)

μ-processor

Cache memory
SRAM ($32F^2$)

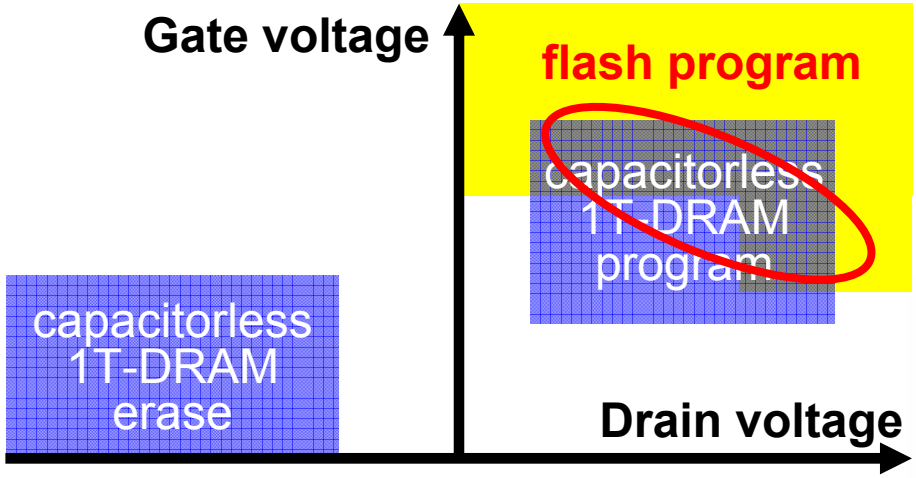


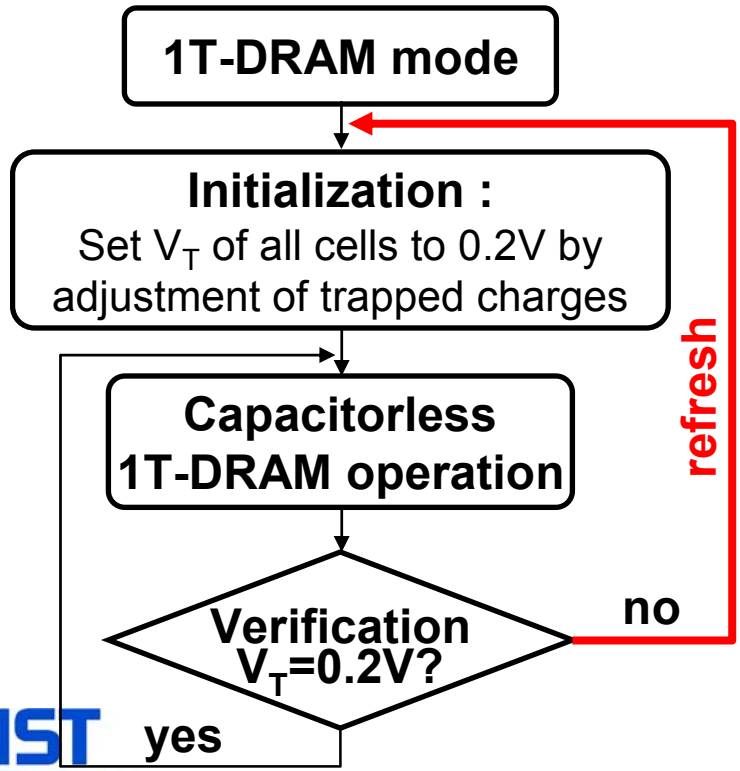
Cache portion → 50% in 2006 83% in 2008 90% in 2011

Is this memory or μ-processor ?

- Cell capacitance in DRAM > 25fF (non-scalable)
  Cell area (~$8F^2$) is continuously reduced.
- Capacitorless DRAM is a promising candidate for embedded memory.

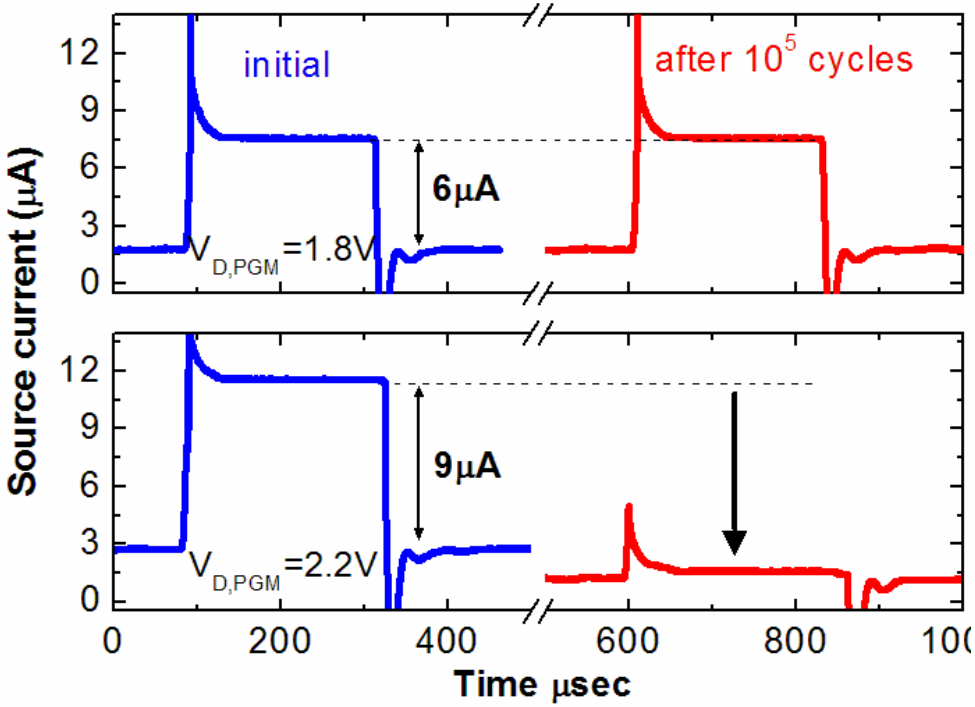
Soft-Program Issue





Disturbance Issue

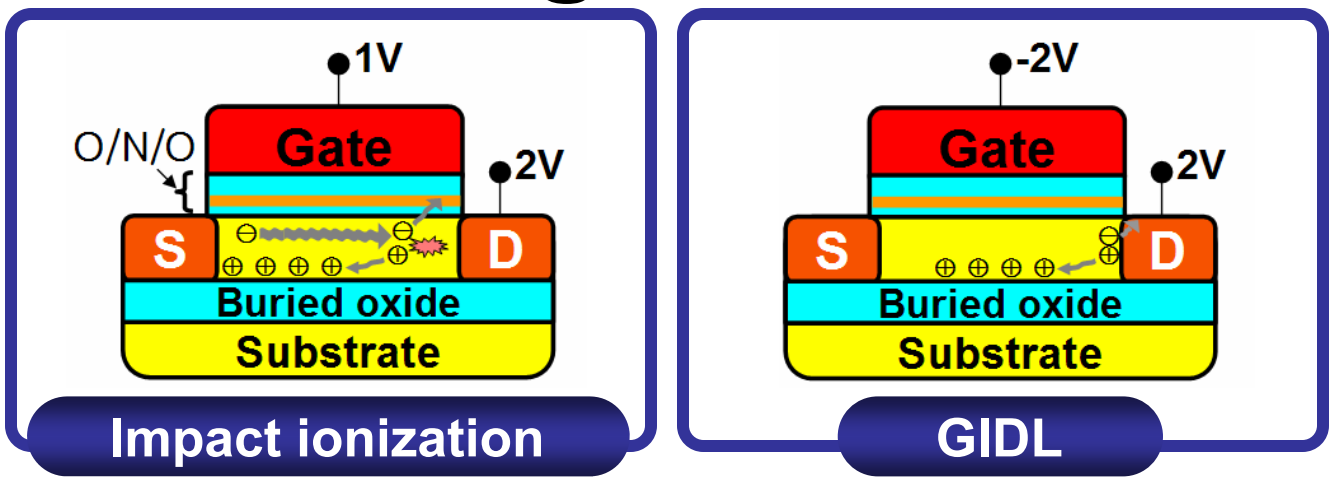
- Periodical refresh

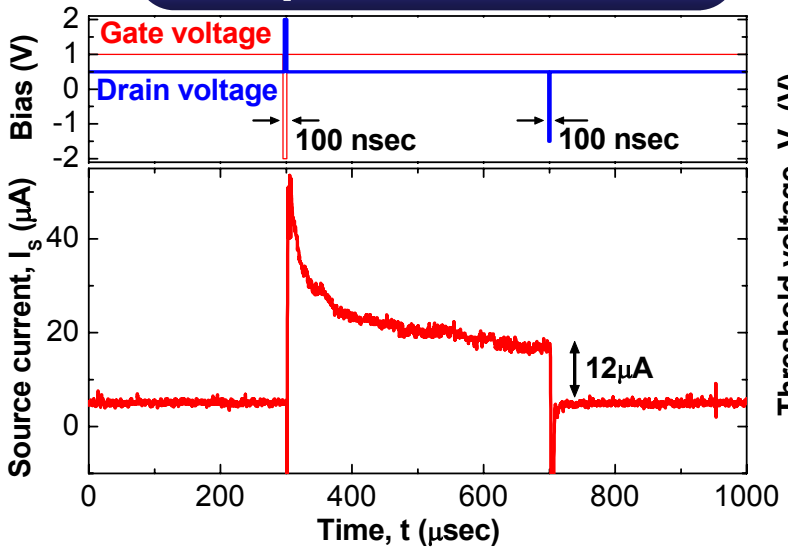


KAIST

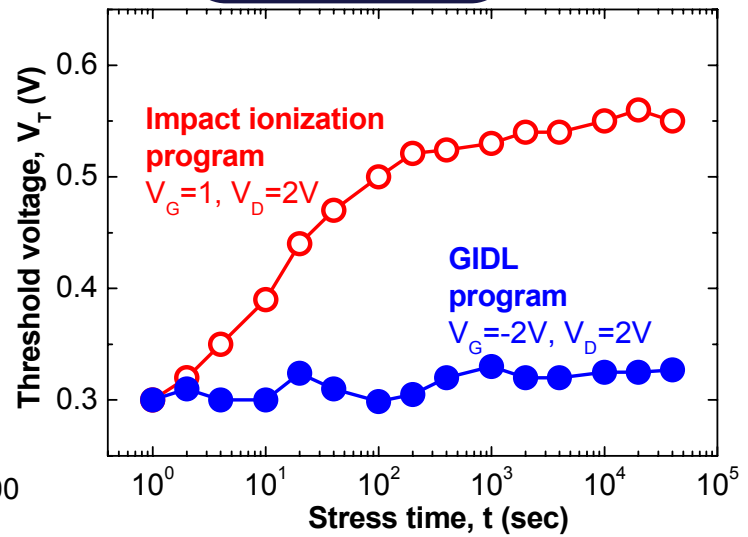
NOBEL Nano-Oriented Bio-Electronics Lab

GIDL Program Method





< 1T-DRAM Measurement >

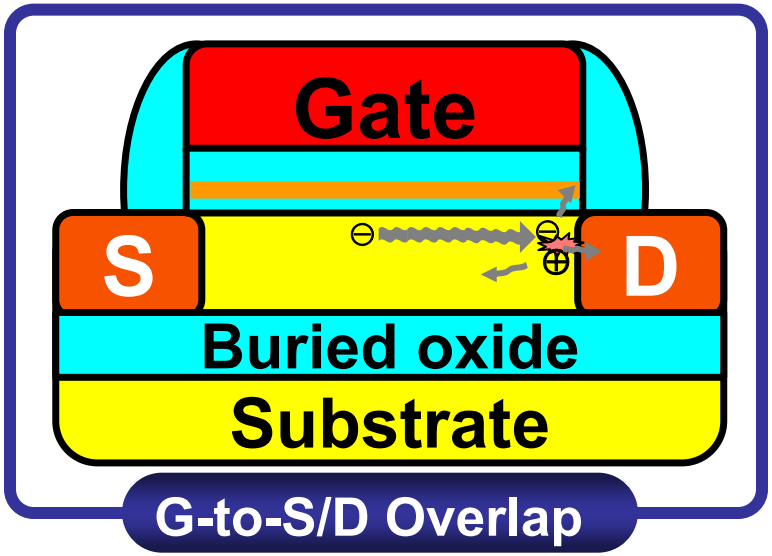


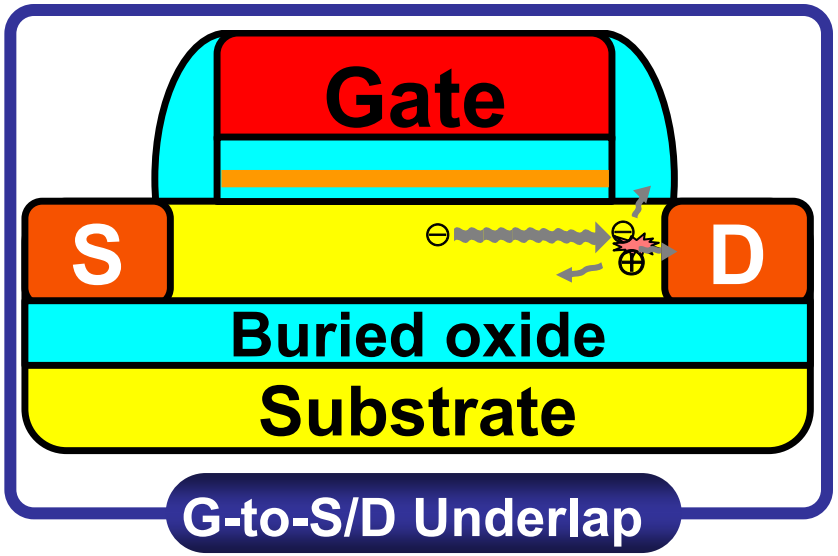
< Soft-program test >

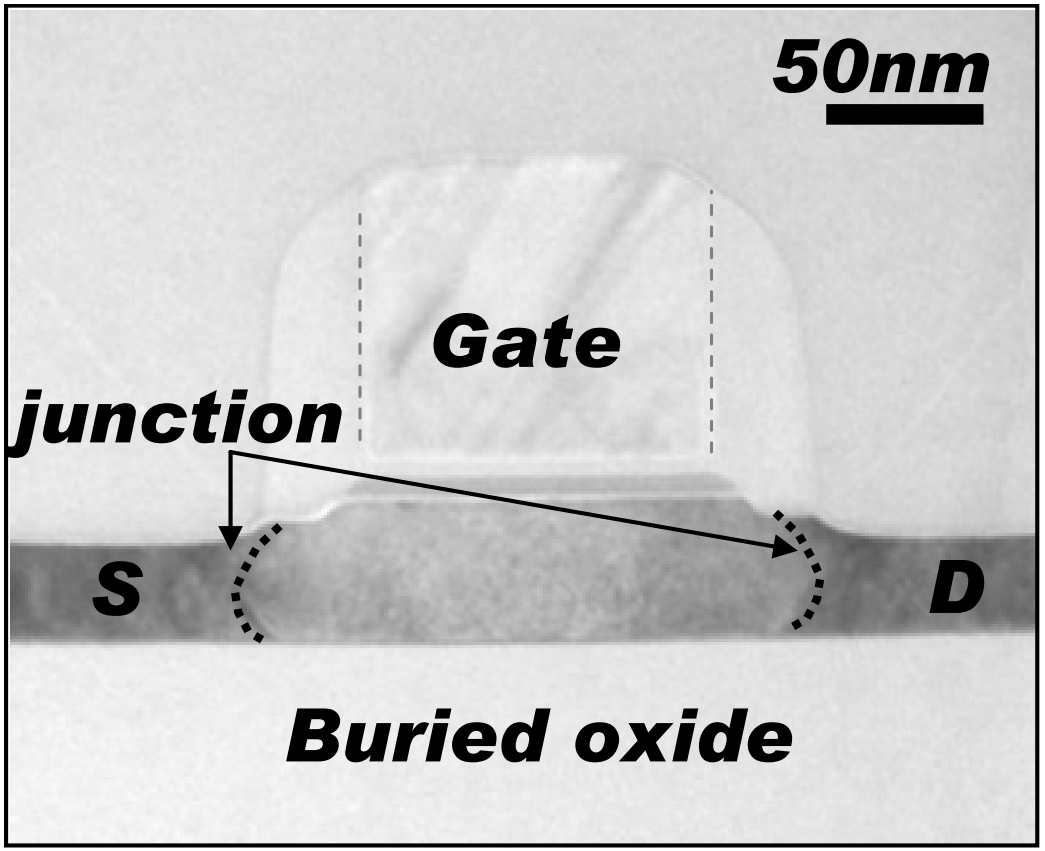
- GIDL program method mitigates soft-programming.

[J.-W. Han *et. al.*, EDL, Apr. 2009]

G-to-S/D Underlap Structure

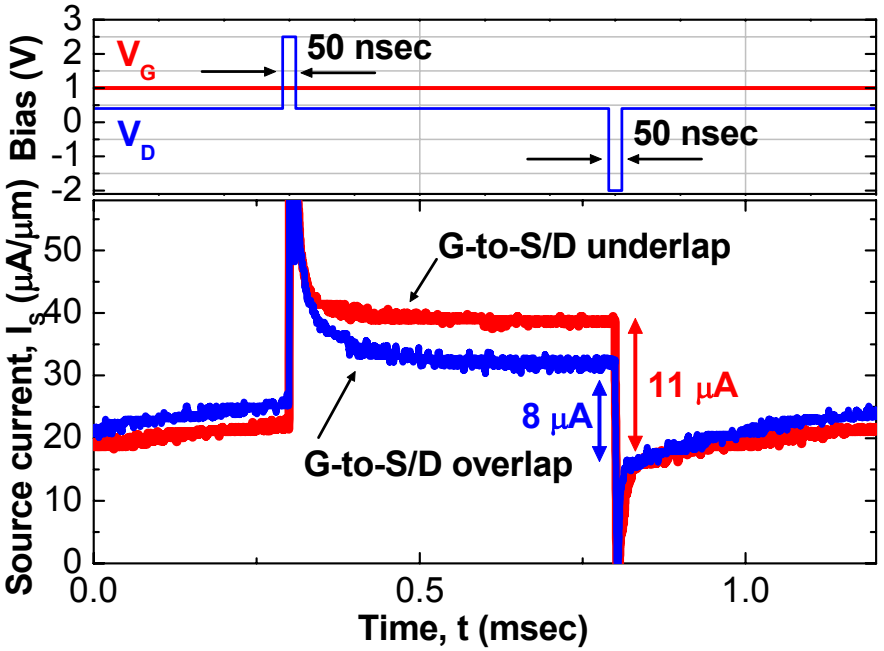




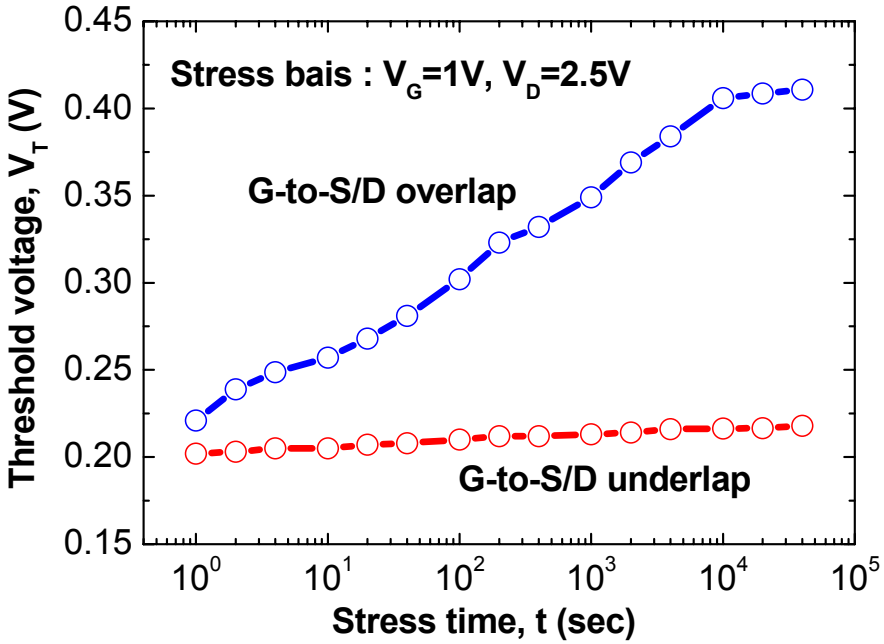


[J.-W. Han *et. al.*, EDL, May 2009]

G-to-S/D Underlap Structure



< 1T-DRAM Measurement >

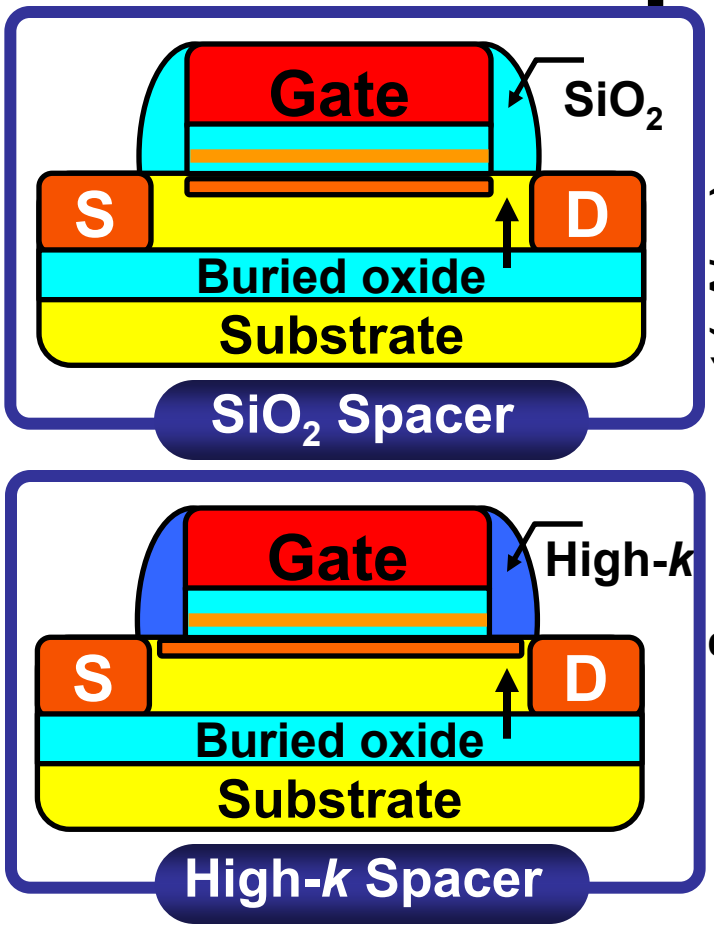


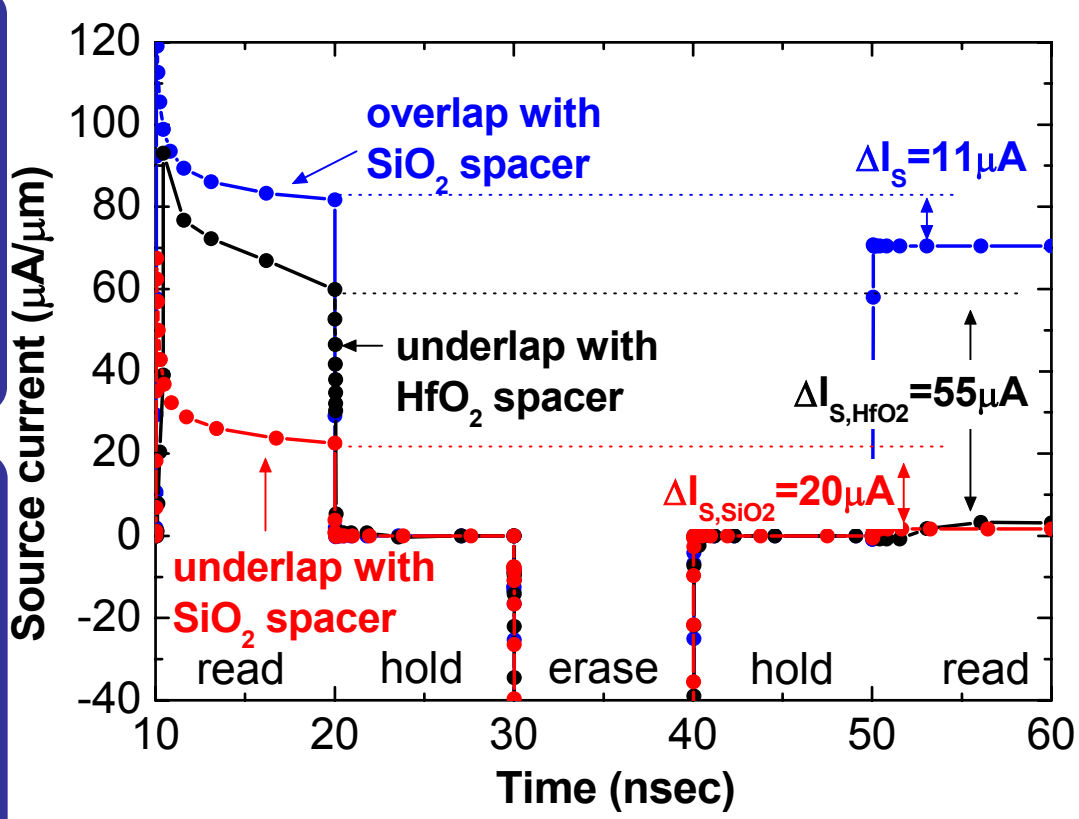
< Soft-program test >

- G-to-S/D underlap structure mitigates soft-programming.

[J.-W. Han *et. al.*, EDL, May 2009]

Issue and Solution of G-to-S/D Underlap Device Structure





< Simulation Results >

- High-*k* spacer countervails the parasitic series resistance of the G-to-S/D underlap.

[J.-W. Han *et. al.*, EDL, May 2009]