Information Processing in the Presence of Variability and Defects of Nanoscale

Sandip Tiwari
st222@cornell.edu

Today's information processing systems are designed to be totally predictable, reproducible, and are designed hierarchically to be manageable.

Plenty of room for inefficiencies. What can we do within this model?

Are there other opportunities at the hardware - software wall?

Random and non-random variability and defects

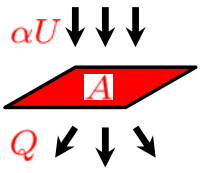
Complexity of scales connecting nanoscale to terascale

Cornell University

Acknowledgements: Arvind Kumar, Ravi Nair, Chris Liu, Ravishankar Sundararaman, Joshua Rubin, Howard Davidson, Jae Yoon Kim, Wei Min Chan, Moon Kyung Kim …

Power and Heat

Rapid changes in fields -> excess charged particle energy loss to medium -> heat



time constant of energy consuming operation

$$\tau = \frac{\alpha U}{QA}$$

- α: activity factor
- U: energy per operation
- A: x-section area of heat removal
- Q: density of heat removal

1D Heat Spreading: Array regions

$Q = 10^2\ W/cm^2$
$\Rightarrow \tau = 5\ ns$

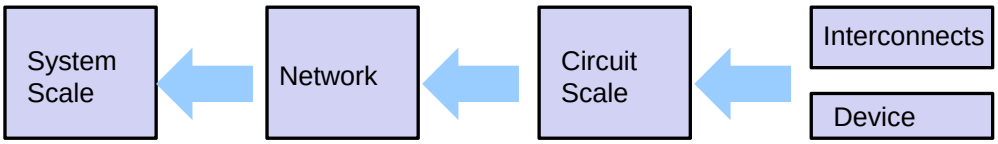
3D Heat Spreading: Logic regions

$Q = 10^5\ W/cm^2$
$\Rightarrow \tau = 5\ ps$

10 nm λ ⟺ $7.5 \times 10^{12}\ \lambda^2$ in 1 inch^2 => 10^{12} devices/chip

S. Tiwari et al., IEEE NMDC (2006)

Hierarchy and Data Movement: Energy



You have heard plenty about the device issues here in the morning
-- The corollary of the discussion is power
-- this is also true for communications

A 16 nm processor!

Source: W. Dally (2008)

RoadRunner Supercomputer

1 Petaflops
6562 Dual-core AMD Opteron chips
12240 Cell chips (used in Sony Playstation 3)
~15 Tera transistors
98 Terabytes of memory
~800 Terabits
278 racks
2.35 MW of power

Element	Energy	Units
32b integer op	0.35	pJ
64b floating op	7	pJ
Instruction exec	210	pJ
32b 16K RAM read	11	pJ
32b across 1mm	5	pJ
32b across 20mm	100	pJ
32b off chip	320	pJ

Moving data is expensive; LVDS mitigates only partly

Computation Problems

- Most computation problems are inexact
  - Speech and Video's
  - Recognition
  - Machine learning
  - Data compression
  - …
  - Decision making
    - Inexact inputs
    - Inexact model
    - Limited resources for decision making

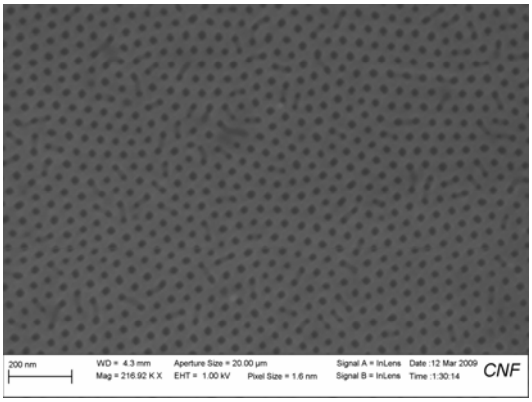
Example: The Current Economic Crisis

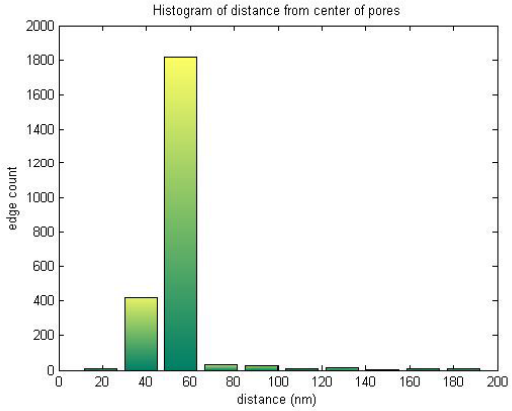
FFTs, GPUs, ALUs, Compression Engines, Transform Engines, Neurons, Analog, … in coprocessing with Exact Computing.

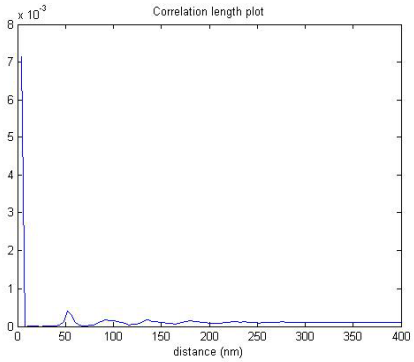
W. M. Chan et al., unpublished

Self-Assembly

PS(68k)-PMMA(33.5k) HCP BCP film on ps-r-pmma brush



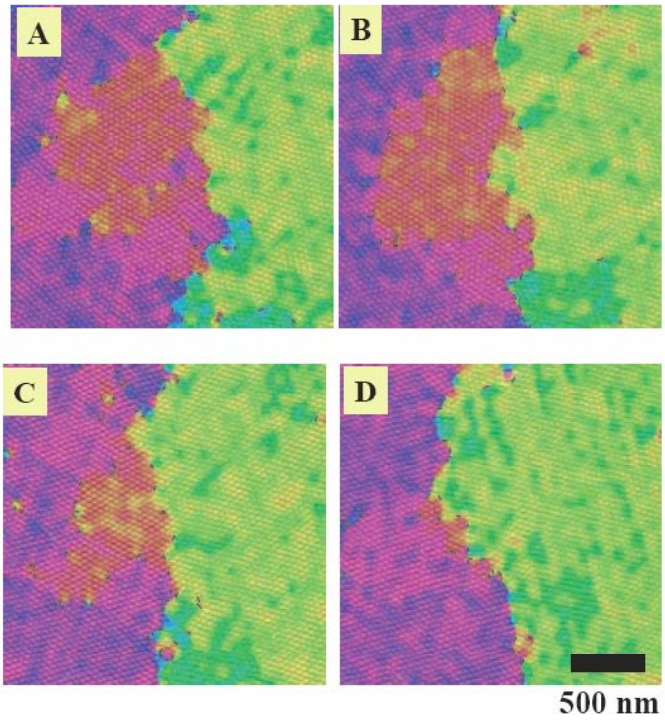




Process Variability
Defects ⇔ Activation Energies

CNT: 20% diameter control, chirality?

Energy and Defect Rates



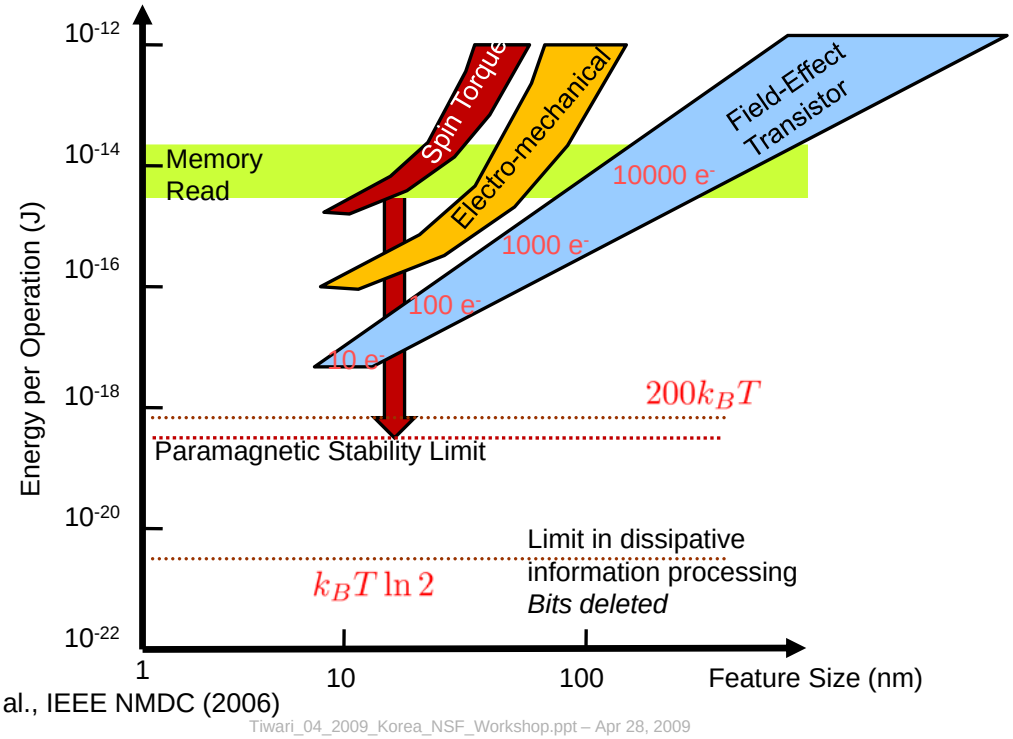
Time evolution afm snapshot of self-assembly front propagation

$t^{1/4}$ dependence

$$p \propto \exp\left(-\frac{\Delta E}{k_B T}\right)$$

C. Harrison et al., Europhysics Letters (2005)

Fundamental Limits: Energy per Operation



S. Tiwari et al., IEEE NMDC (2006)

Implications of Hierarchy - Communication

1. When M parts connected in series, the system fails when one component does.

2. If *N* components, *w* work per component over time *T*, and in communication to *N-1* others

Work produced in time *T* by individual component

$$T = \frac{w}{a} + \frac{(N-1)w}{b} + \frac{(N-1)w}{b}$$

Two Component Communications

a: rate at which individual component works

b: rate at which transmitting to others and rate at which receiving from others

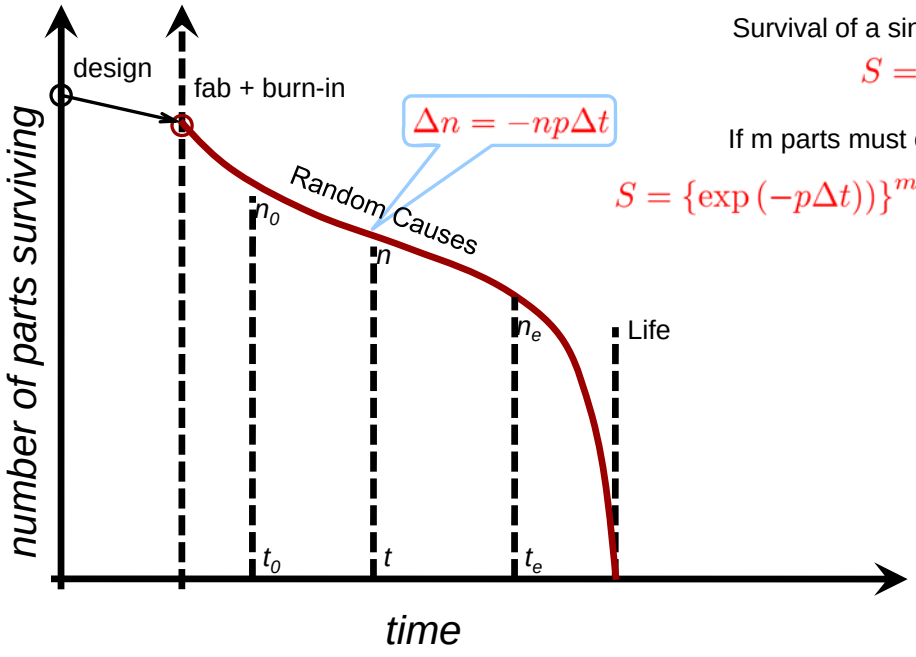
Total work output: $W = Nw$

Rate of work: $\frac{Nw}{T} = \frac{W}{T} = \frac{Nab}{b+2a(N-1)}$

If N become large $N \to \infty$

$$\frac{W}{T} \to \frac{b}{2a}$$

Large System Robustness



Survival of a single component:

$$S = \exp(-p\Delta t))$$

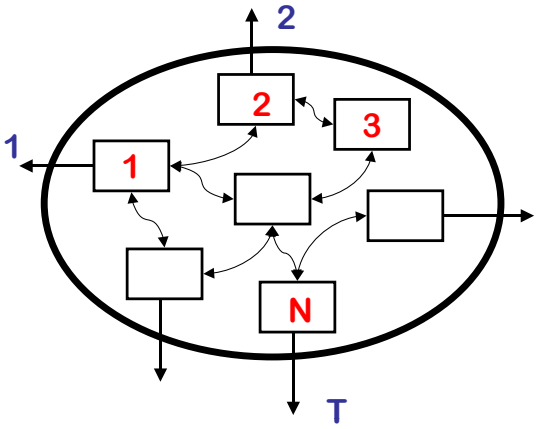
If m parts must concurrently survive

$$S = \{\exp(-p\Delta t))\}^m = \exp(-mp\Delta t))$$

Working with Defects & Power Penalty

Rent's Rule

$$T = kN^p < kN$$



T - the average no. of external terminals (pins) in a subcircuit or partition

N - is the number of modules in the subcircuit

k - Rent's constant (average no. of pins per module)

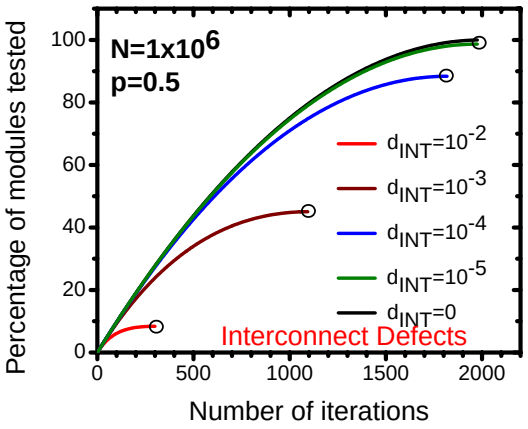
p - Rent's exponent ($0 < p < 1$)

If logic blocks defective: $N_{accessible} \sim ((1-d)N)^p$

If wiring defective, the number of testable logic blocks:

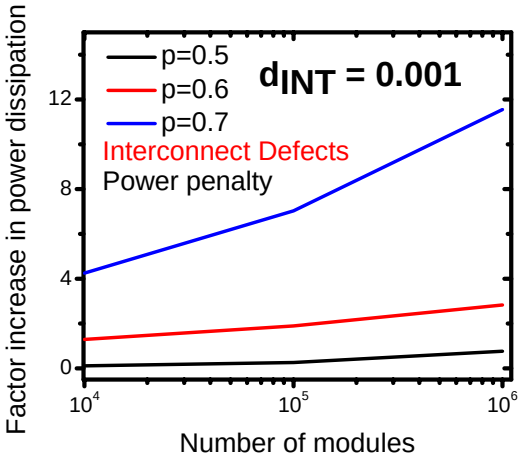
$N_{accessible} \sim (1-d)\, N^p$ - a considerably more serious problem

Defects: Configurability Penalty on Power



A. Kumar et al., DFT, 280(2004)

Defects limit testability and limit the usable devices and interconnects

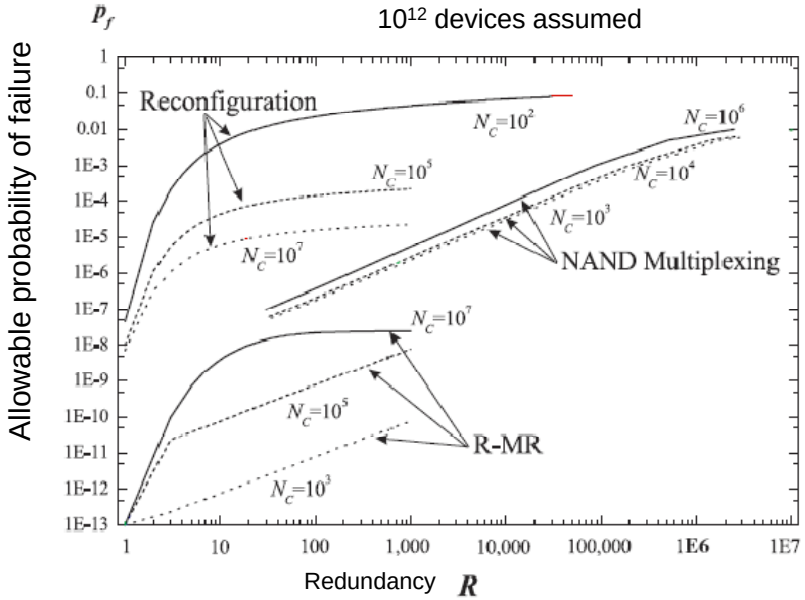


Defect rate ⇔ Optimum size of maximum functional unit that is testable and configurable

Redundancy

Nikolic et al.

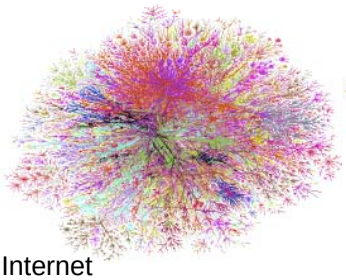
10^{12} devices assumed



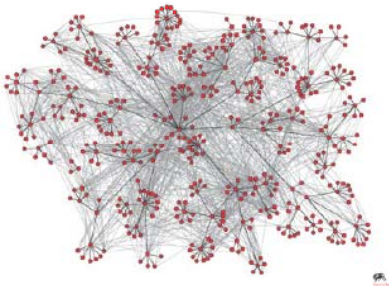
Using R-fold modular redundancy
NAND multiplexing
Reconfiguration (using knowledge of faulty devices)

Defects place severe constraints

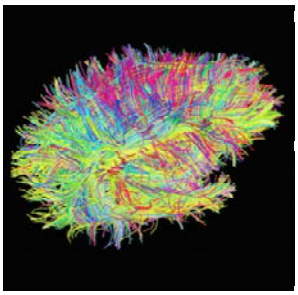
Networks: Information Flow and Robustness

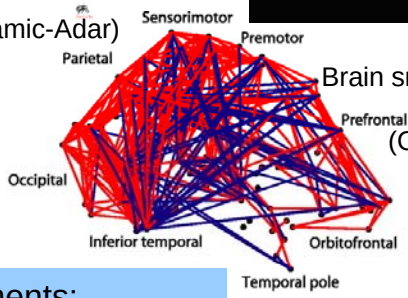


Internet
(Burch-Cheswick)

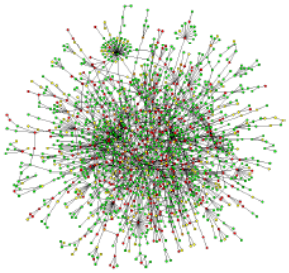


Email Communications (Adamic-Adar)





Brain small-world network
(O. Sporns)

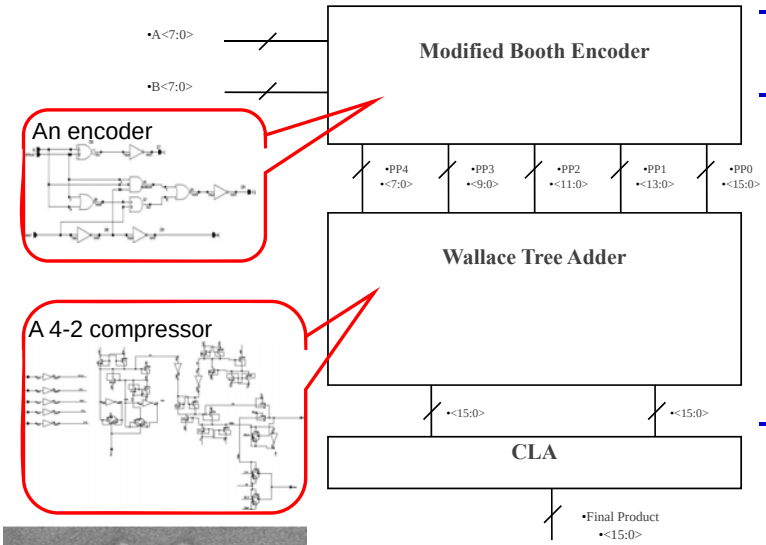


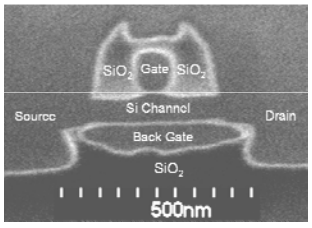
Protein Interactions
(Jeong)

Hub & Spoke arrangements:
Fixed degree at various length scales
most likely candidates for robustness

A mixture of high-degree and low-degree nodes.
A mixture of long-range and short-range links.

Adaptation





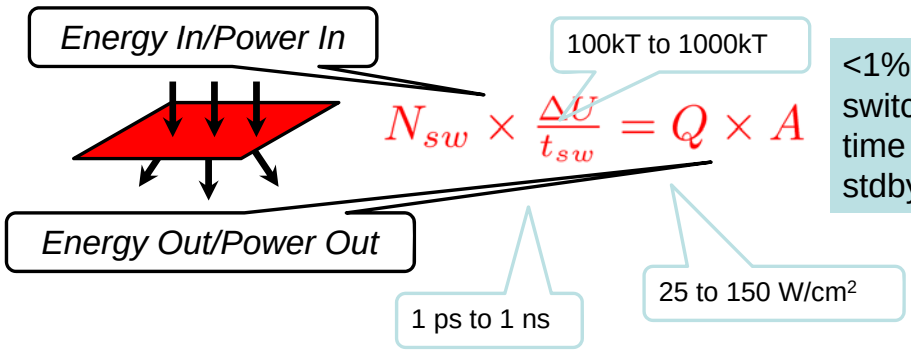
	DGFET Multiplier
Number of bits	8
Power	7.72 mW
Frequency	≈500 MHz
Device	100 nm
V_{DD}	1 V

W. M. Chan (2007)

Booth Multiplier
Nearly x10 reduction in power without sacrificing high speed. Compact and dense

In the Nanoscale Limit

10 nm λ ⟺ 7.5x10^{12} λ^2 in 1 inch^2 => 10^{12} devices/chip



A sea of compute element resources
Power and bandwidth are the scarce resources
Use the compute resources for different efficient appliances
Turn on, connect, and use only those that are necessary for the task

A **multi-tasking** chip from a sea of resources

Computing Inexactly

Algorithms:

Tolerate errors in hardware
Probabilistic approaches
…

Architecture:

Merge software and hardware through an interface
Allow specification of precision tolerance
Allow specification of incoherence tolerance
…

Implementation:

Build in dynamic testing and configuring
Implement large functions that compromise solution exactness
Devices and Circuits that address this within power and variability limits – memory, new ideas that merge functions and break boundaries effciently
…