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Technology progress of advanced gate stack and reliability issues

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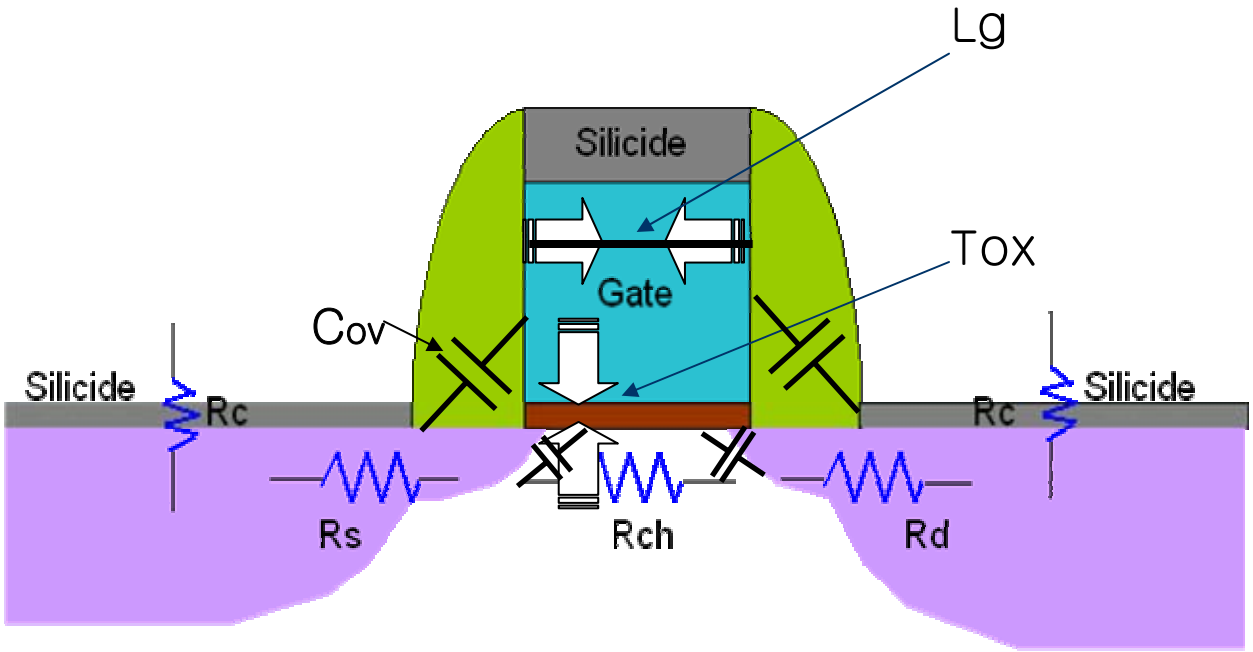
Gate Stack Scaling

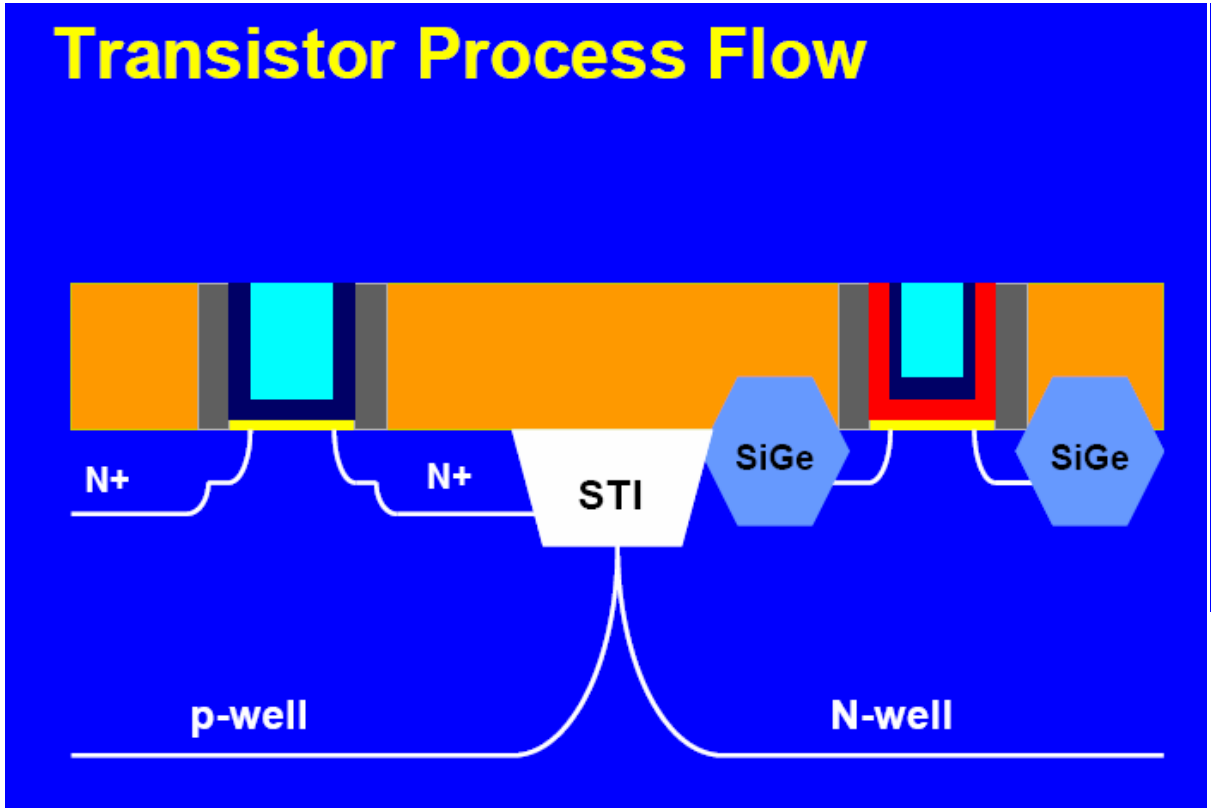


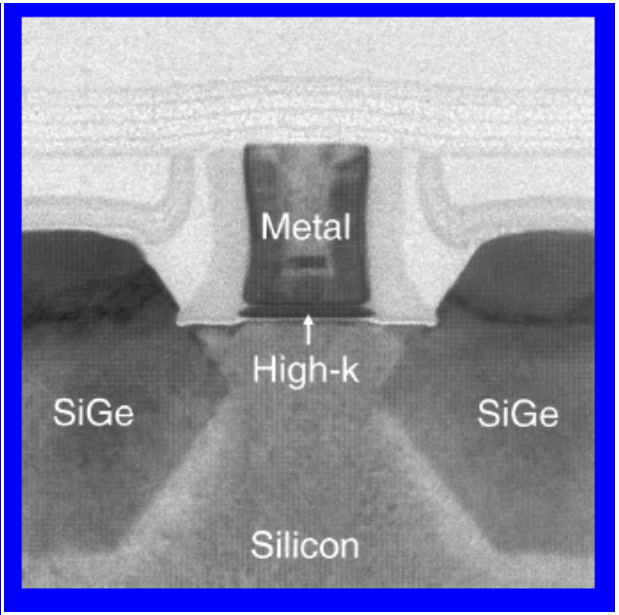
Objectives

- **Scale electrical (equivalent oxide) thickness of SiO_2 dielectric**
  - **Maximize I_{on} at a tolerable I_{off}**
  - **Little or no mobility degradation**
  - **No reliability impact (TDDB, QBD, NBTI, hot e)**
- **Scale L_g to maximize performance gain and minimize delay τ**

  (worsens Short Channel Effects)
- **Minimize depletion from (poly-Si0 electrode**
  - **Adds to electrical thickness of gate dielectric**

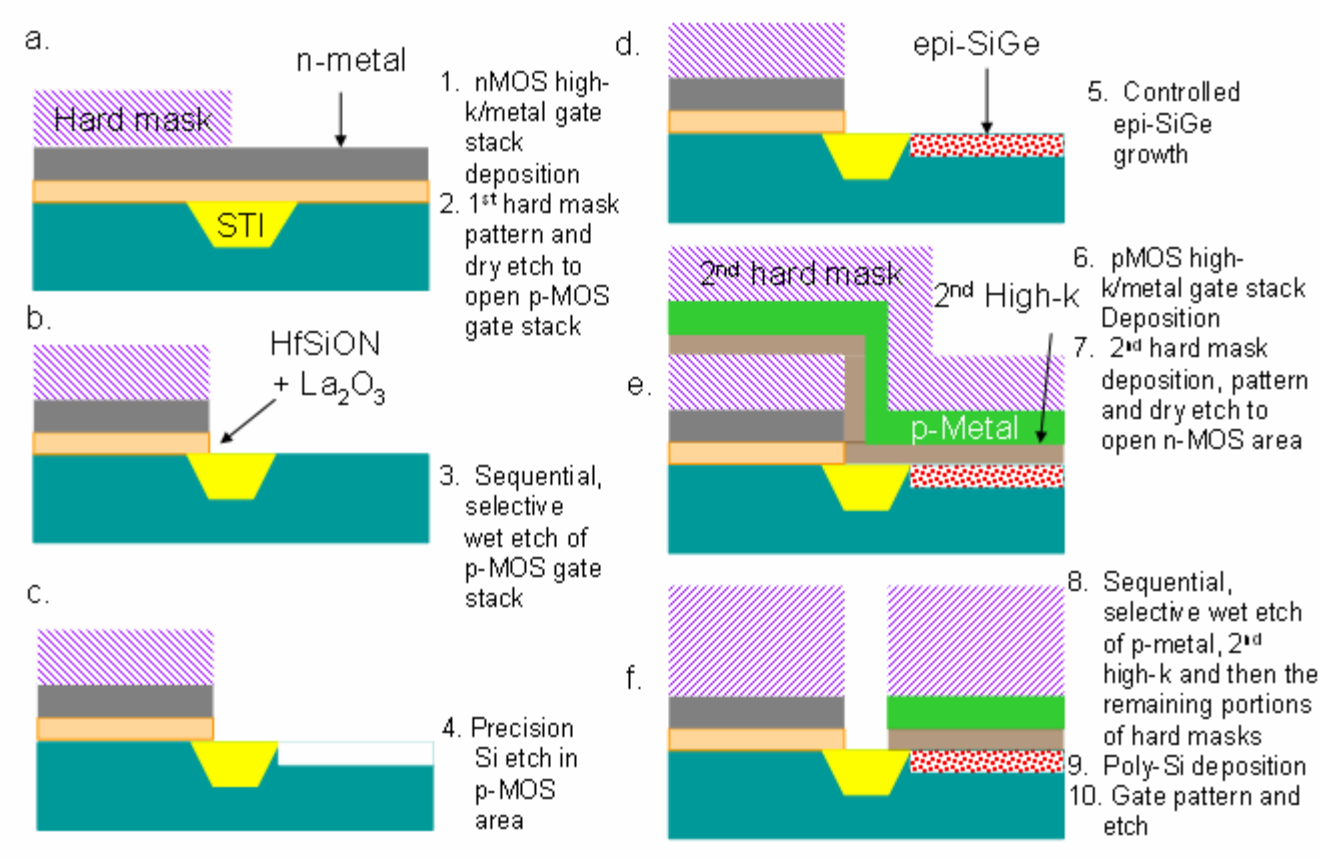
High-k/metal gate solution I





- In Feb, 2007, INTEL announced that it has implemented two materials- high-k dielectrics and metal gates for the technology
- In IEDM 2007, Intel presented dual replacement gate process for metal gate with extremely improved pFET performance

High-k/metal gate solution II



- In 2007 VLSI, SEMATECH published a novel high-k integration scheme using SiGe for PMOSFET for Vt control

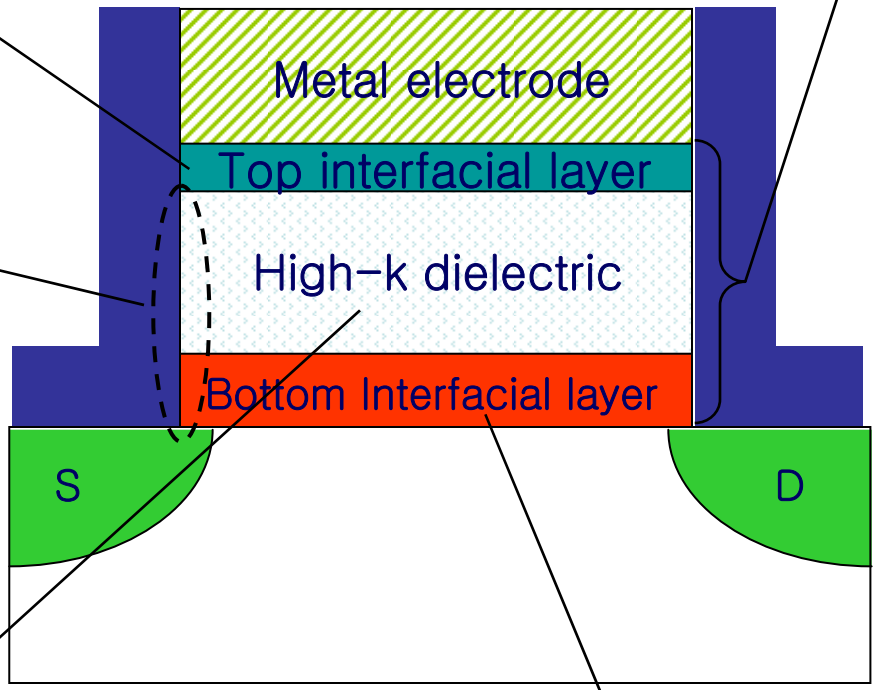
Outline

- Overview of technology progress
  - High-k Dielectric scaling
  - Metal gate electrode
- Reliability methodologies and status
  - Charge trapping and BTI
  - Breakdown

New materials require new methodologies

Dipole formation, pinning?
(V_{TH} controllability issue)
→ Complicate to measure effective metal work function

Complex fixed charge distribution → Complicate to measure effective metal work function



<u>Heterogeneous interface</u>
Leakage or breakdown path??
Different fringe field behavior

Transient charging effect due to relatively higher bulk traps

Dipole formation
Screening effect on remote phonon scattering

Demand on new methodologies

- **Metal gate/high-k gate stack devices have physical and electrical properties different from conventional polysilicon/ SiO_2 gate stack devices**
  - *Dielectric stack consists of multiple layers*
  - *Smaller bandgap and bandgap offsets*
  - *Influence of metal electrodes*
  - *Transient charging effects (TCE)*

⇒ Hard to import and apply SiO_2 test methodologies
⇒ Needs novel methodologies to decouple contributions from different components of the gate

Winner should be ….

From Bin Yu's publication in ICSICT

- Simple and low cost manufacturing than silicon CMOS chip
- Intrinsic potential to improve chip performance by orders of magnitude – not only a diminutive or incremental difference
- Feasibility to achieve super-high integration density – greater than 10^{10} transistors or other computing components per circuit
- High reproducibility to manufacture
- High reliability – at least comparable to silicon chips in terms of key component lifetime
- Remarkably lowered power dissipation

Acknowledgements

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