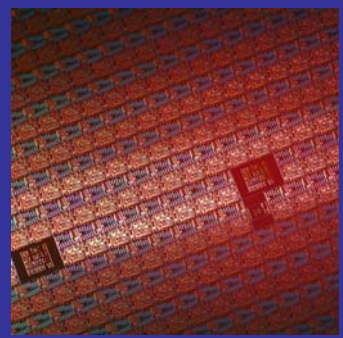
US Korea NanoForum
April 2009

Accelerating the next technology revolution

CMOS Scaling for the Next Decade and Emerging Technologies:

SEMATECH Perspective



Prashant Majhi
Front End Processes, SEMATECH

SEMATECH's 20-year Evolution

Mfg Productivity

SVTC: Foundry

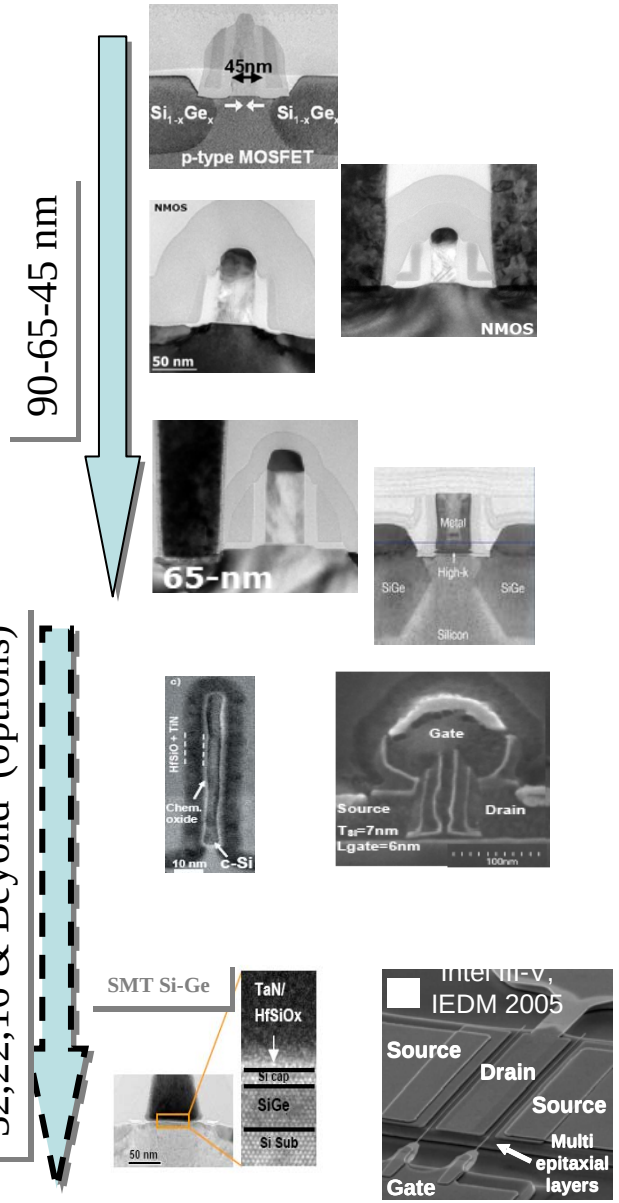
Research & Development

Today:

SEMATECH is non-profit research & development consortium with global membership of chipmakers, suppliers, universities, and governments to drive technology commercialization.

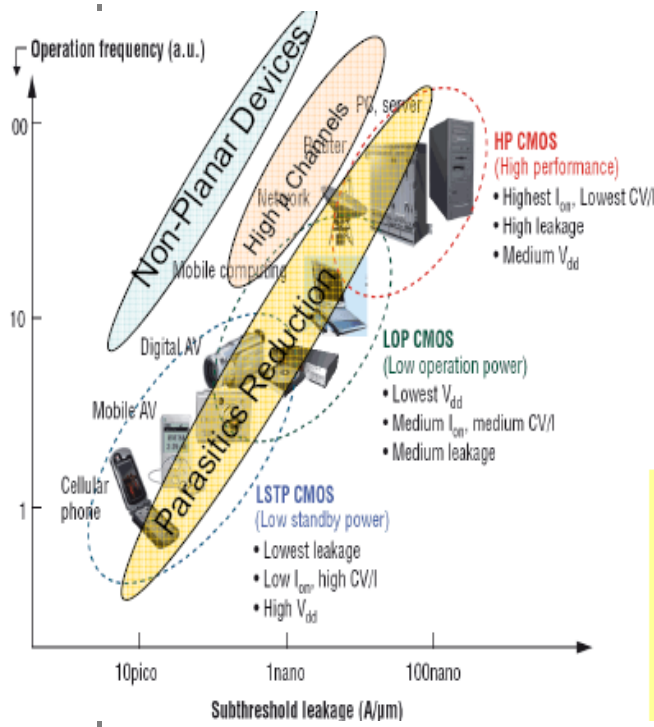
Generic MOSFET Scaling

Trends/Innovations



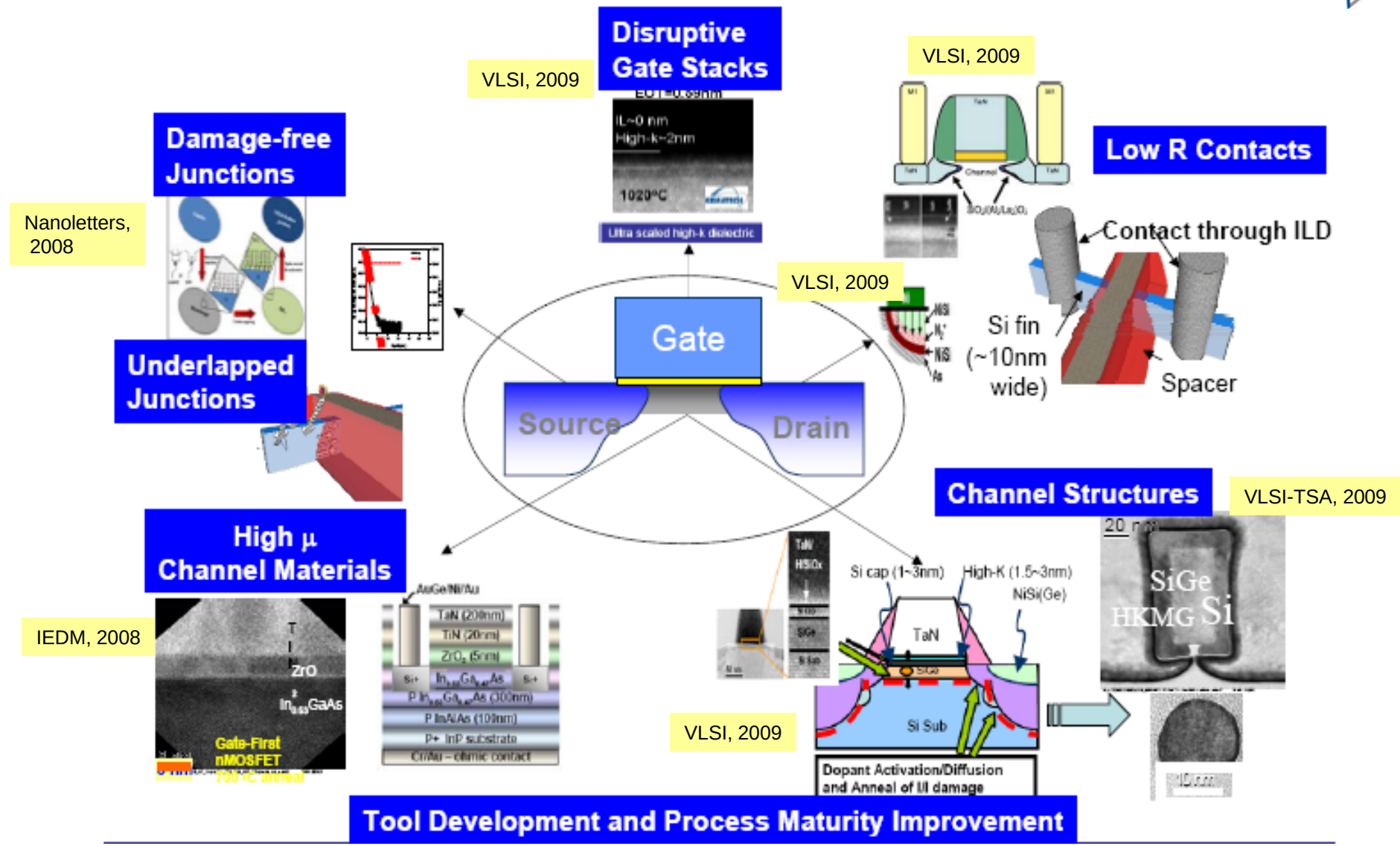
Key Innovations

- Uniaxial Strain
- Scaled Oxynitrides
- NiSi (doped)
- SOI / SOA
- **High-k / Metal Gates**
- Strain Additivity
- Millisecond Anneals
- Low K Spacers
- Dual WF silicides
- Dopant Seg. Schottky FE
- Non-Planar FETs
- High Mobility Channels
- STEEP Devices
- Novel SRAM concepts



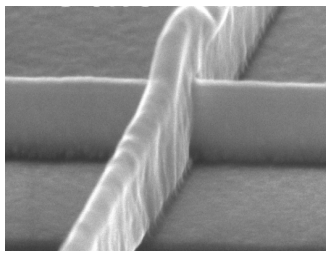
Modules currently under R&D

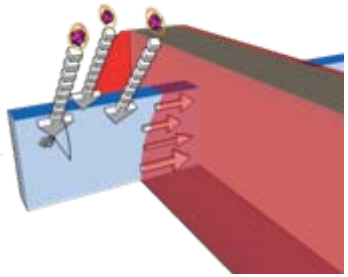
SEMATECH CMOS Activities

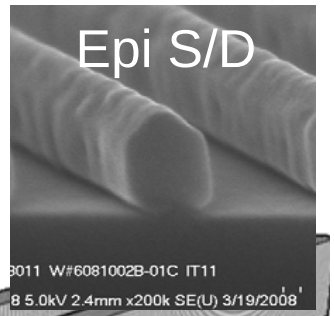


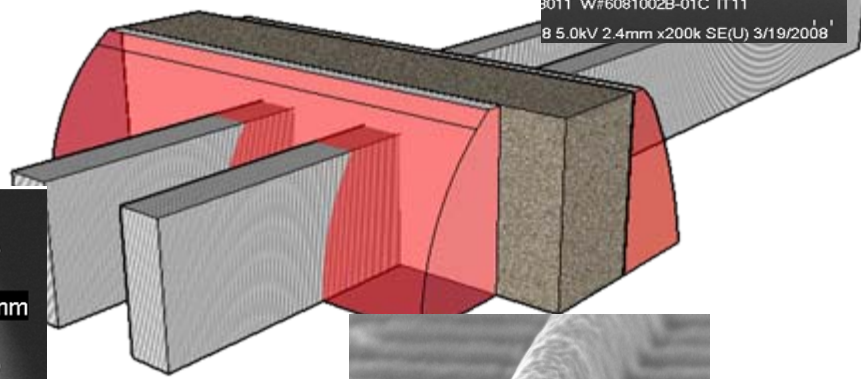
Non-Planar Devices:
Similar Module Challenges & improved SCE

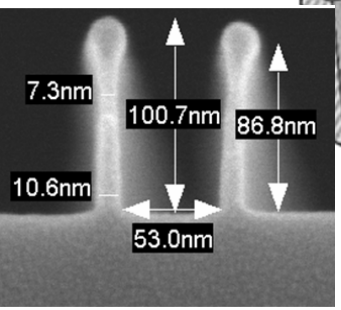
R. Harris, P. Majhi (SEMATECH),
Stanford workshop on MUGFETs, 2007;SEMICON 2008

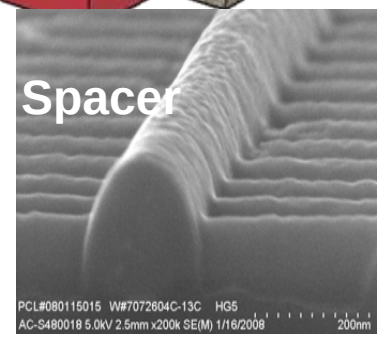


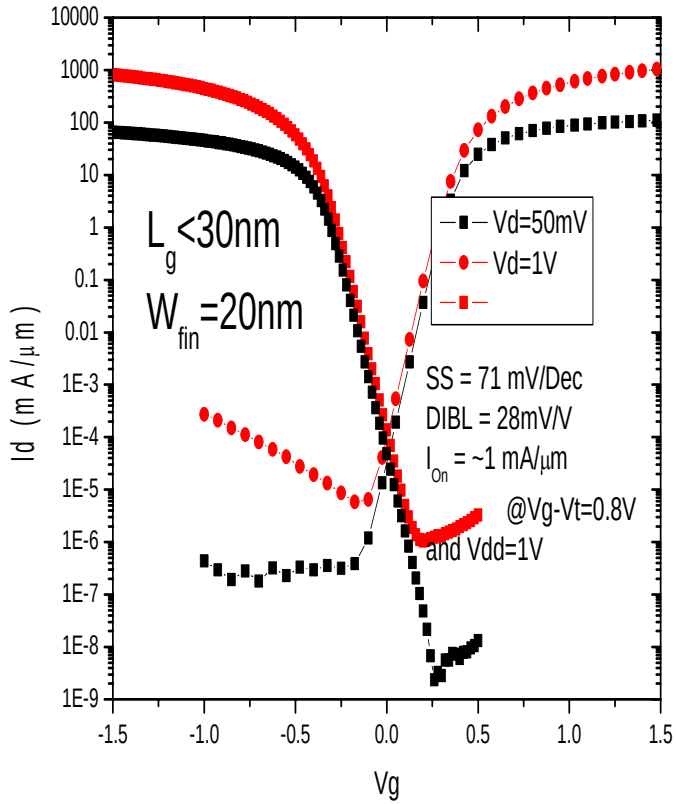












Key Challenges with High μ Channel Materials

Group consensus in SEMATECH hosted workshop **"New Channel Materials for Future MOSFET Technology"** ***Dec'06-07***

Challenges with Ge devices

1. Short Lg demonstration
   - BTBT due to low Eg?
   - Compete with strained Si

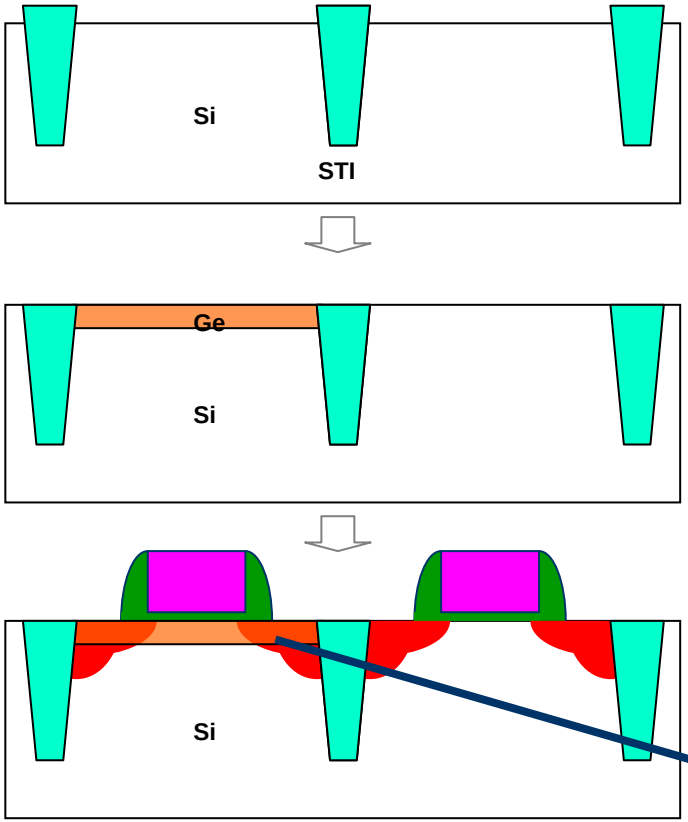
2. CMOS ?
   - NMOS: practical or fundamental barrier?

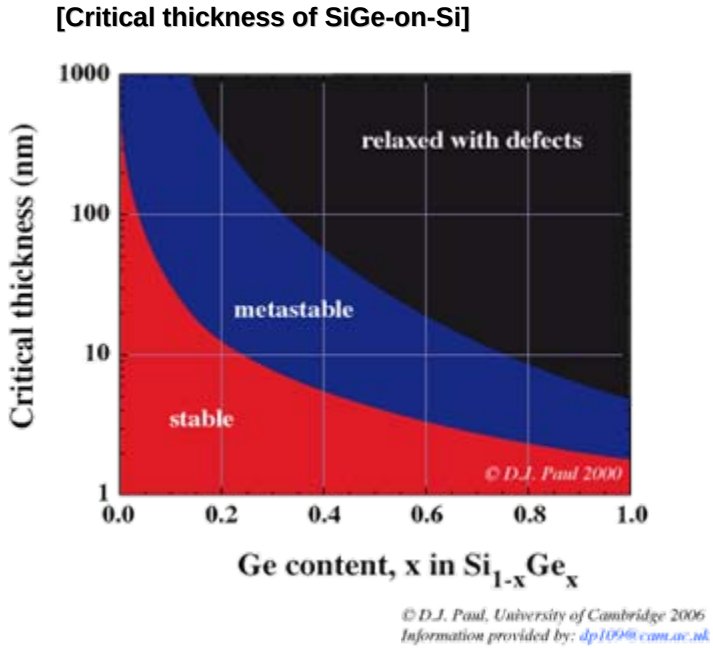
3. Gate Stacks
   - scalability
   - reliability

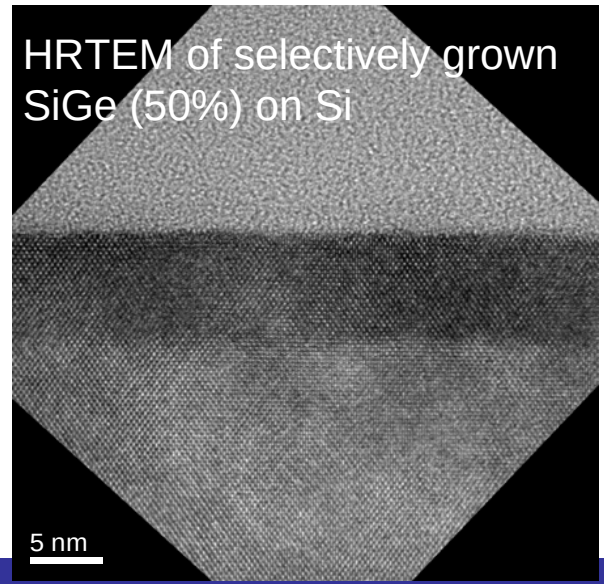
4. Heterogeneous integration on Si
   - selective epi ?

Several Other Challenges w.r.t Metrology, Process Challenges…

High Mobility Materials on Si Platform

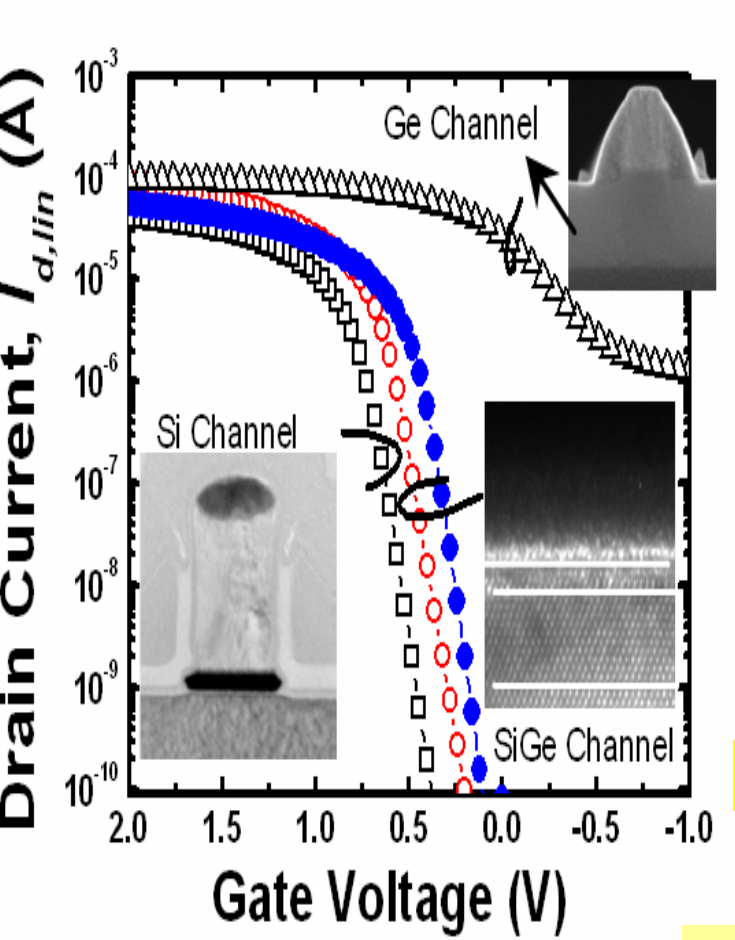


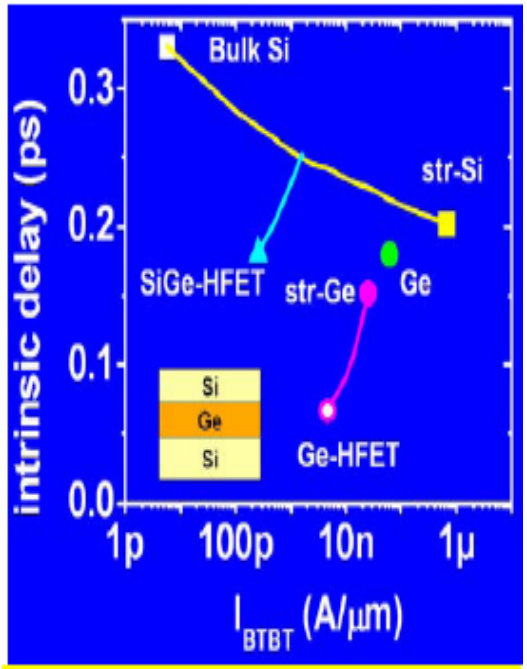




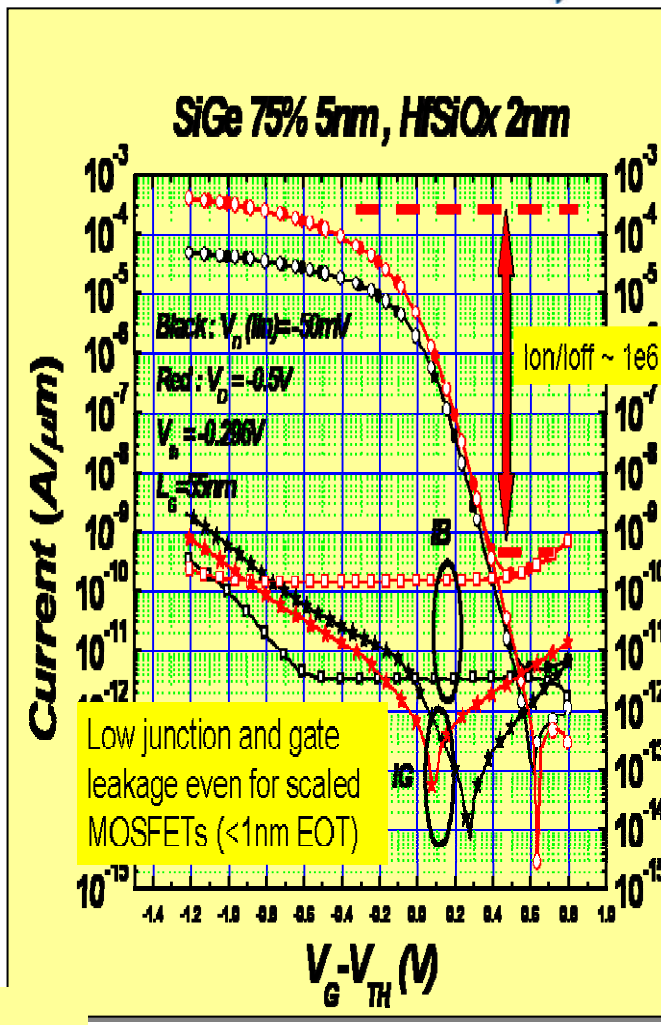
- *Selective* deposition of Ge on Si
- Thin – below critical thickness
  - Low defect density
- Can be used for SiGe, Ge, III-V
- Confine inversion layer

Short Lg MOSFETs on Ge Based Channels:
Ion and Ioff Control





Krishnamohan, Saraswat (Stanford)



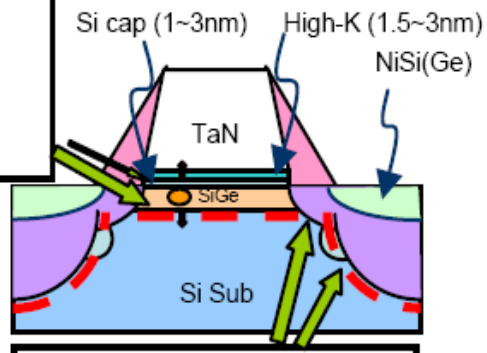
Ioff can be controlled in heterostructures

P. Majhi et.al, SEMATECH, EDL 2008

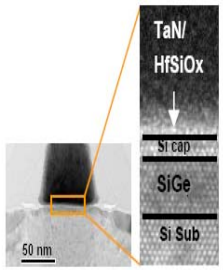
S. Lee et.al, SEMATECH, EDL 2008

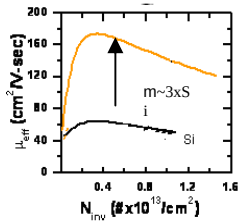
Planar and Non-Planar Si/SiGe/Si QW pMOSFETs

-SiGe relaxation if thickness above tc (with defect generation)
-SiGe relaxation from thermal treatment (with defect generation)
-Si-Ge inter-diffusion

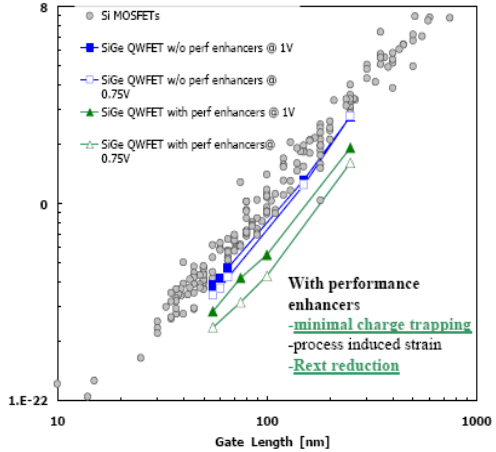


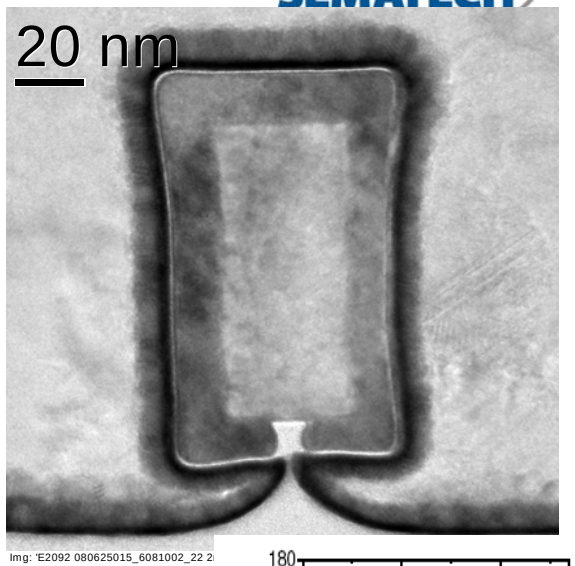
Dopant Activation/Diffusion and Anneal of I/I damage

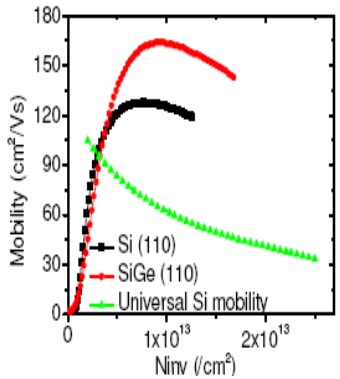




SEMATECH, EDL 2008, VLSI 2009





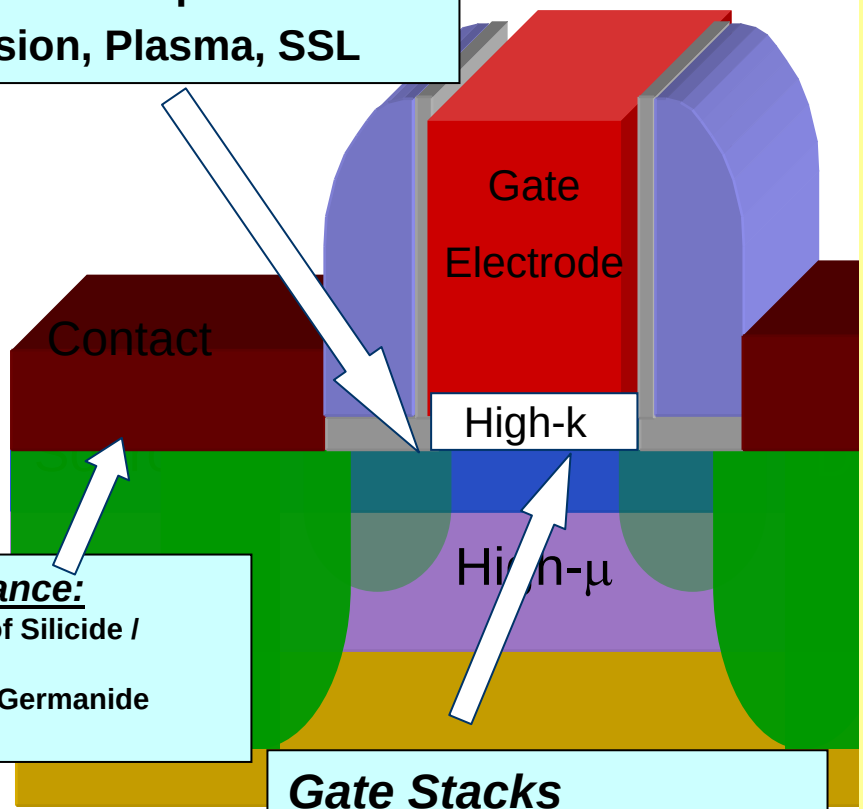


SEMATECH, VLSI-TSA 2009

- Best reported short Lg pFET (I_{on}/I_{off} ~ 5e4 !) devices with high Ge%. Better than state-of-art Si on power / performance metric
- Also demonstrated concept in scaled non-planar scheme

Ge “N”MOS Issue: “Is it INTRINSIC ?”

Junction Extensions:
- **USJ: Flash/Spike anneals**
- **Infusion, Plasma, SSL**



Contact Resistance:
- **Schottky Barrier of Silicide / Germanides**
- **Doped Ni Silicide/Germanide**
- **Schottky FETs**

Gate Stacks
- **High-k/metals**
- **No fermi-level pinning**
- **scalability**
- **reliability**

- Dit/Nit
  - -High Dit/Nit near Ec
  - - But what about GeO2?
- Low SSL and High diffusivity, and hence poor shallow junctions
  - -What about milli-sec anneals ?
- Fermi-Level Pinning at Ev and hence high Schottky Barrier Height for n-Ge.
  - -What about SBH modulation techniques
  - - what about Germanides ?

Key Challenges with High μ Channel Materials

Group consensus in SEMATECH hosted workshop **"New Channel Materials for Future MOSFET Technology"** ***Dec'07-08***

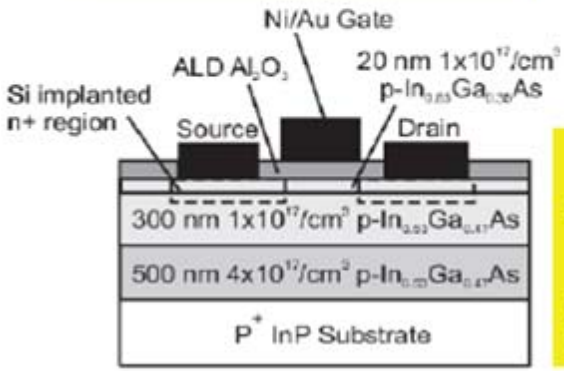
Challenges with III-V devices

1. III-V on Si
2. **PMOS**
3. Scalability
4. Enhancement mode
5. Gate Stacks

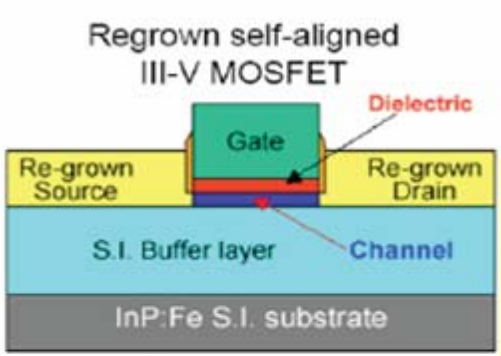
Several Other Challenges w.r.t Metrology, Process Challenges…

Classification of III-V FETs Being Evaluated

SURFACE Channel



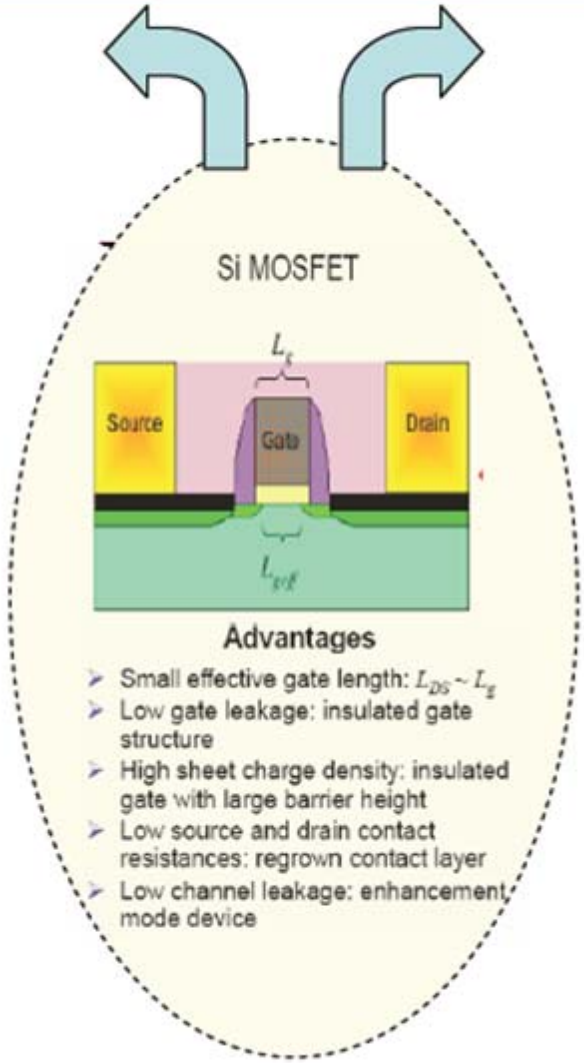
I/I junctions



insitu-doped S/D

Regrown Structure

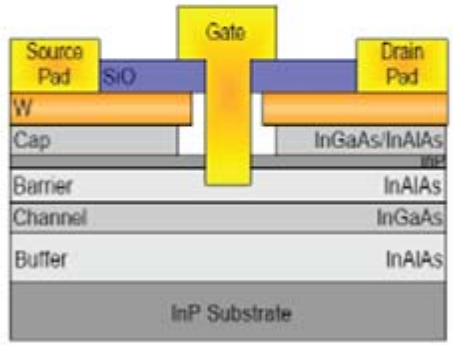
- Regrown self-aligned III-V MOSFET structure mimics advanced Si device designs.
- Low temperature process for regrown source/drain contacts
  - High doping concentration → low contact resistance
  - Better geometry control → $L_{DS} \approx L_g$
  - Preserve dielectric/channel interface quality



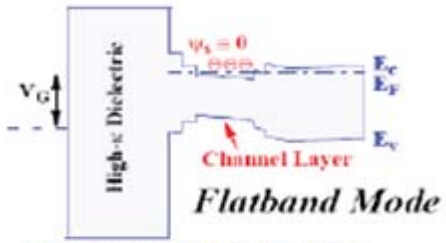
Advantages

- Small effective gate length: $L_{DS} \sim L_g$
- Low gate leakage: insulated gate structure
- High sheet charge density: insulated gate with large barrier height
- Low source and drain contact resistances: regrown contact layer
- Low channel leakage: enhancement mode device

BURIED Channel



Schottky Gate



Flatband Mode

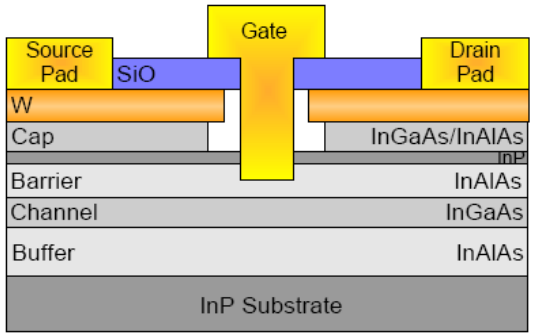
- Majority Carrier Device
  ⇒ Majority Carrier Mobility ($\mu_n > 10{,}000$ cm^2/Vs for $In_{0.75}Ga_{0.25}As$)
- Smaller Surface Potential
  $\psi_s << E_G$, $\psi_s \cong 0$: Shallower Quantum Wells
  ⇒ Smaller Quantization
  ⇒ Higher DOS
  ⇒ Less Intervalley Scattering

MOSFET

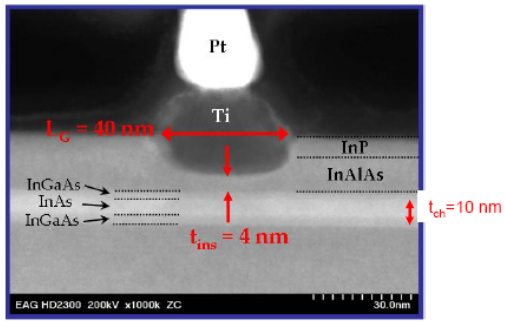
W. Tsai, P.Majhi, New CMOS Channel Materials, ITRS on-line workshop, July 2008

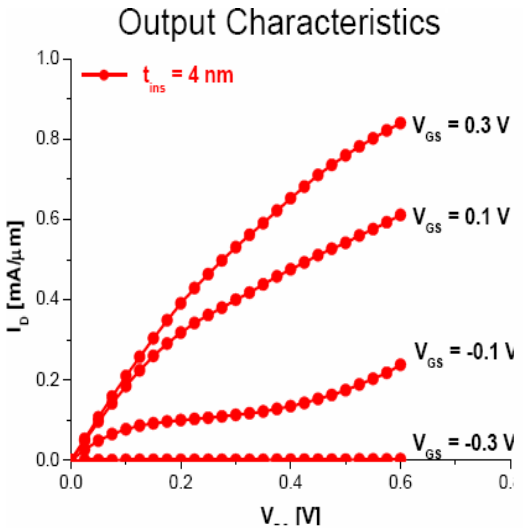
III-V FETs Grand Challenge:

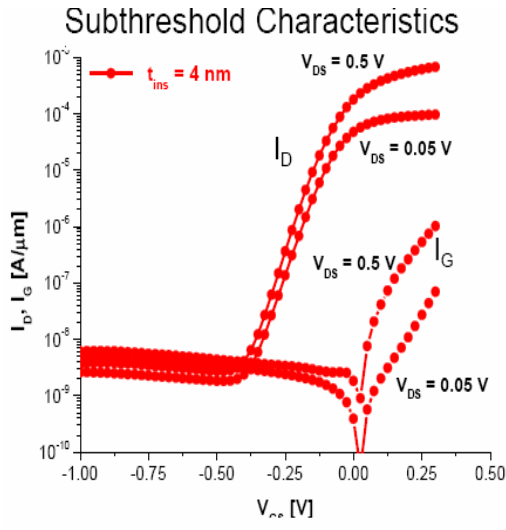
Short Channel Performance (Del Alamo et.al IEDM 2007)



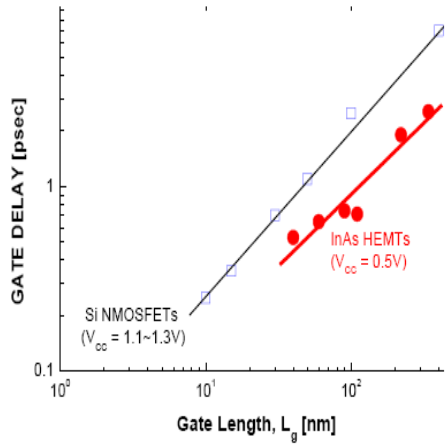
Kim, IEDM 2007





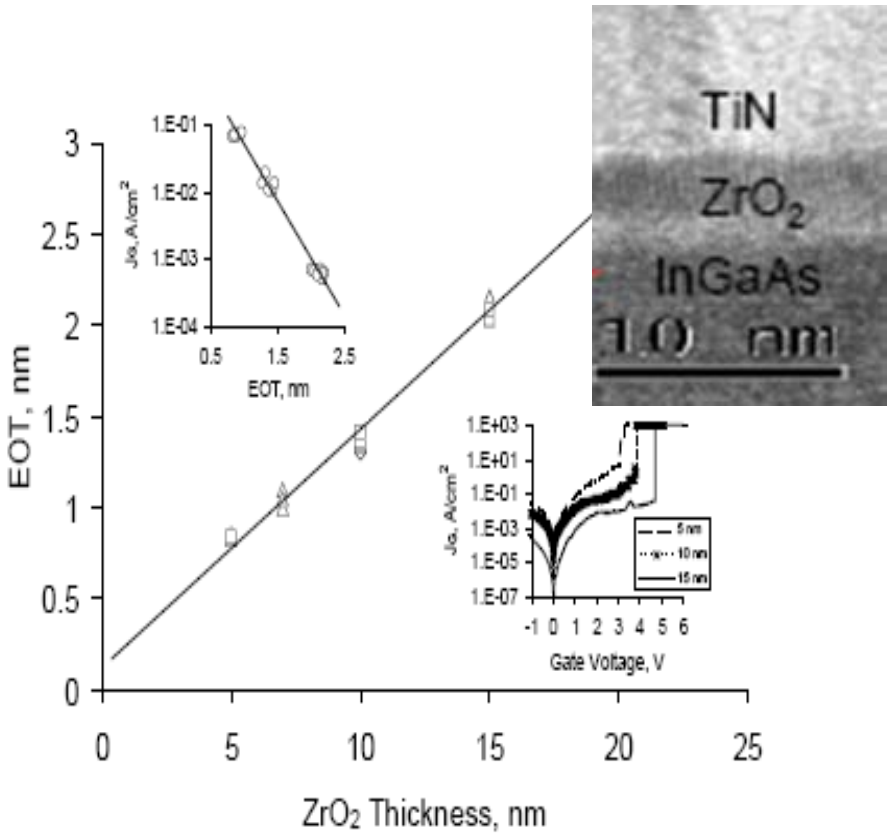


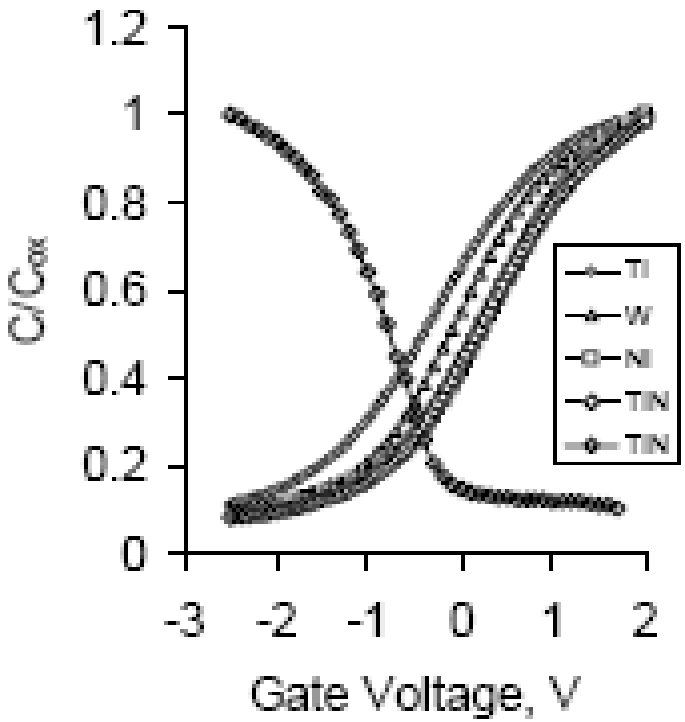
- I_{ON}-I_{Leak} characteristics better than 65 nm CMOS at 0.5 V
- Excellent scaling behavior of gate delay down to 40 nm
- 1.6X higher source injection velocity than Si at VDS=0.5 V
- NEED high-k for Ioff control; and Rext (eliminate resistance contribution from barrier layer)



Manufacturable and Scalable Gate Stacks on InGaAs

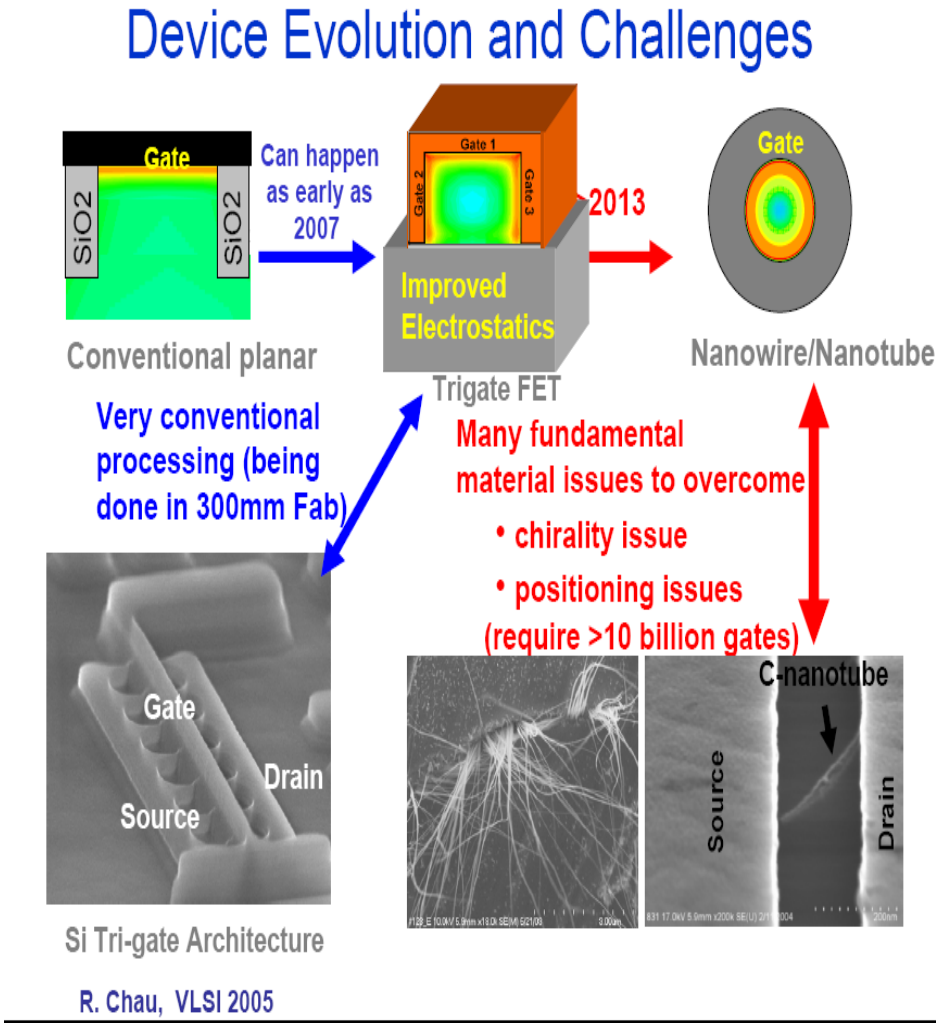
Intel-SEMATECH (in APL, DRC, IEDM 2008)

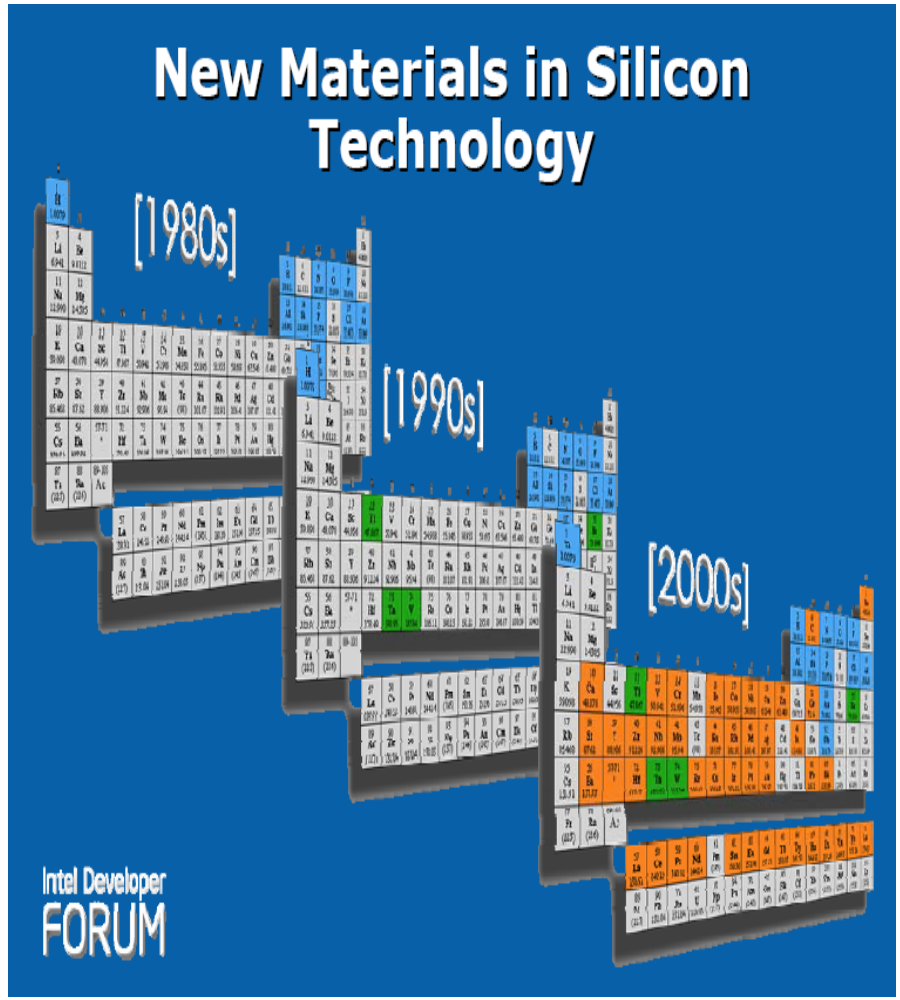




- Lowest CET devices on III-V to-date
- Ability to tune Vfb with Metal work function
- Surface channel mobility needs improvement (currently ~ 2000 cm2/v.sec)

CMOS Scaling Enabled by New Materials and/or Architecture





SEMATECH Extensive R&D Network

- **University Network:** 80+ schools
- Examples: MIT, Stanford, Berkeley, UIUC, CMU, GATech, UT Austin
- Students completed (or completing) their PhD research: 27
- Co-authored papers = 180+
- Jointly arranged conferences, workshops = 9

National Lab Network:

- BHNL Synchrotron XPS, XSW
- LANL Neutron SANS, SPEAR
- ORNL HR TEM
- ANL Ferroelectric, piezoelectric
- Sandia MEMS
- NIST FTIR,1/f Noise, XRD

Austin, TX:
Home of FEP, Emerging Technologies and ISMI

Premier user of 68,000 sq. ft. class 1 clean room for 200/300mm wafers

R&D of advanced materials/structures

Albany, NY:
SEMATECH North
Funded by State of NY
Home of Lithography, 3D Interconnect, Metrology and FEP

300,000 sq. ft. class 1 clean room
State of the art tools for 300 mm wafers

Summary

- CMOS Scaling is feasible only with New Materials (High-k/Metals, Dual/Engineered Silicides, SiC/SiGe S/D, Non-Si channels).

- Numerous challenges facing CMOS Scaling, but numerous opportunities as well. With intense and focused research (industry- academia) these challenges are surmountable !

- SEMATECH evaluating use of its well recognized skill base to execute emerging nanotechnology R&D agenda in:
  - NEMS, Sensors, Energy, Biotech, Photonics, III-V structures
  - Electrical characterization and failure analysis
  - Centered around univ network with faculty / students participation