RTD-based High Speed and Low Power Integrated Circuits

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Outline

- Introduction
- RTD/HEMT Integration Technology
- RTD-based NRZ-mode D-F/F
- MOBILE Using only RTDs
- Lateral Scaling of RTD Area
- Summary
Various extensions of the MOBILE (MOnostable-to-BIstable transition Logic Element) concept with reduced circuit complexity and power dissipation have been proposed:

- Static binary frequency divider: 34 Gb/s operation with under 10 mW power dissipation
- Multi-valued logic circuits: Various multi-valued logic circuits utilizing multi-peak characteristics of series connected RTDs
- Threshold logic gates: Linear and multi-threshold threshold logic circuits
MOBILE for High-speed/Low-power Digital ICs (2)

- MOBILE for high-speed optical communications
  - 80 Gb/s operation with 7.68 mW power dissipation using UTC-PD

- MOBILE using molecular RTDs
  - Latch, shift register, Boolean logic, and memory array have been proposed

- Co-integration of RTDs with CMOS
  - SRAM memory cell was demonstrated
  - InP-based RTD on Si substrate was demonstrated

- Optical MOBILE (H. Matsuzaki et al., IEEE JSSC, 2001)
- Molecular MOBILE (H. Matsuzaki et al., IEEE ISSCC, 2002)
- Fluoride RTD on Si (T. Terayama et al., JJAP, 2002)
- InP RTD on Si (W. Prost et al., ESSDERC, 2005)
To fabricate RTD-based high-speed and low-power logic circuits, RTD/HEMT integration technology is developed.

- Peak Current Density ($J_p$) = 112 kA/cm$^2$
- Peak voltage ($V_p$) = 0.3 V, PVCR = 12
  - RTD demonstrated harmonic oscillation of > 1 THz. (TIT, 2008)

- $G_m = 1.2$ S/mm, $f_T = 220$ GHz
  - 15nm HEMT with $f_T$ of 610GHz. (SNU, 2007)
  - 30nm HEMT of $f_T$, $f_{max}$ > 500GHz. (MIT, 2008)
MOBILE-based NRZ D-F/F

- Limit of MOBILE
  - RZ-mode operation: Incompatibility to conventional NRZ-mode logic circuit

- MOBILE-based NRZ D-F/F
  - Non-Return-to-Zero operation by combining original MOBILE with set/reset flip-flop

12.5 Gb/s with about 10mW power consumption (RTD/HEMT technology)

32 Gb/s with 45mW power consumption (RTD/HBT technology)

Large increase in circuit complexity & power consumption compared to original MOBILE

→ Need new circuit topology which inherits MOBILE’s merits with NRZ mode operation
New NRZ-mode Logic Element Using RHS As Load

Conventional MOBILE configuration

A New RHS/RHP Logic Element

Advantages of Newly Proposed RHS/RHP Logic Element

- **High-speed and low-power operation**
- **Reduced circuit complexity**
- **Compatibility to the conventional digital ICs – NRZ-mode operation**
- **Reduced clock loading**
Measurement Results

< Microphotograph of the fabricated IC >

(Single)
• Operating Speed : 36 Gbps
• Power Dissipation ~ 2.5 mW
• Device count : 4 (2 RTDs and 2 HEMTs)

(Differential)
• Operating Speed : > 12.5 Gbps
• Power Dissipation ~ 10 mW
• Device count : 9 (4 RTDs and 5 HEMTs)

< Measured output waveform at 12.5 Gb/s >

< Measured eye-diagram at 12.5 Gb/s >
In this work, the CML–Type RTD/HBT based High-Speed/Low-Power NRZ D-Flip Flop with differential output has been developed.
For the first time, the CML-type RTD/HBT based 2:1 Multiplexer has been developed.
To fully exploit high-speed/low-power characteristics of RTDs, MOBILE using only RTDs is designed and demonstrated up to 40 Gbps with very low-power dissipation about 0.86 mW.

Minimum power-delay product of about 22 fJ was obtained by considering AC current effect of MOBILE and designing MOBILE using only RTDs without TRs.

Cf.) 42 fJ using RTD/Schottky diode, 48 fJ using RTD/HEMT, and 96 fJ using RTD/UTC-PD.
Minimum power-delay product of about 22 fJ was obtained by considering AC current effect of MOBILE and designing MOBILE using only RTDs without TRs.

Ref.) 42 fJ using RTD/Schottky diode, 48 fJ using RTD/HEMT, and 96 fJ using RTD/UTC-PD
Flash ADC is the fastest ADC topology
- Limit of resolution bit due to device count \( 2^{n-1} \)

Using RTDs, device count can be reduced
- 2-stage operation
- Increase in circuit complexity due to encoding circuit

Using the proposed literal gates, ADC can be implemented more compactly
- 1-stage operation with n literal gates
Previously reported MOBILE-based logic circuits utilize NDR characteristics and multi-peak characteristics for the switching

- Need increased circuit complexity to implement complex functions

Universal literal gate based on the proposed MOBILE can be implemented using simple circuit configuration by utilizing NDR characteristics and multi-peak characteristics for both switching and current modulation
3-bit Flash ADC Using Proposed Universal Literal Gate

- 3-bit flash ADC using only RTDs
- 3-bit ADC was designed using the proposed MVL circuits using only RTDs
  - 15 devices (10 RTDs and 5 resistors)
  - ~ 5.2 mW power dissipation (core circuit)

- Designed flash ADC circuits exhibit advantages in terms of device count, circuit complexity and power dissipation with respect to the previously reported circuit.
In this work, the RTD/HBT based **Differential-mode VCO** has been developed
Nano-scale RTD Fabrication – Dry etching

- ICP dry etching
- Remote ICP SiN passivation
- BCB etchback

RTD with lateral scale of up to 50 nm has been fabricated
- Peak current = 0.6 uA, PVCR ~ 4.7
MOBILE using Nano-scale RTDs

**MOBILE operation and MVL operation using 200 nm-scale RTDs were confirmed**

**Core size: 0.8x1.4 μm², Measured DC power dissipation ~ 6.6 μW**
Potential of III-V Devices for more than Moore (I)

Likharev’s CMOL (Hybrid CMOS/Nanoelectronic IC)

Sub-22 nm node

Target of EU’s DUALLOGIC Project
- Next Generation CMOS
Potential of III-V Devices for more than Moore (II)

**Optical Interconnect**
(F. E. Doany, IBM, 2008)

- Module-based 300Gb/s optical interconnect (300Gb/s; 12.5Gb/s x 24 channel)
- More functionalities with III-N materials
  - High power & high temperature
  - Wide optical spectrum
  - Thermoelectricity & Piezoelectricity

**III-V on Si & III-V Devices**
- Periodic IMF array
- QD Dislocation Filtering
- Growth on Structured Substrate
- Wafer Bonding
- SoP Integration

* Tb/s Optical Interconnect
RTD-based high-speed and low-power circuits with reduced circuit complexity are designed and demonstrated

- 36 Gbps operation of NRZ-mode logic element using only 2 HEMTs and 2 RTDs
- 40 Gbps operation of RTD-only MOBILE with power-delay product of 22 fJ.
- 3-bit ADC circuit with reduced circuit complexity (using only 15 devices) based on the newly proposed universal literal gate.
- 45 Gbps, 22.5mW operation of RTD/HBT CML-type 2:1 Multiplexer

Nano-scale RTD fabrication was demonstrated.
- To fabricate nano-scale RTD, quasi-planar fabrication process with low-damage dry etching is developed.
- 50 nm scale RTD with high PVCR of 4.7 was successfully demonstrated.
- MOBILE operation and MVL operation using 200 nm-scale RTDs were confirmed.

Advanced process techniques such as neutral beam etching, MOS-like passivation or selective epitaxy are necessary for nano-scale RTD ICs.

RTDs’ are still promising for high speed & low power nanoscale ICs.
Thank You for Your Attention!

Any Questions?