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RTD-based High Speed and Low Power Integrated Circuits

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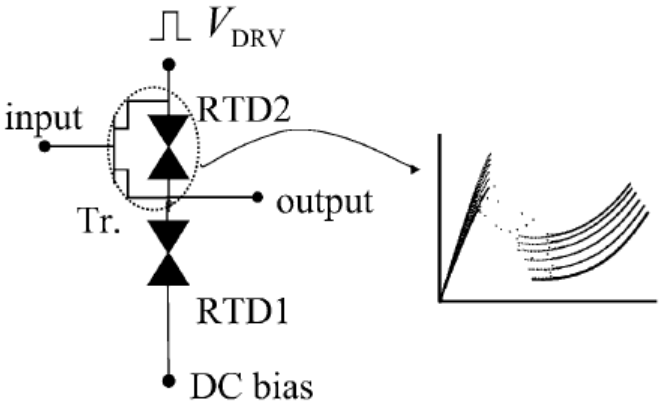
Outline

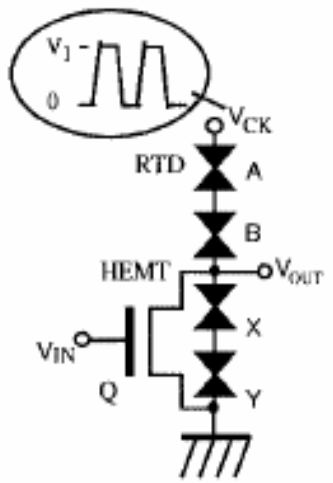
- Introduction
- RTD/HEMT Integration Technology
- RTD-based NRZ-mode D-F/F
- MOBILE Using only RTDs
- Lateral Scaling of RTD Area
- Summary

MOBILE for High-speed/Low-power Digital ICs (1)

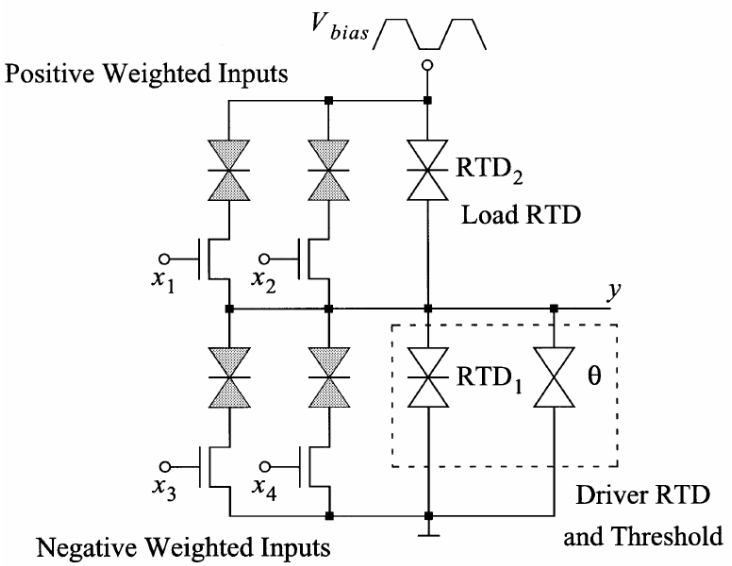
- Various extensions of the MOBILE (MOnostable-to-BIstable transition Logic Element) concept with *reduced circuit complexity and power dissipation* have been proposed
  - Static binary frequency divider : 34 Gb/s operation with under 10 mW power dissipation
  - Multi-valued logic circuits : Various multi-valued logic circuits utilizing multi-peak characteristics of series connected RTDs
  - Threshold logic gates : Linear and multi-threshold threshold logic circuits



[MOBILE Noninverting D-F/F]



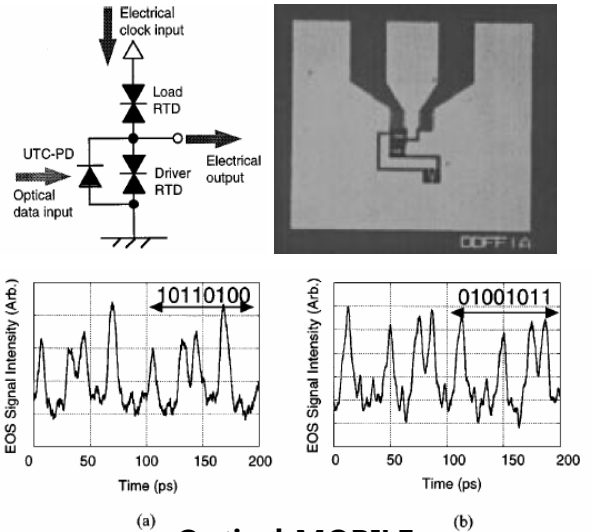
[Multi-valued quantizer circuits]



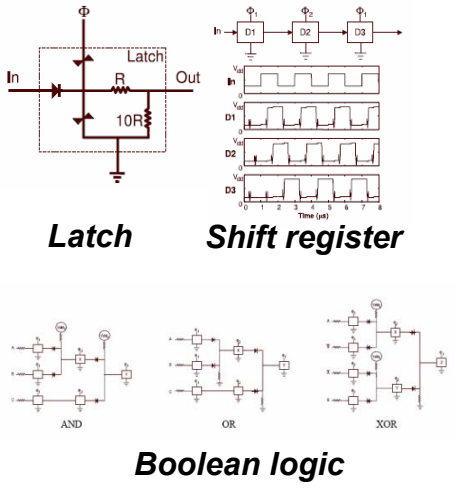
[Threshold logic gates]

MOBILE for High-speed/Low-power Digital ICs (2)

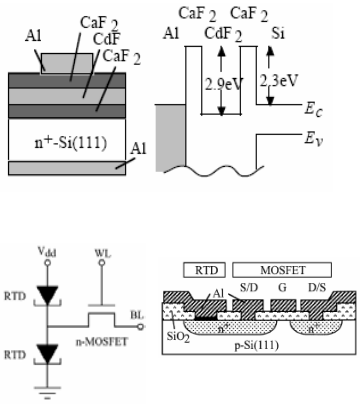
- MOBILE for high-speed optical communications
  - 80 Gb/s operation with 7.68 mW power dissipation using UTC-PD
- MOBILE using molecular RTDs
  - Latch, shift register, Boolean logic, and memory array have been proposed
- Co-integration of RTDs with CMOS
  - SRAM memory cell was demonstrated
  - InP-based RTD on Si substrate was demonstrated



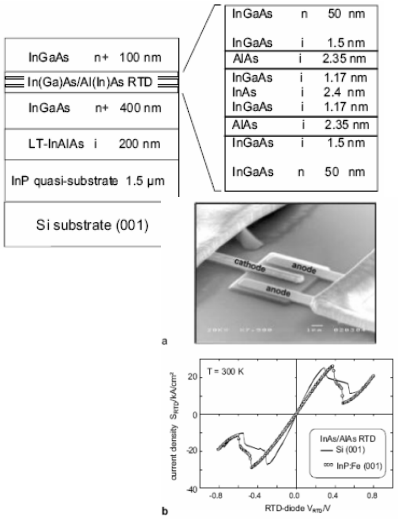
Optical MOBILE
(H. Matsuzaki et al., IEEE JSSC, 2001)



Molecular MOBILE
(H. Matsuzaki et al., IEEE ISSCC, 2002)



Fluoride RTD on Si
(T. Terayama et al., JJAP, 2002)



InP RTD on Si
(W. Prost et al., ESSDERC, 2005)

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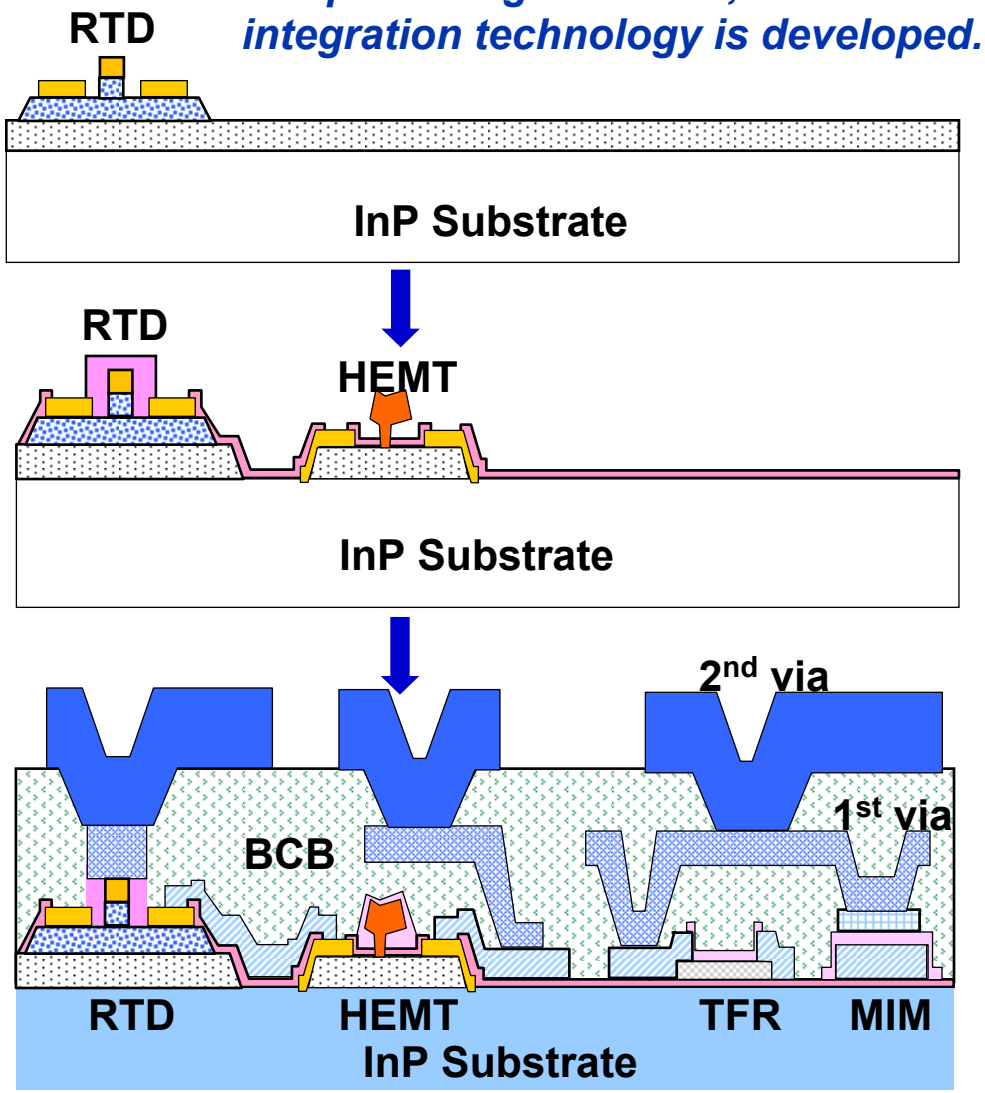
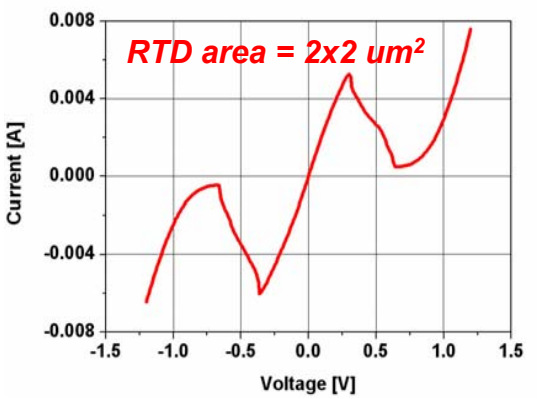
Process for InGaAs RTD + 0.1μm HEMT Integration

- *To fabricate RTD-based high-speed and low-power logic circuits, RTD/HEMT integration technology is developed.*



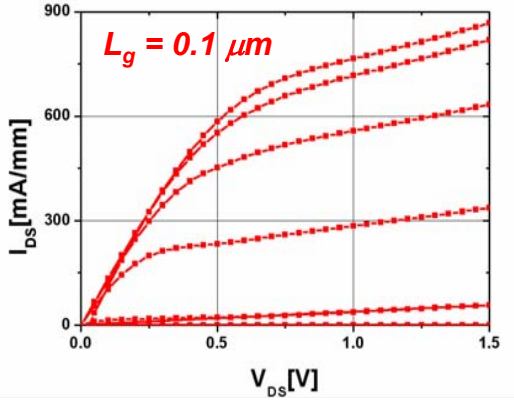
< RTD I-V curves >



- *Peak Current Density (J_P) = 112 kA/cm²*
- *Peak voltage (V_P) = 0.3 V, PVCR = 12*

◆ RTD demonstrated harmonic oscillation of > 1 THz. (TIT, 2008)

< HEMT I-V curves >



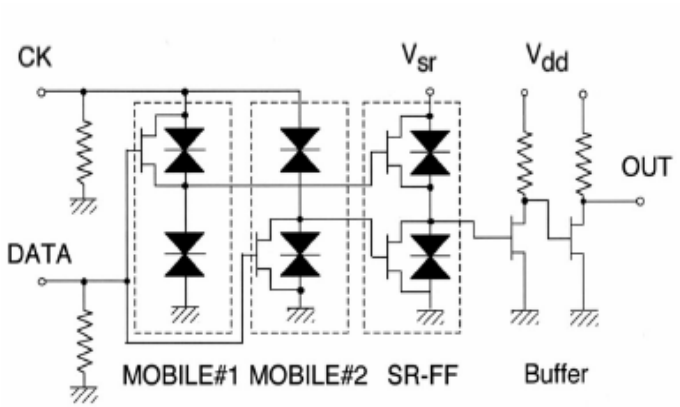
-- *Gm = 1.2 S/mm, f_T=220 GHz*

◆ 15nm HEMT with f_T of 610GHz. (SNU, 2007)

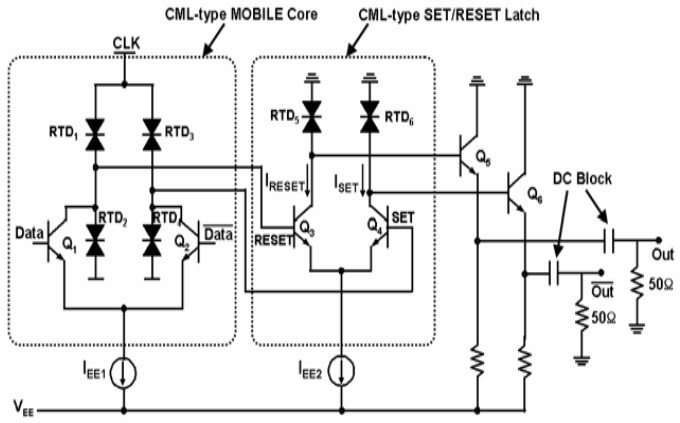
◆ 30nm HEMT of f_T, f_{max} > 500GHz. (MIT, 2008)

MOBILE-based NRZ D-F/F

- Limit of MOBILE
  - RZ-mode operation Incompatibility to conventional NRZ –mode logic circuit
- MOBILE-based NRZ D-F/F
  - Non-Return-to-Zero operation by combining original MOBILE with set/reset flip-flop



12.5 Gb/s with about 10mW power consumption (RTD/HEMT technology)



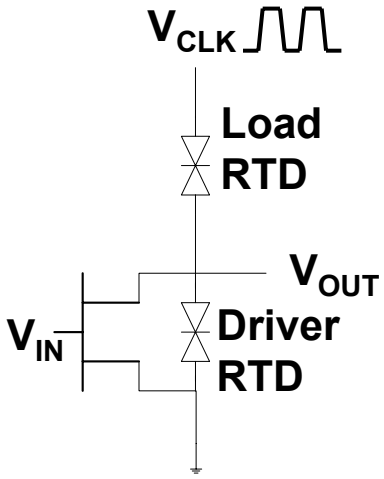
32 Gb/s with 45mW power consumption (RTD/HBT technology)

Large increase in circuit complexity & power consumption compared to original MOBILE

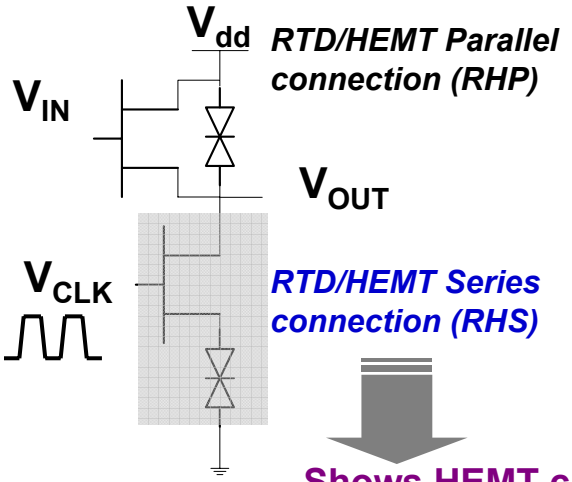
→ Need new circuit topology which inherits MOBILE's merits with NRZ mode operation

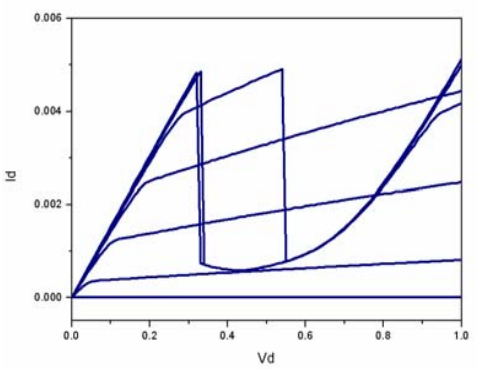
New NRZ-mode Logic Element Using RHS As Load

Conventional MOBILE configuration



A New RHS/RHP Logic Element

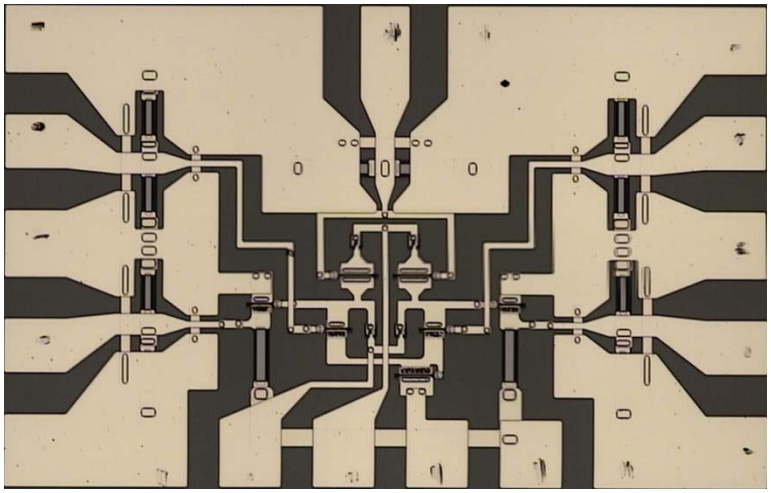




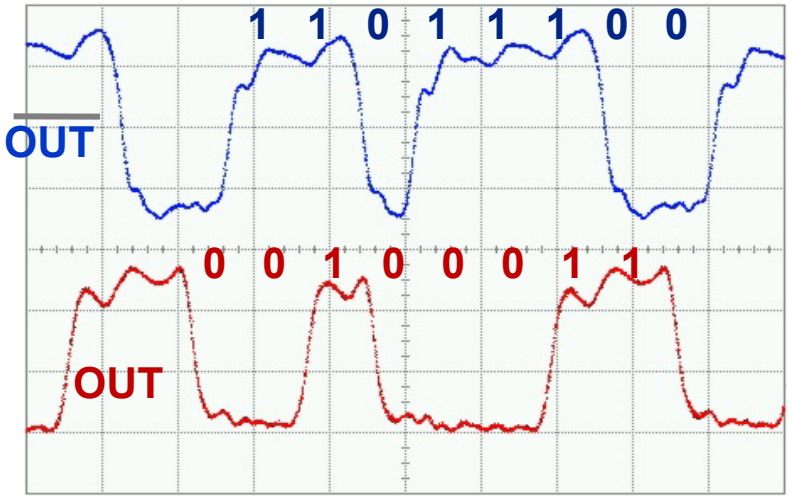
Shows HEMT characteristics and RTD characteristics according to gate bias

- **Advantages of Newly Proposed RHS/RHP Logic Element**
  - ✓ **High-speed and low-power operation**
  - ✓ **Reduced circuit complexity**
  - ✓ **Compatibility to the conventional digital ICs – NRZ-mode operation**
  - ✓ **Reduced clock loading**

Measurement Results



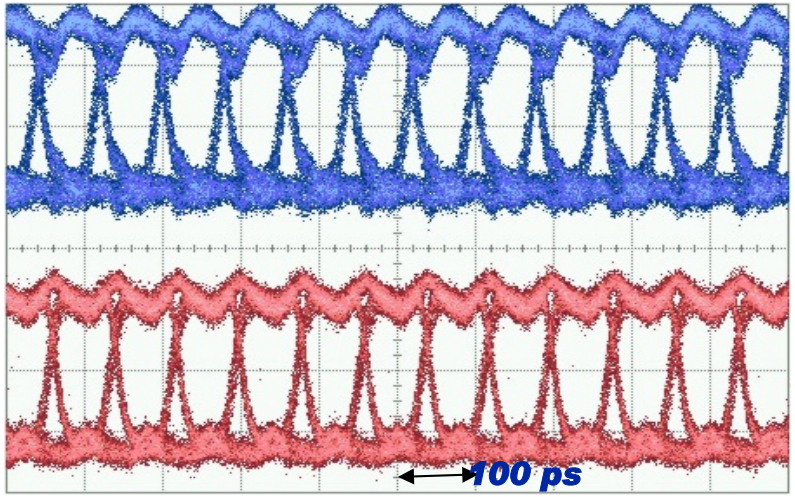
< Microphotograph of the fabricated IC >



< Measured output waveform at 12.5 Gb/s >

(Single)
- *Operating Speed : 36 Gbps*
- *Power Dissipation ~ 2.5 mW*
- *Device count : 4 (2 RTDs and 2 HEMTs)*

(Differential)
- *Operating Speed : > 12.5 Gbps*
- *Power Dissipation ~ 10 mW*
- *Device count : 9 (4 RTDs and 5 HEMTs)*



< Measured eye-diagram at 12.5 Gb/s >

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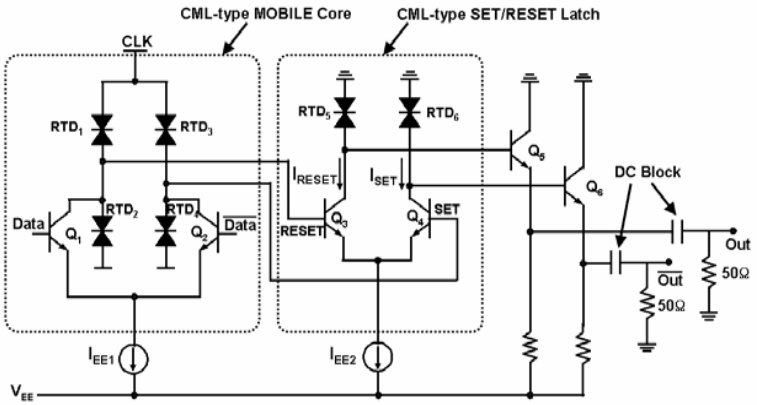
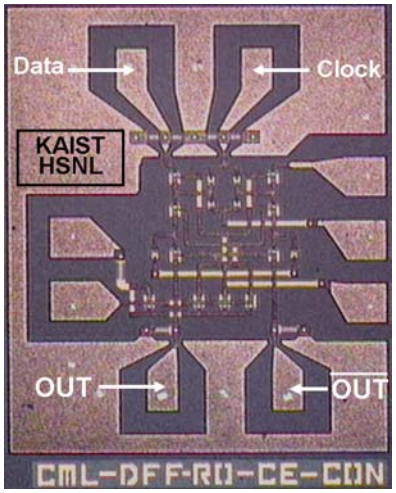
New CML-type RTD/HBT NRZ D-Flip Flop - KAIST

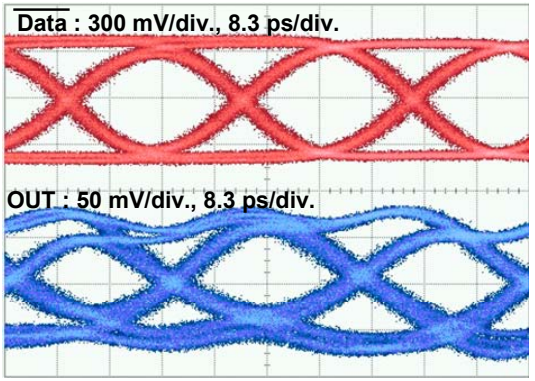
• Circuit Diagram



• Micrograph of the fabricated NRZ D-Flip Flop

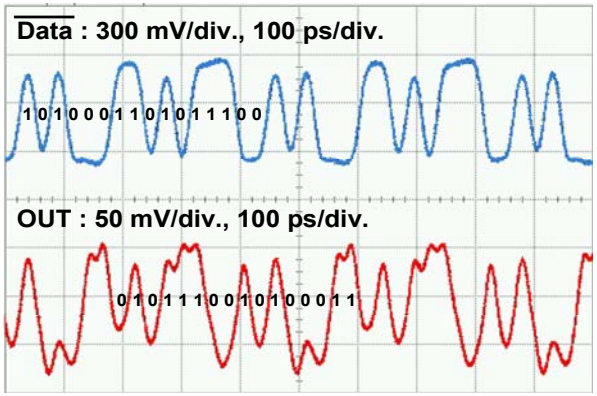


•Eye-diagram result at 36 Gb/s



• Measurement result at 38 Gb/s

- Input=1010110011001010



- For the first time, the CML-type RTD/HBT NRZ D-Flip Flop with differential output has been proposed and fabricated.
- Operating Speed : 36 Gb/s, Output swing : 125 mV_{P-P}
- Power Dissipation in Core : 20 mW

  cf.) Conv. HBT D-FF : 0.5~1.0 W

  RTD/HEMT NRZ D-Flip Flop : 12.5 Gb/s (NTT)

(2007, EL)

In this work, the CML –Type RTD/HBT based High-Speed/Low-Power NRZ D-Flip Flop with differential output has been developed.

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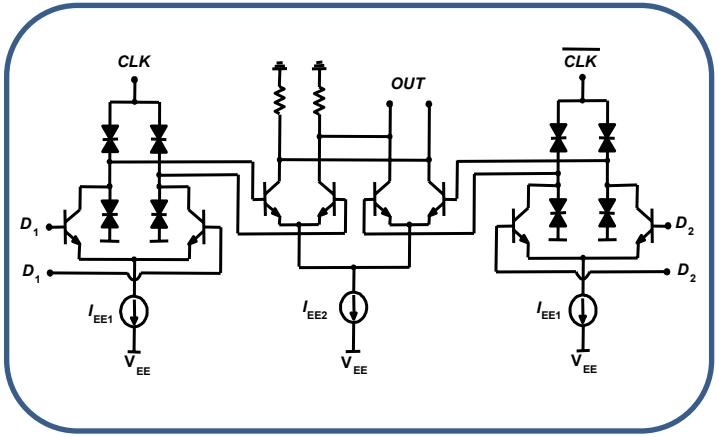
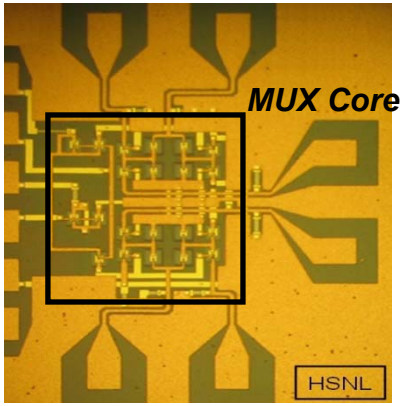
Measurement Results of Multiplexer - KAIST

• Circuit Diagram of MUX IC core

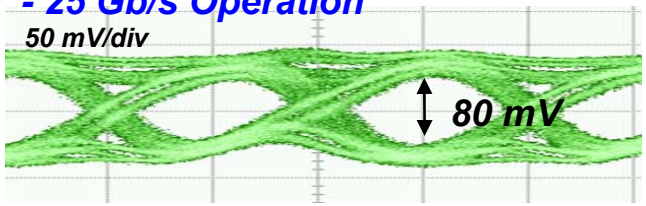


• Microphotograph of the fabricated 2:1 MUX IC

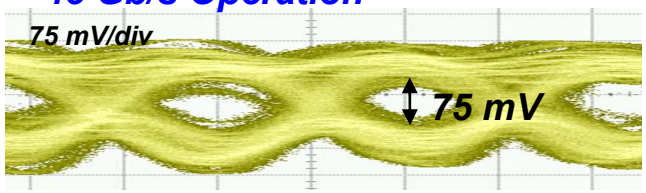


• Eye-diagram results

- 25 Gb/s Operation

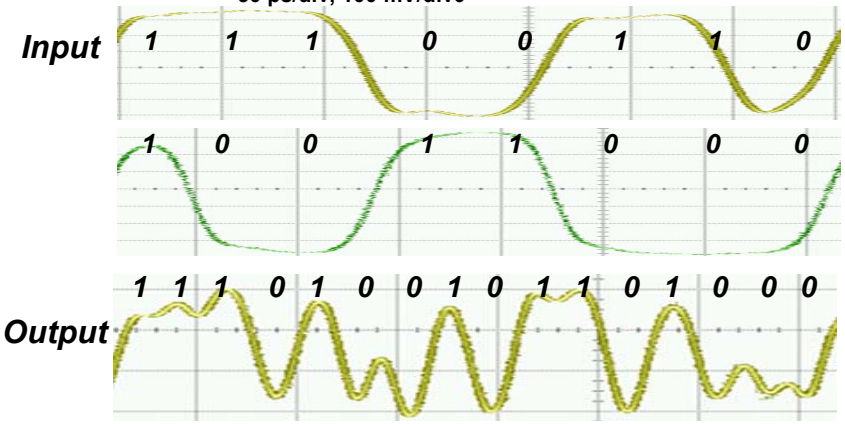


- 45 Gb/s Operation



• Measurement results (@ 45 Gb/s)

- DATA 50 ps/div, 100 mV/div0



- Operating Speed : 45 Gb/s, Output eye opening: 60 mV_{P-P}
- Power Dissipation in Core : 22.5 mW

cf.) Conv. CMOS & HBT MUX : > 100 mW

- MUX. IC fabricated by KAIST HSNL's process technology
- Test system set in the KAIST HSNL

⇒ Confirmed operation speed at 45 Gb/s

(2008, IEEE Nano Conference)

For the first time, the CML-type RTD/HBT based 2:1 Multiplexer has been developed.

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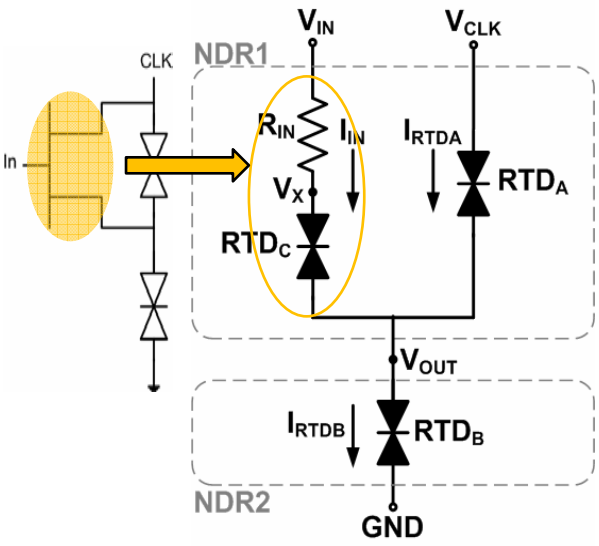
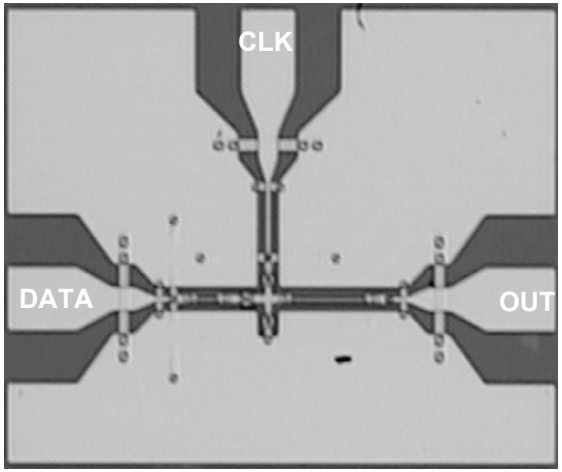
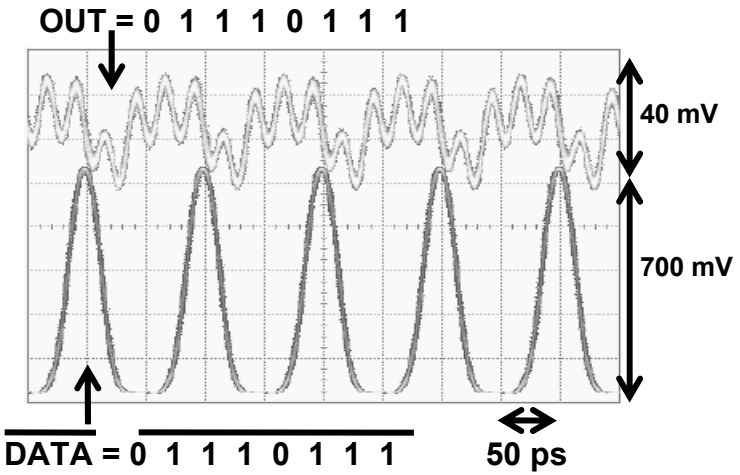
RZ MOBILE using only RTDs as active devices



[Circuit configuration]



[Microphotograph of MOBILE]

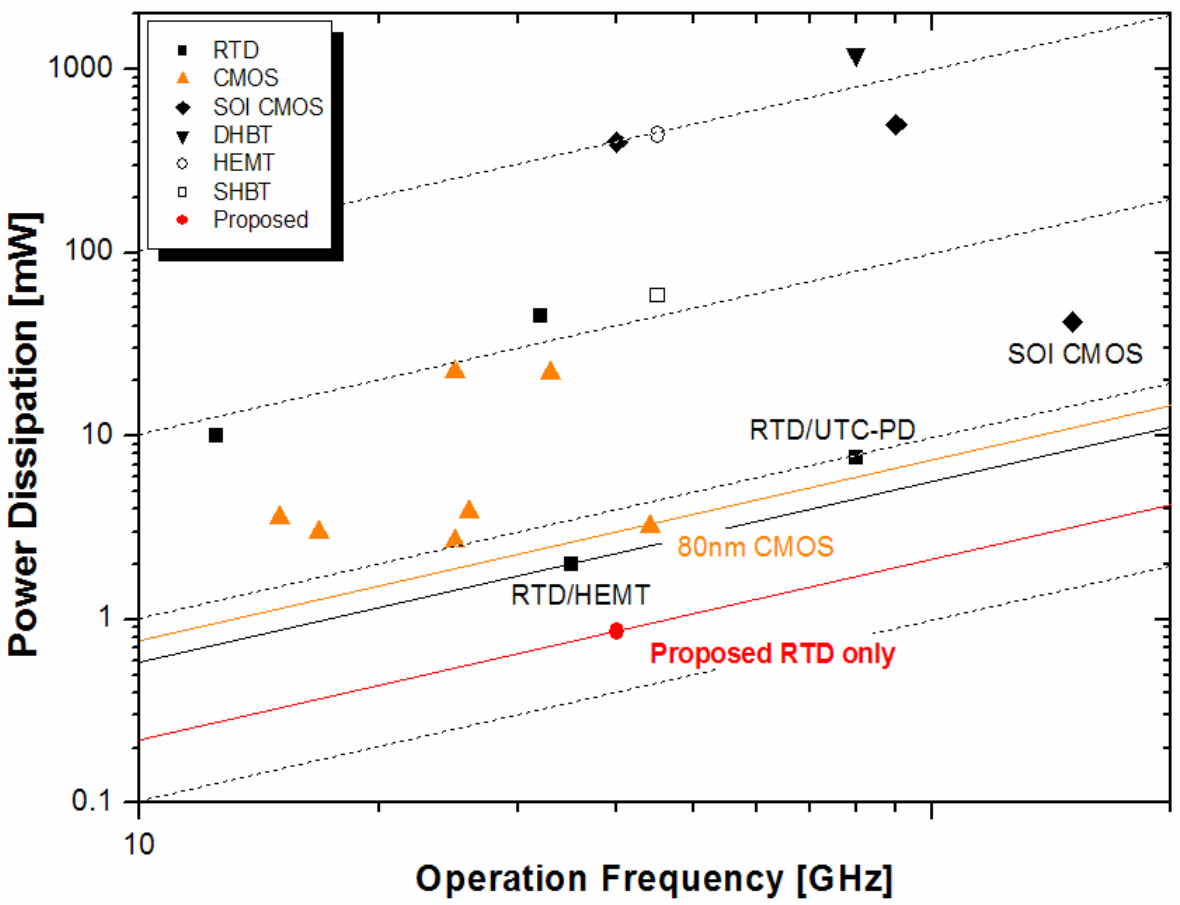


[Measurement result at 40 Gbps]

- *To fully exploit high-speed/low-power characteristics of RTDs, MOBILE using only RTDs is designed and demonstrated up to 40 Gbps with very low-power dissipation about 0.86 mW*
- *Minimum power-delay product of about 22 fJ was obtained by considering AC current effect of MOBILE and designing MOBILE using only RTDs without TRs*

Cf.) 42 fJ using RTD/Schottky diode, 48 fJ using RTD/HEMT, and 96 fJ using RTD/UTC-PD

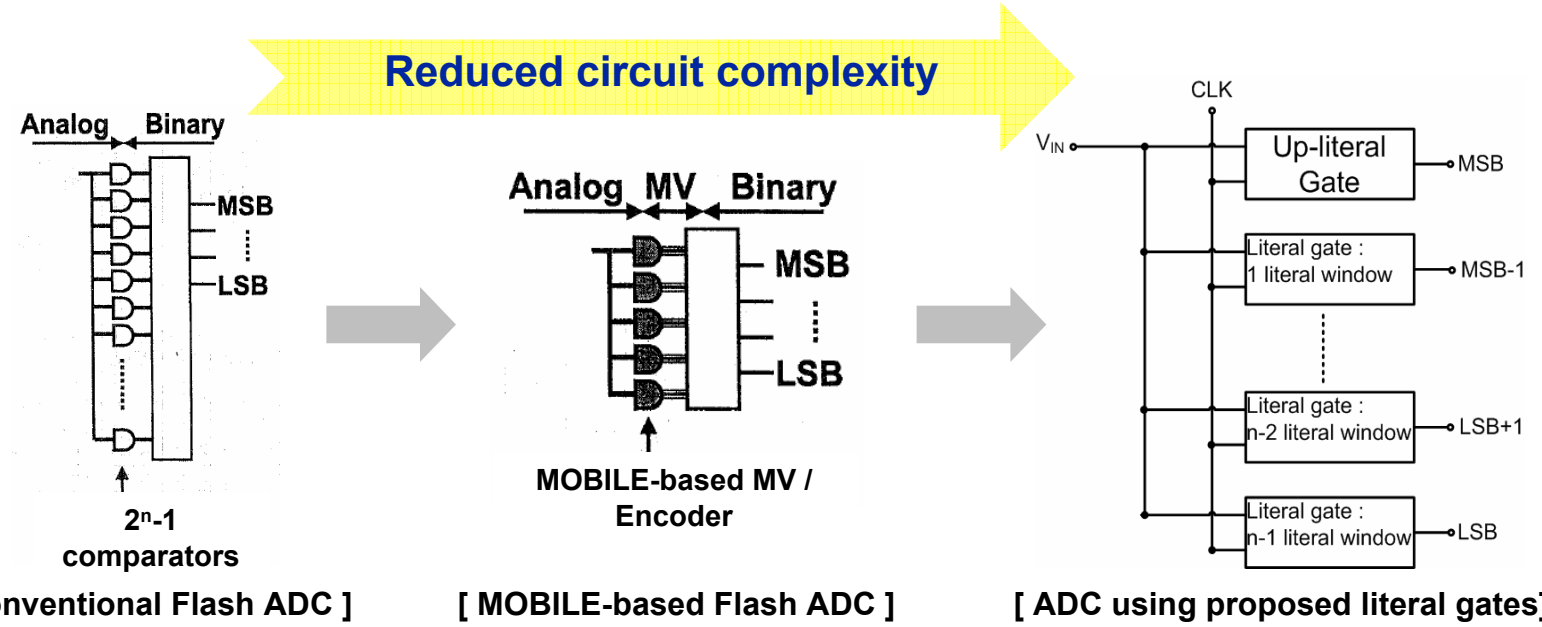
Comparison of D-F/F Performance



- ***Minimum power-delay product of about 22 fJ was obtained by considering AC current effect of MOBILE and designing MOBILE using only RTDs without TRs***

Ref.) 42 fJ using RTD/Schottky diode, 48 fJ using RTD/HEMT, and 96 fJ using RTD/UTC-PD

Flash ADC using MOBILE-based MVL

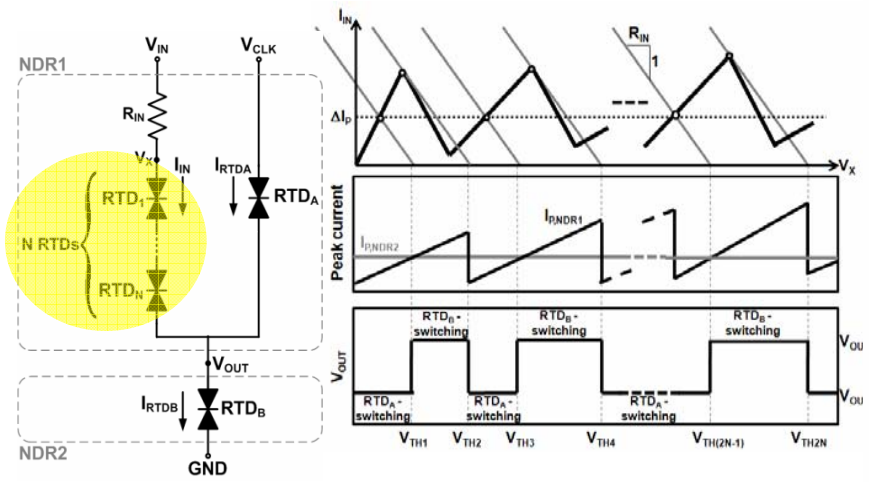


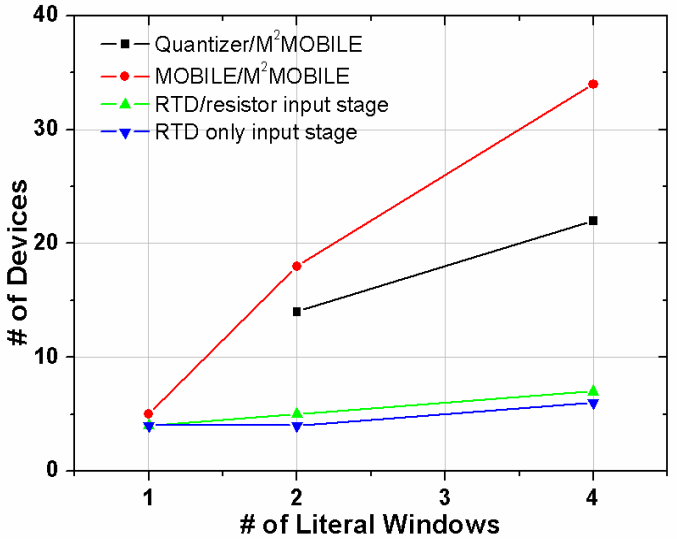
[Conventional Flash ADC] [MOBILE-based Flash ADC] [ADC using proposed literal gates]

- Flash ADC is the fastest ADC topology
  - Limit of resolution bit due to device count (2^n-1)
- Using RTDs, device count can be reduced
  - 2-stage operation
  - Increase in circuit complexity due to encoding circuit
- Using the proposed literal gates, ADC can be implemented more compactly
  - 1-stage operation with n literal gates

Universal Literal Gate Based on Proposed MOBILE

Nonlinear foldback I-V characteristics + multi-peak I-V characteristics





[Circuit configuration of the proposed universal literal gate]

[Comparison of literal gates]

- Previously reported MOBILE-based logic circuits utilize NDR characteristics and multi-peak characteristics for the switching

  → Need increased circuit complexity to implement complex functions

- Universal literal gate based on the proposed MOBILE can be implemented using simple circuit configuration by utilizing NDR characteristics and multi-peak characteristics for both switching and current modulation

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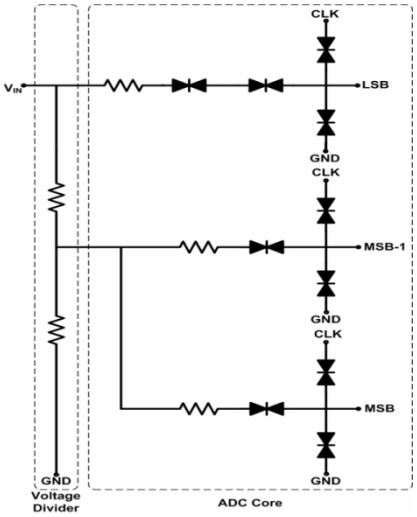
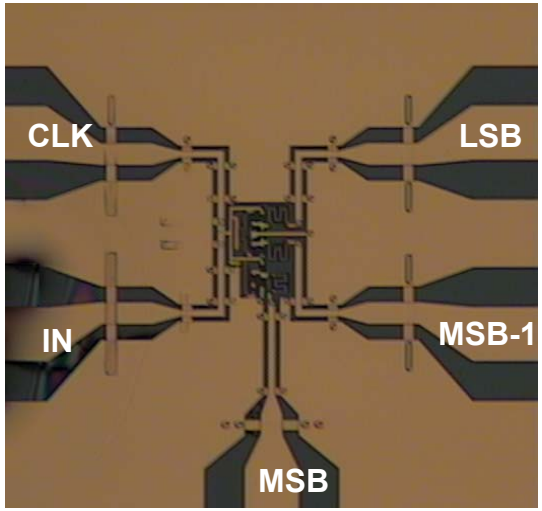
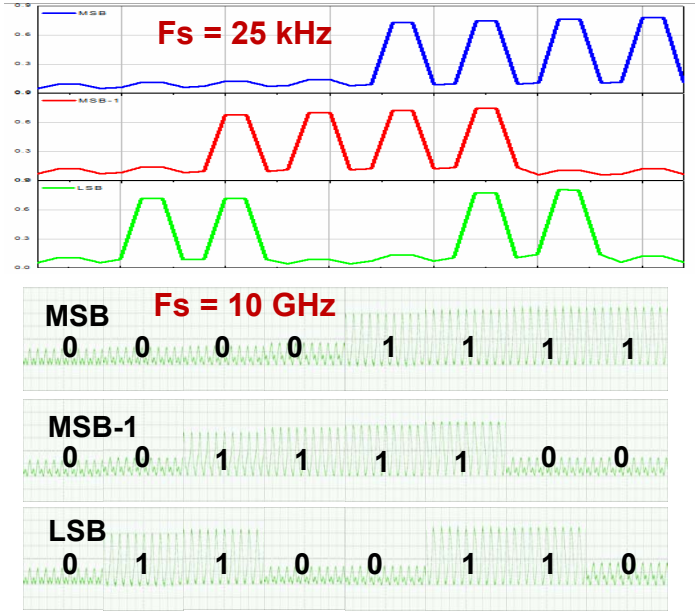
3-bit Flash ADC Using Proposed Universal Literal Gate



[Circuit configuration]



[Microphotograph of the fabricated Circuit]



[Measured output waveform at low freq.]

- *3-bit flash ADC using only RTDs*
- *3-bit ADC was designed using the proposed MVL circuits using only RTDs*
  - *15 devices (10 RTDs and 5 resistors)*
  - *~ 5.2 mW power dissipation (core circuit)*

- ***Designed flash ADC circuits exhibit advantages in terms of device count, circuit complexity and power dissipation with respect to the previously reported circuit.***

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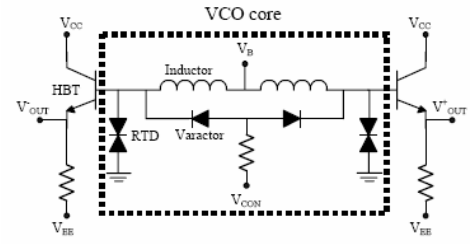
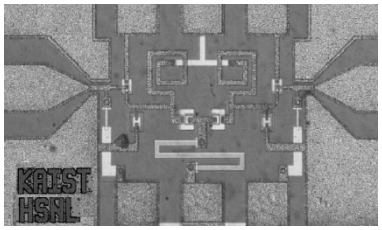
K/Ka-band Differential-mode RTD/HBT VCO - KAIST

• Schematic of the VCO



• Microphotograph

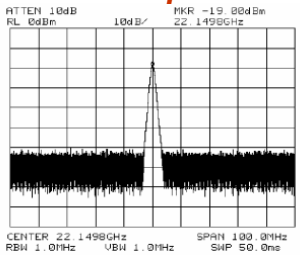


• Performances for the RTD/HBT VCO Core

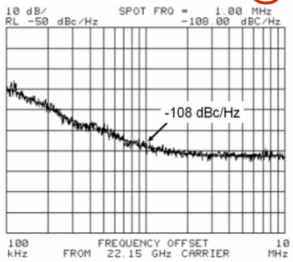
Parameters	Value (K-band)	Value (Ka-band)
Supply Voltage	0.34 V	0.42 V
Bias Current	2.97 mA	1.5 mA
DC Power Consumption	1.01 mW	0.63 mW
Center Frequency	22.2 GHz	34.15 GHz
Tuning-range	2.07 GHz	3.1 GHz
Max. Output Power	-19 dBm	-22.8 dBm
Phase Noise @1 MHz	-108 dBc/Hz	-102.3 dBc/Hz
F.O.M.	-195 dBc/Hz	-195 dBc/Hz

K-band VCO

- **Measured Output spectrum**
  - *Center freq.=22.15 GHz*

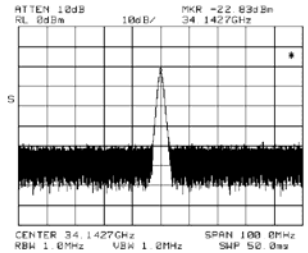


- **Measured phase noise**
  - *PN = -108 dBc/Hz @ 1MHz*

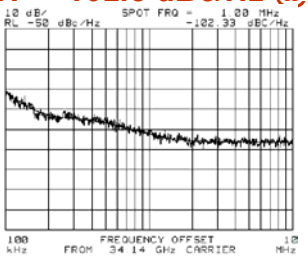


Ka-band VCO

- **Measured Output spectrum**
  - *Center freq.=34.15 GHz*



- **Measured phase noise**
  - *PN = -102.3 dBc/Hz @ 1MHz*

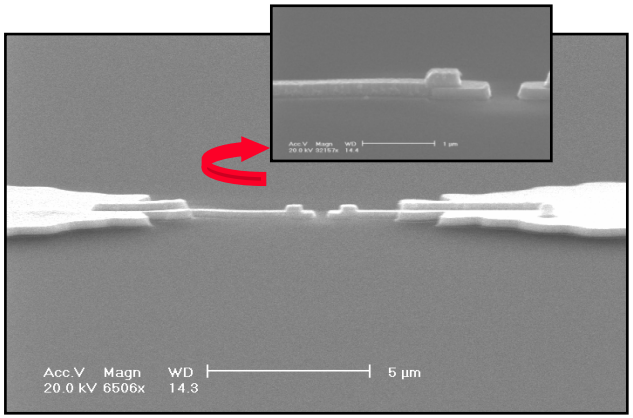


- *A K/Ka-band differential mode RTD VCO is developed*

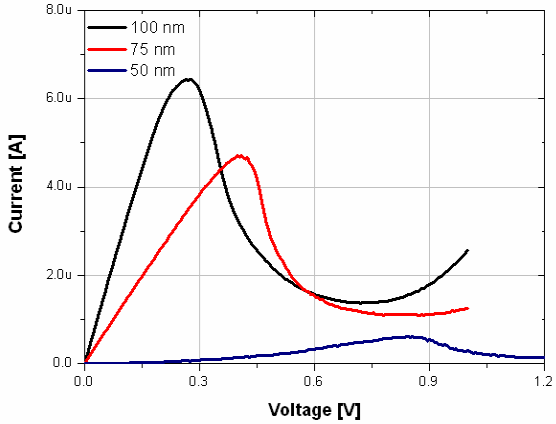
In this work, the RTD/HBT based Differential-mode VCO has been developed

21 Frontier R&D Program

Nano-scale RTD Fabrication – Dry etching

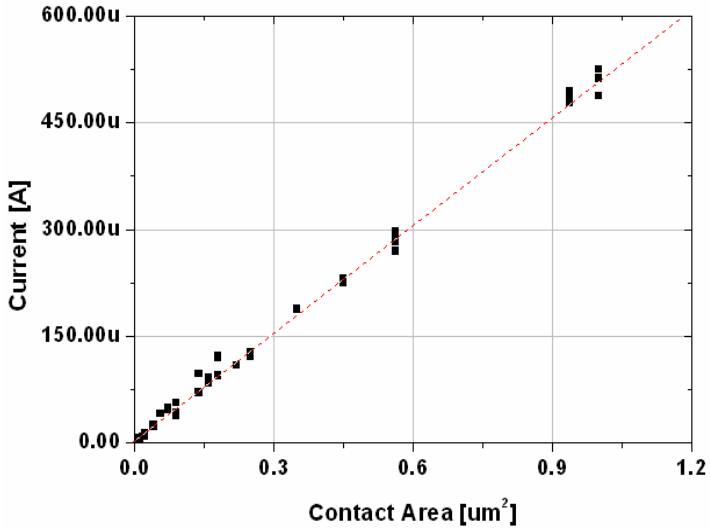


- *ICP dry etching*
- *Remote ICP SiN passivation*
- *BCB etchback*

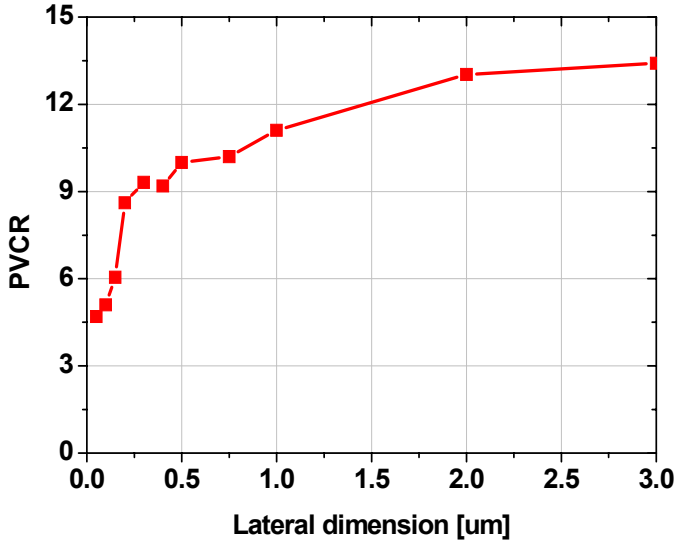


[SEM image of the fabricated nano-scale RTD]

[I-V characteristics of RTD of 50 x 50 nm^2]



[Peak current v.s. lateral scale]

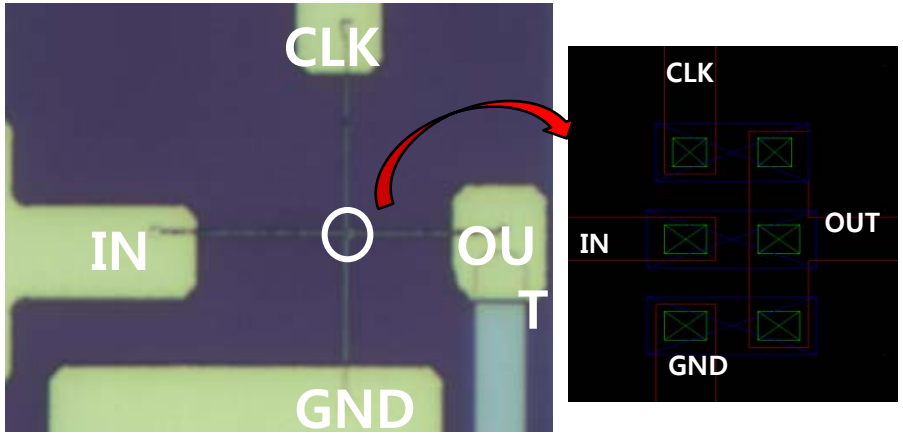


[PVCR v.s lateral scale]

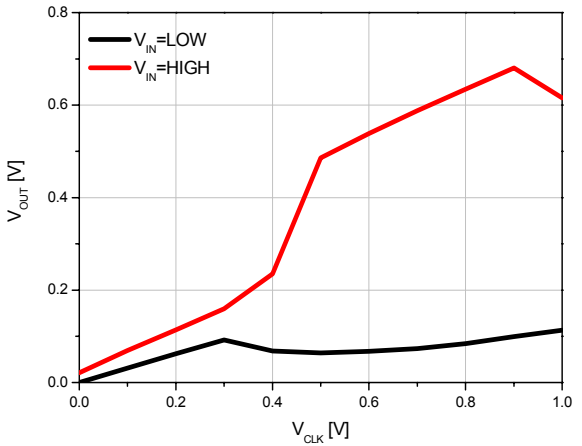
- *RTD with lateral scale of up to 50 nm has been fabricated*
- *Peak current = 0.6 uA, PVCR ~ 4.7*

21 Frontier R&D Program

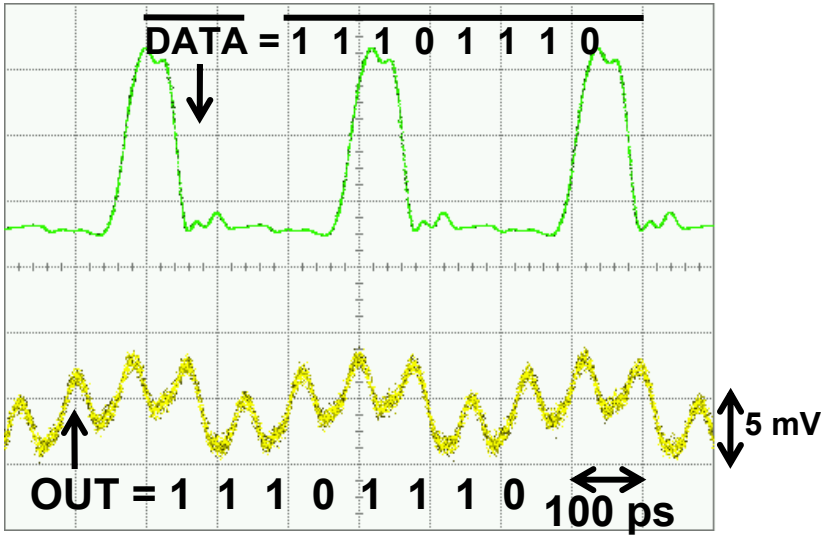
MOBILE using Nano-scale RTDs



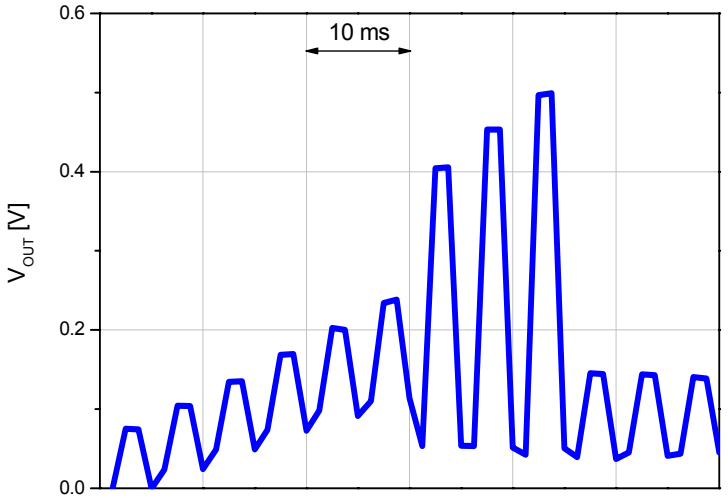
[Microphotograph of the fabricated MOBILE]



[DC transfer characteristics of MOBILE]



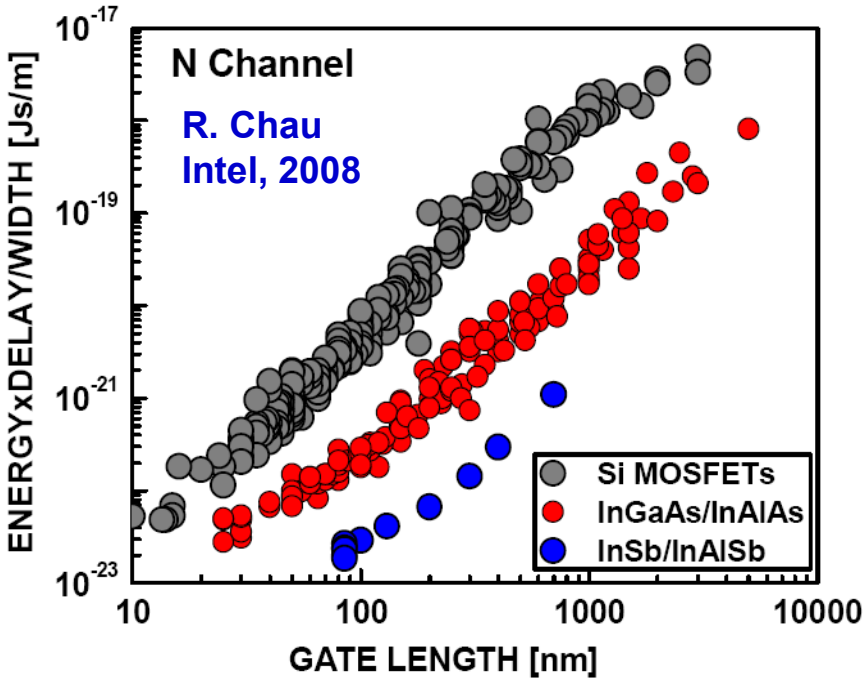
[12.5 Gbps operation]



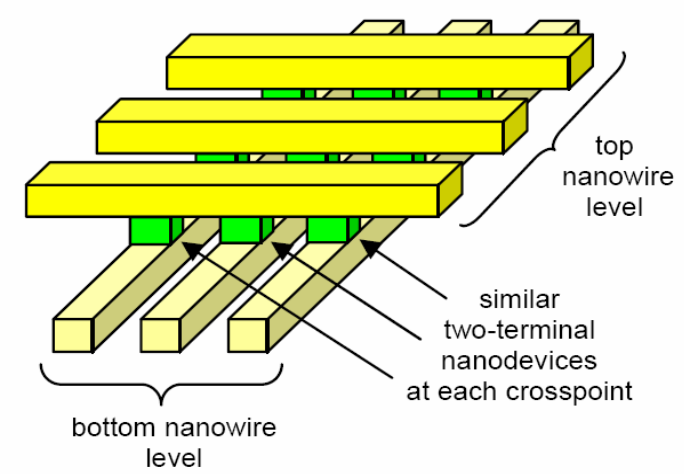
[Literal gate operation]

- *MOBILE operation and MVL operation using 200 nm-scale RTDs were confirmed*
- *Core size : 0.8x1.4 μm^2, Measured DC power dissipation ~ 6.6 μW*

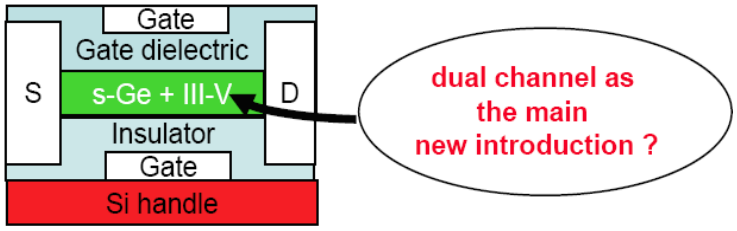
Potential of III-V Devices for more than Moore (I)

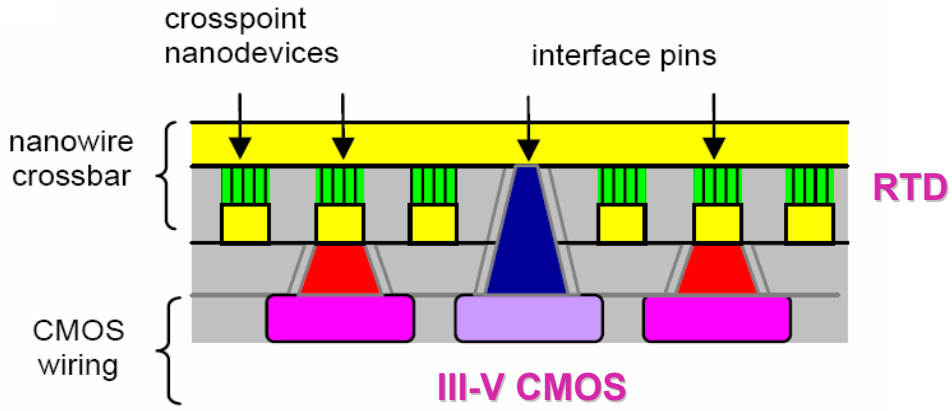


Likharev's CMOL
(Hybrid CMOS/Nanoelectronic IC)



Sub-22 nm node





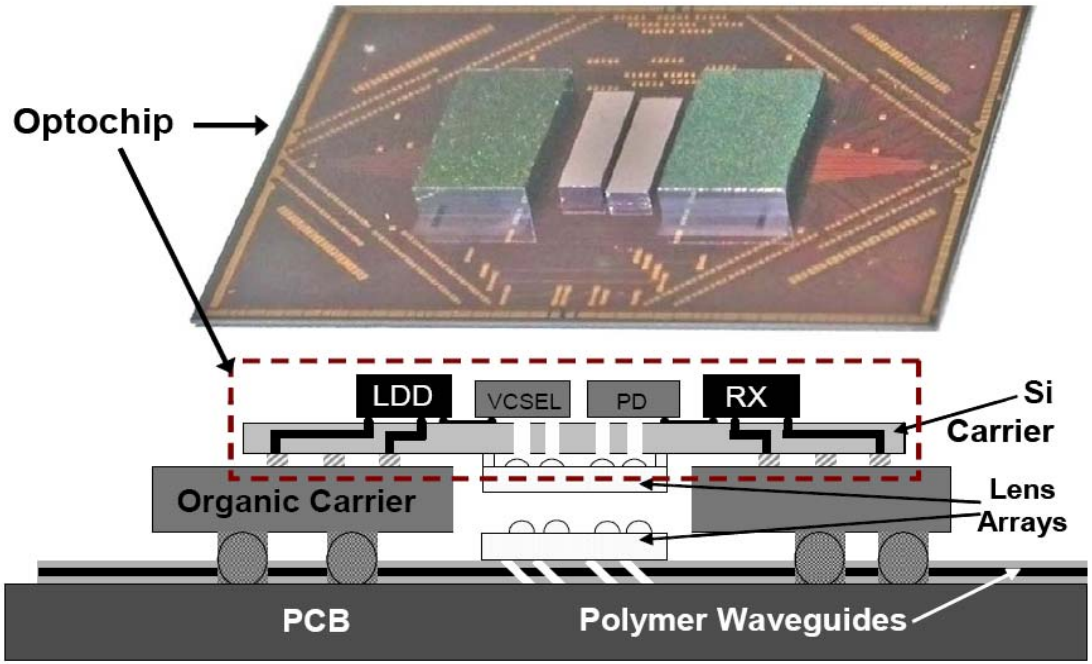
Target of EU's DUALLOGIC Project
- Next Generation CMOS

21 Frontier R&D Program

Potential of III-V Devices for more than Moore (II)

Optical Interconnect

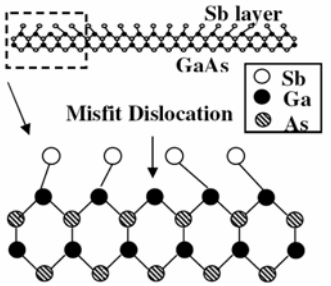
(F. E. Doany, IBM, 2008)



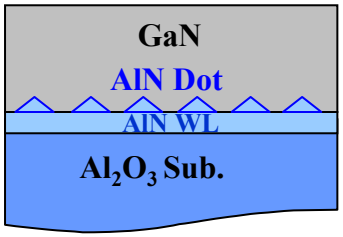
Module-based 300Gb/s optical interconnect

(300Gb/s ; 12.5Gb/s x 24channel)

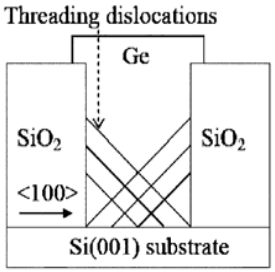
◆ Periodic IMF array



◆ QD Dislocation Filtering



◆ Growth on Structured Substrate



III-V on Si & III-V Devices

◆ Wafer Bonding

◆ SoP Integration

> Tb/s Optical Interconnect

* More functionalities with III-N materials

- High power & high temperature
- Wide optical spectrum
- Thermoelectricity & Piezoelectricity

21 Frontier
R&D Program

Summary

- RTD-based high-speed and low-power circuits with reduced circuit complexity are designed and demonstrated
  - 36 Gbps operation of NRZ-mode logic element using only 2 HEMTs and 2 RTDs
  - 40 Gbps operation of RTD-only MOBILE with power-delay product of 22 fJ.
  - 3-bit ADC circuit with reduced circuit complexity (using only 15 devices) based on the newly proposed universal literal gate.
  - 45 Gbps, 22.5mW operation of RTD/HBT CML-type 2:1 Multiplexer
- Nano-scale RTD fabrication was demonstrated.
  - To fabricate nano-scale RTD, quasi-planar fabrication process with low-damage dry etching is developed.
  - 50 nm scale RTD with high PVCR of 4.7 was successfully demonstrated.
  - MOBILE operation and MVL operation using 200 nm-scale RTDs were confirmed.
- Advanced process techniques such as neutral beam etching, MOS-like passivation or selective epitaxy are necessary for nano-scale RTD ICs.
- RTDs' are still promising for high speed & low power nanoscale ICs.

Thank You for Your Attention !

Any Questions ?