Ultimately Scaled CMOS: DG FinFETs?

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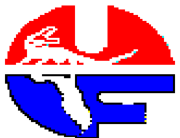


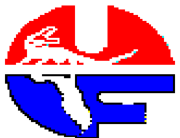
Outline

* Introduction - CMOS Scaling
* Thin-BOX FD/SOI MOSFETs
* *Pragmatic* Nanoscale FinFETs
* Conclusions

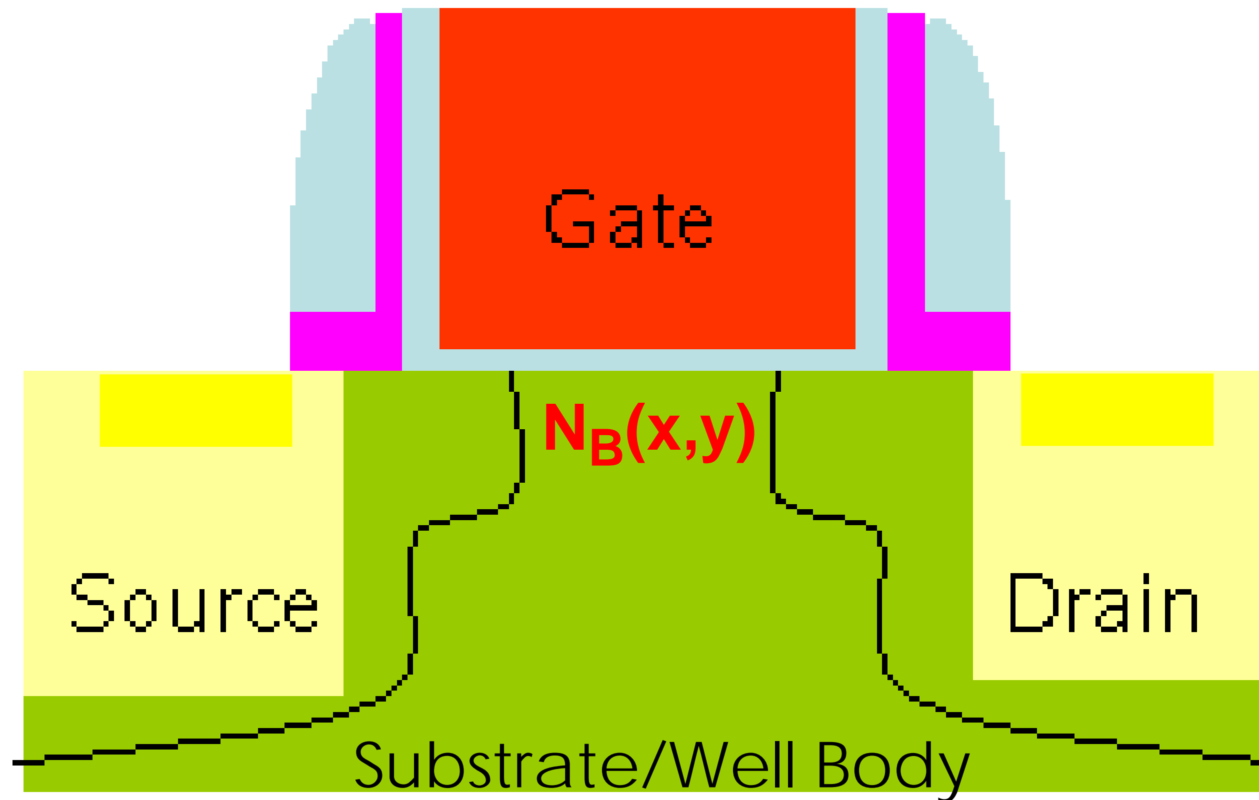
Projected HP CMOS Gate-Length Scaling*

INTERNATIONAL SEMATECH

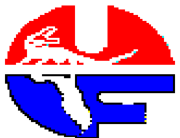
*2003 SIA ITRS



Contemporary Bulk-Silicon MOSFET

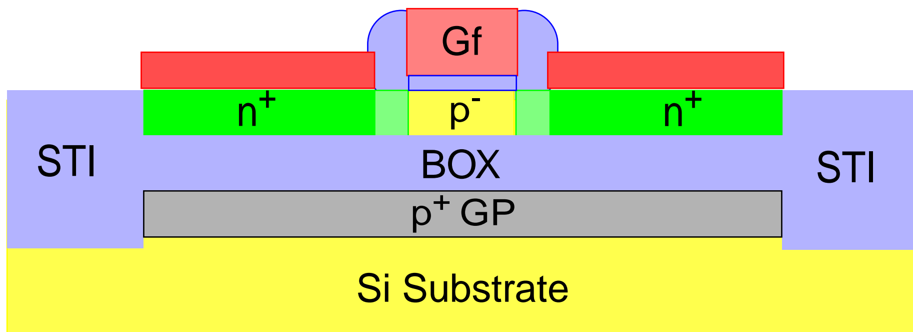


Has been scaled a la Moore's (and now, "More than Moore") Law, but with increasingly complex boosters and body/channel doping density N_B, which can no longer (i.e., for $L_g <$ ~30nm) be adequately controlled.



Continued Scaling to L_g < 10nm: Undoped UTBs/Channels

FD/SOI (n)MOSFET w/ thin BOX and GP?



NO.

Complex processing/layout.

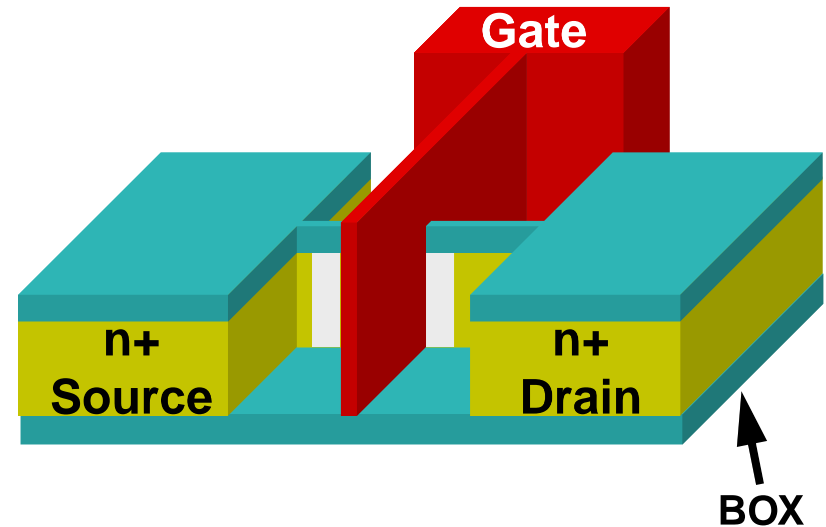
Selective GPs, w/ biasing.

Tuned dual-metal gate work functions.

High inherent V_t:

$$V_{t(long)} = (1 + r)\phi_c \sim 0.6V .$$

(n)FinFET on SOI?



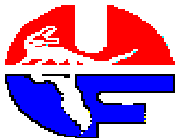
YES.

Quasi-planar.

Conventional processing, w/o N_B.

Two gates: good SCE control.

Can be pragmatic.



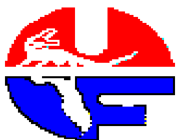
2-D Numerical Simulations: Projected Scaling Limits

Taurus-predicted LP and HP scaling limits (L_{eff}, which, with G-S/D underlap, can be 5-10nm longer than L_g), defined by t_{Si} = 5nm, for thin-BOX/GP nMOSFETs and DG nFinFETs. The devices have been designed for I_{off} ~ 10pA/µm and ~100nA/µm for LP and HP applications, respectively, with DIBL ≤ 100mV/V. The 18nm limit for the HP thin-BOX/GP device with V_{GP} is questionable due to the very large $\Delta\Phi_{Gf}$ (gate work-function tuning below midgap) needed; the scaling limit of 25nm without V_{GP} is more realistic.

LP	Thin-BOX/GP w/o V_{GP}	Thin-BOX/GP w/ V_{GP}	DG FinFET
L_{eff} (nm)	28	**18**	25/**15**
$\Delta\Phi_{Gf}$ (mV)	0	450	0/-450

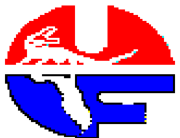
HP	Thin-BOX/GP w/o V_{GP}	Thin-BOX/GP w/ V_{GP}	DG FinFET
L_{eff} (nm)	**25**	18?	**15**
$\Delta\Phi_{Gf}$ (mV)	0	850	0

Pragmatic FinFET-CMOS can be scaled to the end of the SIA ITRS.



Nanoscale *Pragmatic-FinFET* CMOS

- ❋ On SOI (no isolation, S-D leakage complexities).
- ❋ Undoped fin-UTB/channel (no RDF effects).
- ❋ DG, not TG (a top gate is virtually ineffective).
- ❋ One ~midgap metal gate (for nMOS and pMOS).
- ❋ No channel strain (mobilities are high without it).
- ❋ No high-k dielectric (relatively thick SiON is OK).
- ❋ G-S/D underlap ($L_{eff(weak)} > L_g$, $L_{eff(strong)} \cong L_g$).
- ❋ S/D processing for V_t control (and underlap).

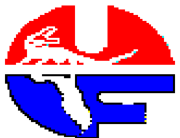


The optimal number of gates is 2!

Davinci (3-D): Undoped L_{eff} = 28nm TG fin size for SCE control; t_{ox} = 1.1nm

S = 80mV
DIBL = 100mV/V
$h_{Si} = w_{Si} = L_{eff}$
$h_{Si} = w_{Si}$ (⇒ easier fin)
DG
Design Space
FD/SOI
$1/5 \sim h_{Si(FD)}/L_{eff}$
$w_{Si(DG)}/L_{eff} \sim 1/2$
h_{Si}/L_{eff}
w_{Si}/L_{eff}
0.0
0.5
1.0
1.5
2.0

Two gates (DG) give good control of electrostatics (i.e., SCEs) with thicker UTB than that needed for one-gate (FD/SOI) device.



A third (top) gate is not very beneficial ...

Davinci (w/o QM): L_{eff} = 25nm, w_{Si} = 13nm, t_{ox} = 1.2nm

TG FinFET

DG FinFET

$R_f \equiv h_{Si}/w_{Si} = 3$

V_{DS}=1.0V

I_{DS} (μA)

V_{GS} (V)

0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1.0

0 10 20 30 40 50 60

$\Delta I_{on}/I_{on(DG)}$ (%)

W_{eff}-implied

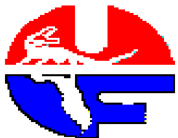
$[w_{Si}/(2h_{Si})]$

R_f

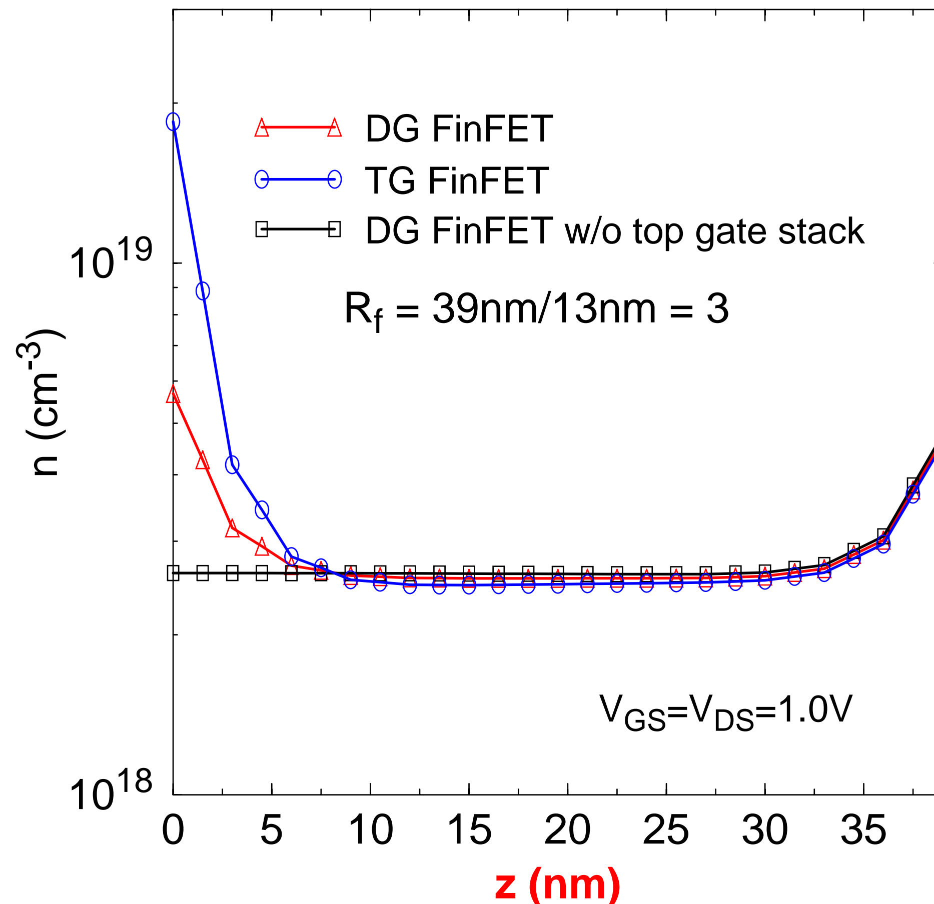
0.5 1.0 1.5 2.0 2.5 3.0 3.5 4.0 4.5 5.0 5.5

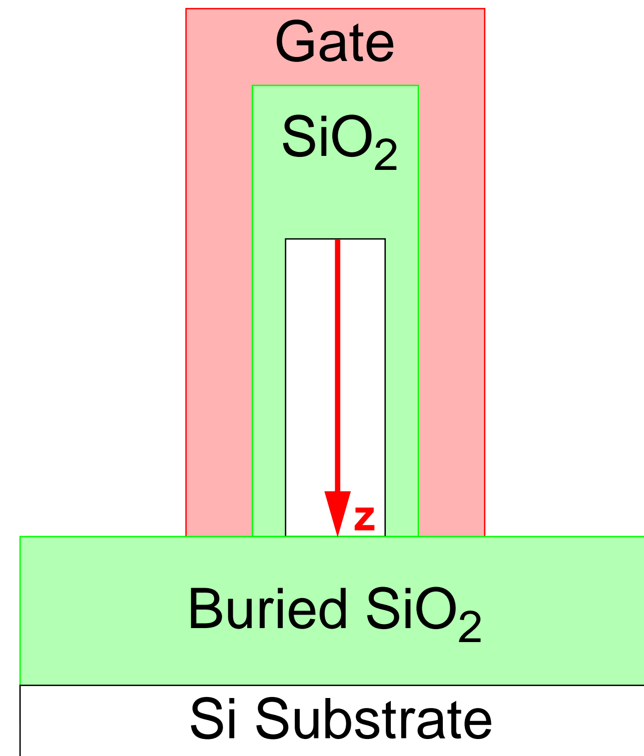
0 20 40 60 80 100

(Note that the effective width (per fin) $W_{eff} = 2h_{Si} + w_{Si}$ is not appropriate.)



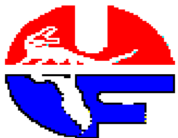
... due to *strong* bulk inversion in the undoped fin-UTB/channel.





The predicted electron density in the bulk of the undoped fin-UTB shows substantial (strong) inversion, irrespective of the top-surface condition.

Activating the third gate is not beneficial nor practical.



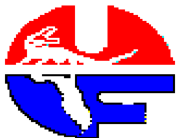
The bulk inversion also underlies the use of thick SiON.

- * Bulk (a.k.a. volume) inversion is not good, but is unavoidable.
- * For strong inversion, it reduces the effective gate capacitance C_G:

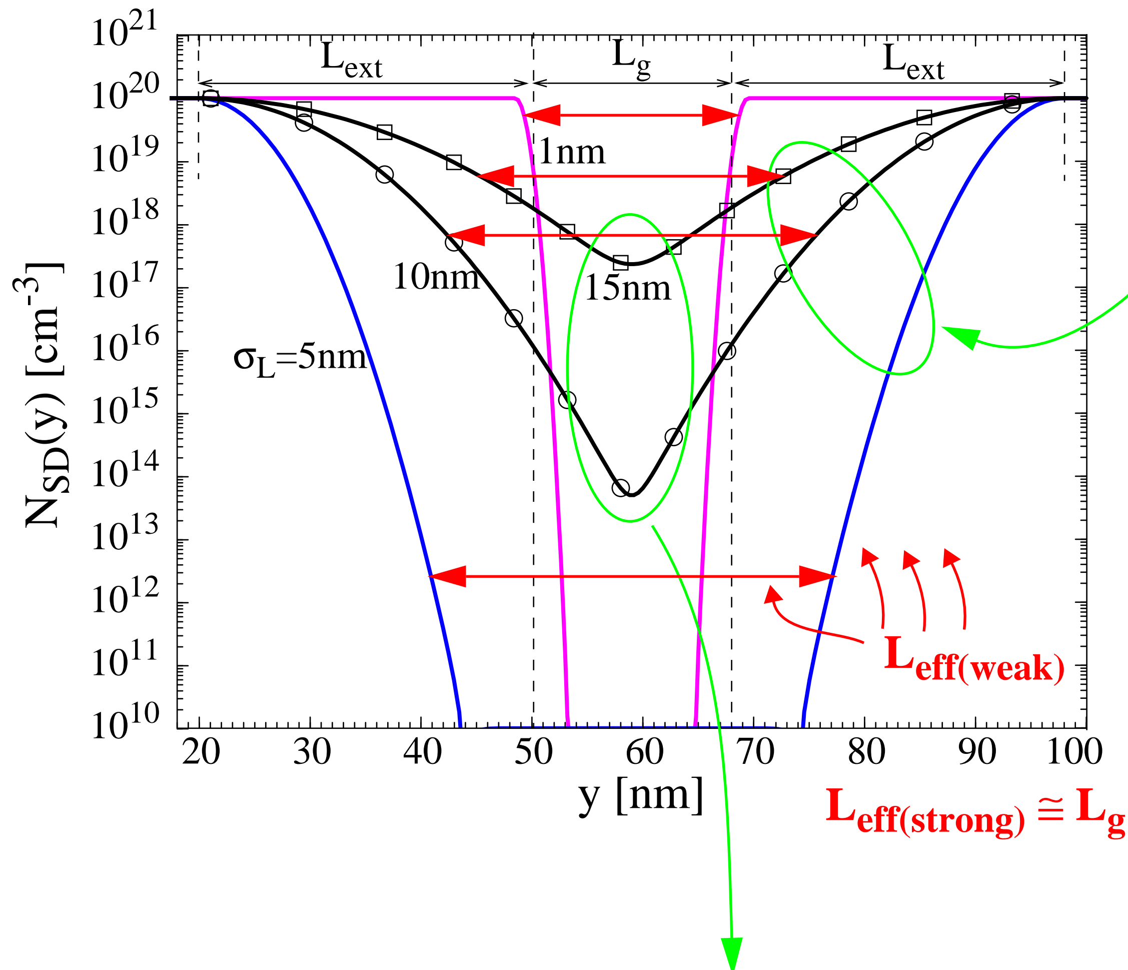
$$-Q_i = 2\left[\frac{C_{ox}}{1 + \frac{\varepsilon_{ox}\bar{x}_i}{\varepsilon_{Si}t_{ox}}}\right](V_{GS} - V_t)$$ (via integration of Poisson's equation)

  where $\bar{x}_i$ is the average depth(s) of the inversion carriers, which is increased by bulk inversion. The deeper $\bar{x}_i$ reflects lower inversion-layer capacitance, and yields lower C_G and Q_i.

- * The quantization effect further increases $\bar{x}_i$ and reduces C_G.
- * Because of the deeper $\bar{x}_i$, increasing t_{ox} is not so detrimental to C_G (which is less than $C_{ox} = \varepsilon_{ox}/t_{ox}$), and hence to Q_i and current.
- * Further, the thicker SiON (t_{ox}) reduces the parasitic G-S/D (fringe) capacitance, which improves speed performance significantly.



The underlap is effected by engineering of the lateral doping-density profile in the S/D fin-extension.



$$N_{SD}(y) \propto 10^{20} exp\left[-\left(\frac{y}{\sigma_L}\right)^2\right]$$

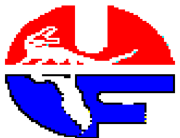
Medici:

L_g=18nm, L_{ext}=30nm, w_{Si}=12nm

σ_L [nm]	DIBL [mV/V]	S [mV]
1 (abrupt)	180	94
5	35	62
10	46	66
15	79	71

Straggle defines $L_{eff(weak)} > L_g$.

Optimal straggle and extension length define best SCE (I_{off}) vs. $R_{S/D}$ (I_{on}) tradeoff; further, V_t can be adjusted for different applications via controlled S/D dopants in channel, with reasonable sensitivity to process variations.

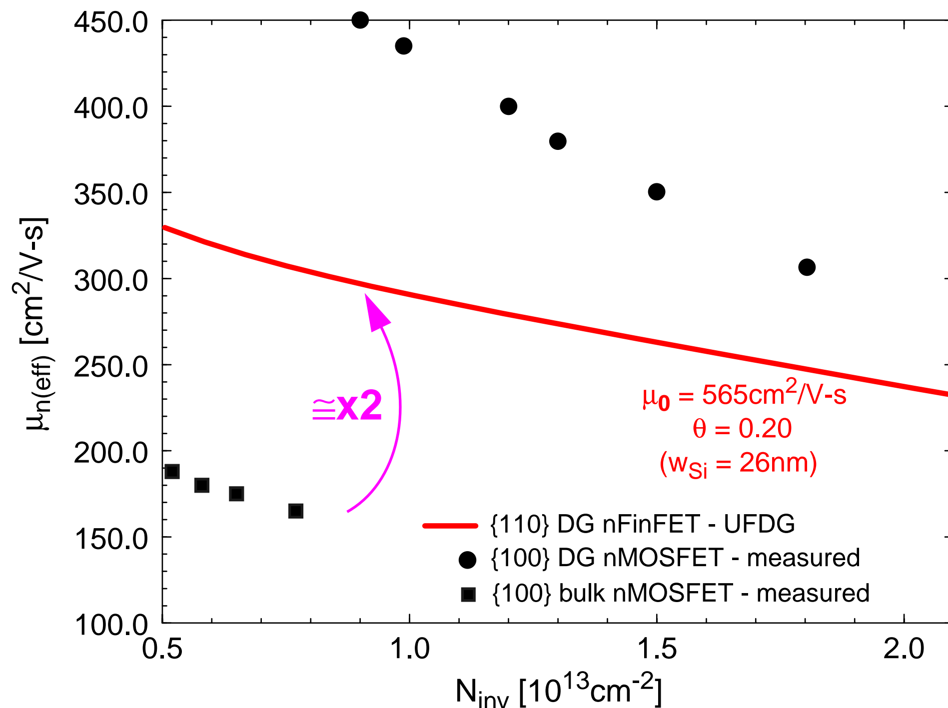


Very high mobilities can be achieved in undoped FinFETs.

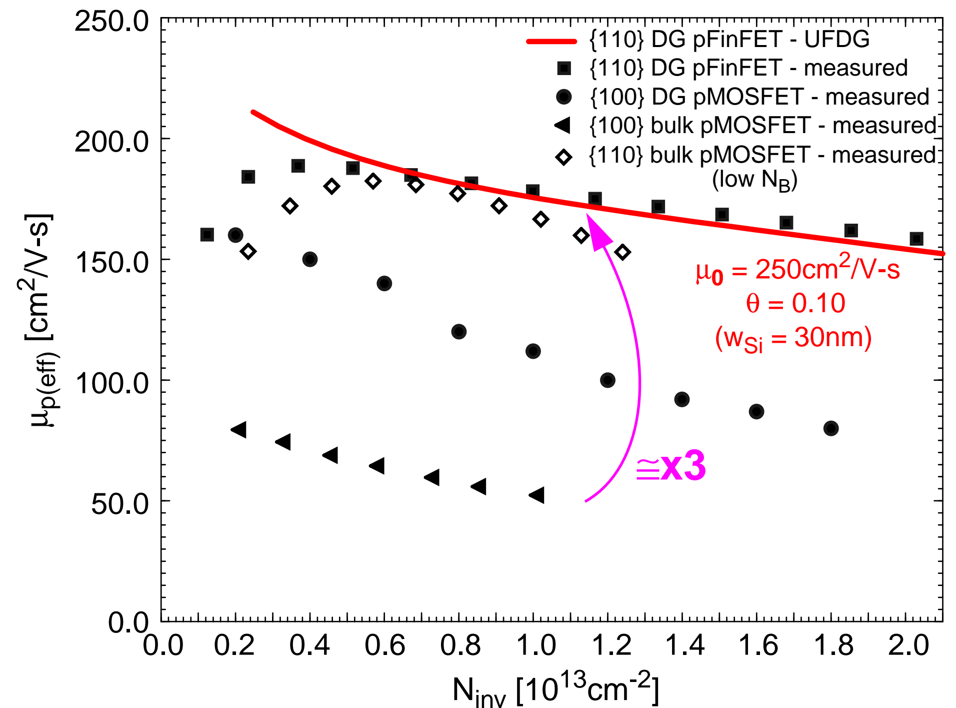
Low transverse electric field ($\Leftarrow Q_i/2$) yields high carrier mobilities:

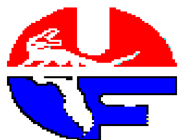
UFDG calibrations to long-L_g FinFETs

nMOSFETs ⇒ **electron mobilities**



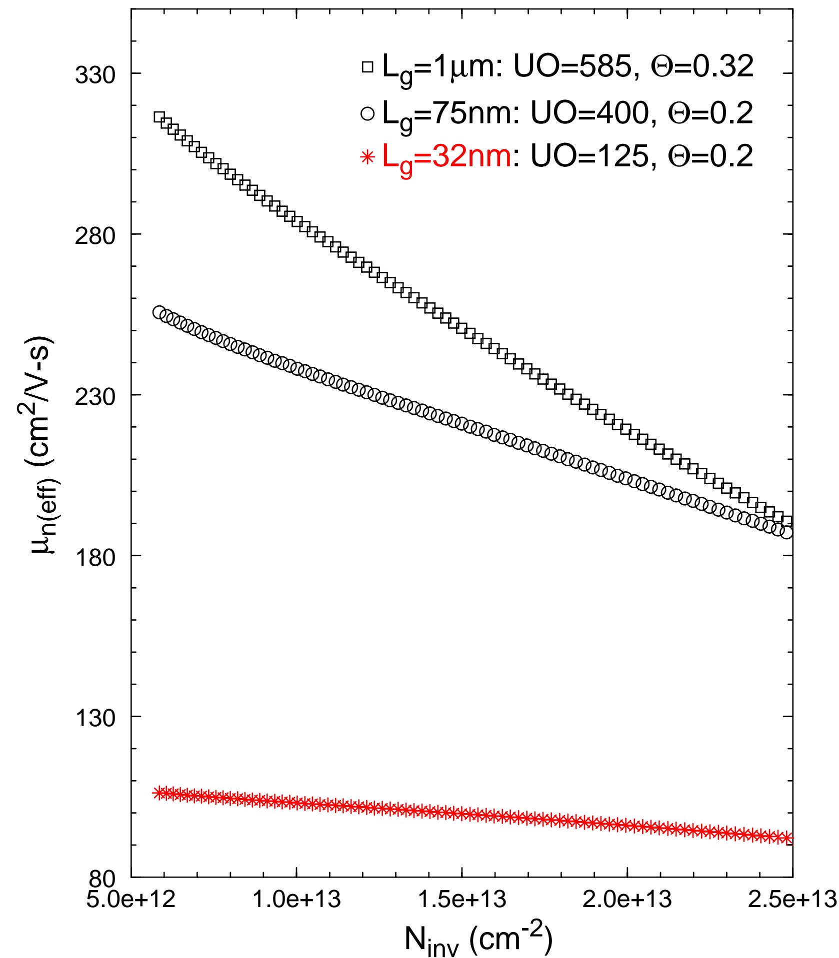
pMOSFETs ⇒ **hole mobilities**





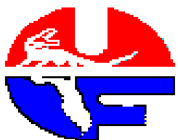
But ....

UFDG calibrations to nFinFETs with varying L_g



Scaling L_g degrades μ_{eff}, which implies excessive scattering centers near the source/drain, or perhaps significant remote S/D Coulomb scattering.

Recent work suggests that this problem can be resolved via optimal S/D engineering.



UFDG/Spice3: Pragmatic nanoscale DG-FinFET CMOS can give good speed performance (with very low I_{off}).

L_g = 18nm DG CMOS unloaded RO delays

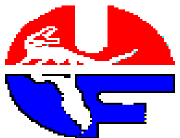
Abrupt $N_{SD}(y)$ w/ G-S/D overlap ($0.1L_g$)
G-S/D underlap (3.4nm); t_{ox} = 1.0nm
G-S/D underlap (3.4nm); t_{ox} = 1.5nm

Delay/Stage [ps]
8.0
7.0
6.0
5.0
4.0
3.0
2.0

0.7
0.8
0.9
1.0
1.1
V_{DD} [V]

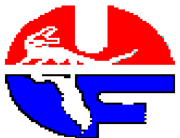
32% speed improvement
with **pragmatic** FinFET design*

*The underlap and the thicker t_{ox} reduce the parasitic G-S/D fringe capacitance, which is very significant in nanoscale CMOS devices.

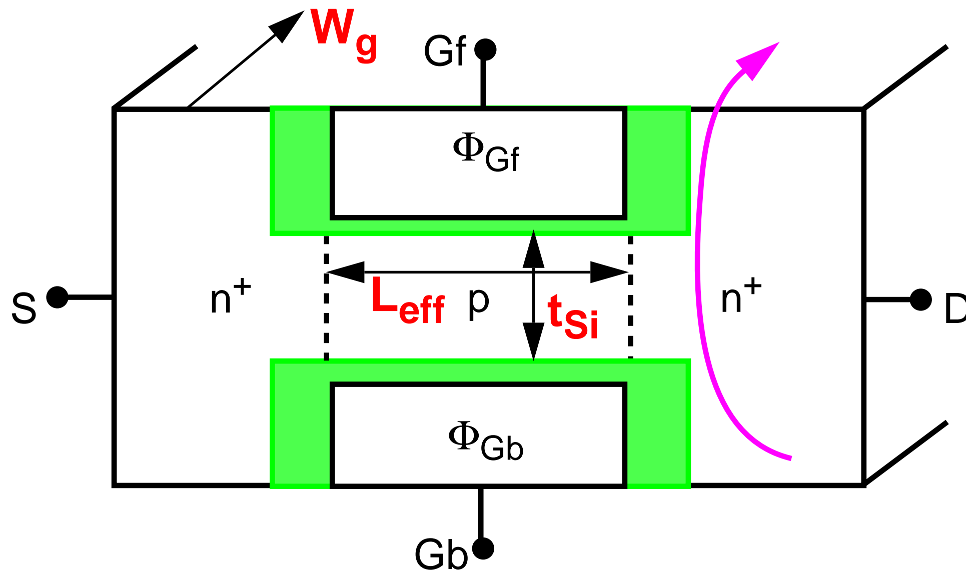


Conclusions

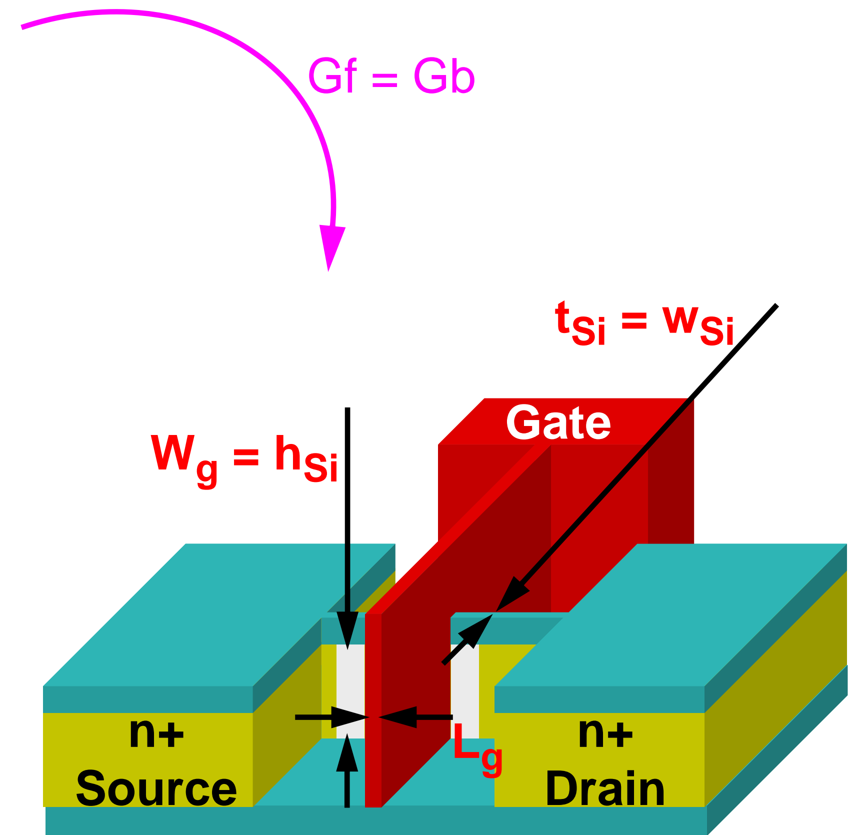
- Pragmatic nanoscale DG-FinFET CMOS is viable, and is potentially scalable to the end of the SIA ITRS (where L_g < 10nm).
- Source/drain engineering for G-S/D underlap, V_t adjustment, and high carrier mobilities must be optimized; and tall, thin fins must be controlled.
- Further, SOI enables embedded FBC (e.g., 1T) DRAM, which can be viable.



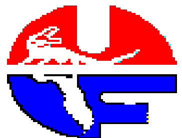
UFDG: A Process/Physics-Based Predictive Compact Model Applicable to Generic UTB DG MOSFETs



Gf = Gb



UFDG is applicable to SG FD/SOI MOSFETs, as well as symmetrical-, asymmetrical-, and independent-gate DG MOSFETs, including FinFETs.

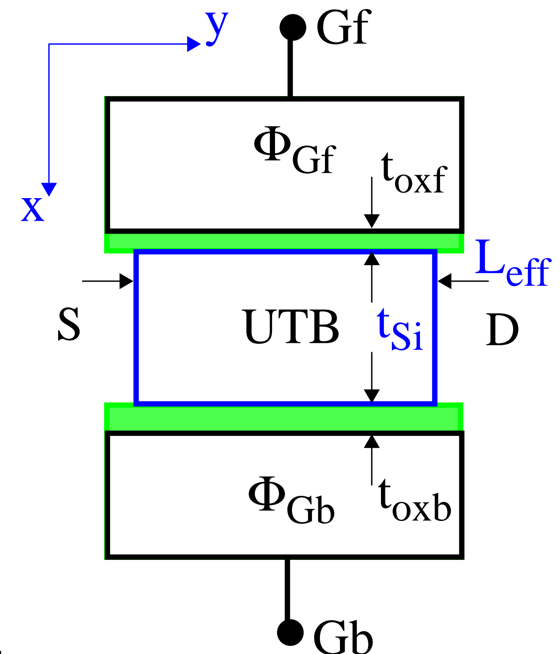


Short-Channel Effects Modeling in UFDG

(or, how two gates give good control of the electrostatics)

2-D Poisson equation (for weak inversion),

$$\frac{\partial^2 \phi}{\partial x^2} + \frac{\partial^2 \phi}{\partial y} \cong \frac{qN_B}{\varepsilon_{Si}} \quad ,$$

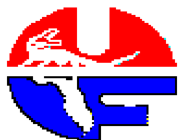


is solved in (rectangular) body/channel (UTB) region, defined by t_{Si} and $L_{eff} \neq L_g$, by assuming

$$\phi(x, y) \cong \alpha_0(y) + \alpha_1(y)x + \alpha_2(y)x^2$$

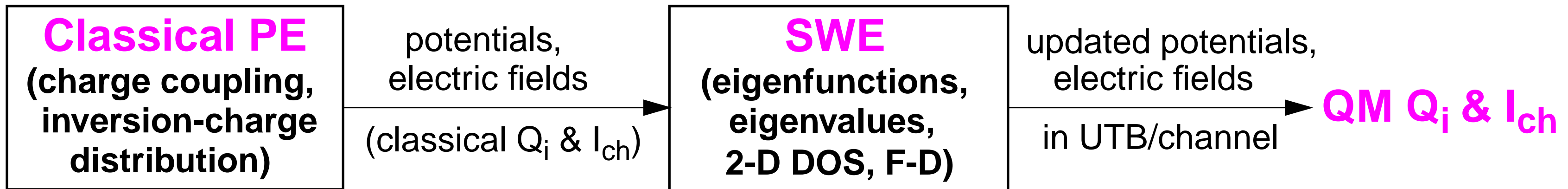
in Poisson, and applying the (four) boundary conditions (including surface-state charge at both interfaces). The derived potential (with QM shift) defines the integrated (in x-y, over t_{Si}) inversion charge (Q_i) and an effective channel length ($L_e < L_{eff}$ averaged over t_{Si}) for predominant diffusion current (in y), and thus accounts for:

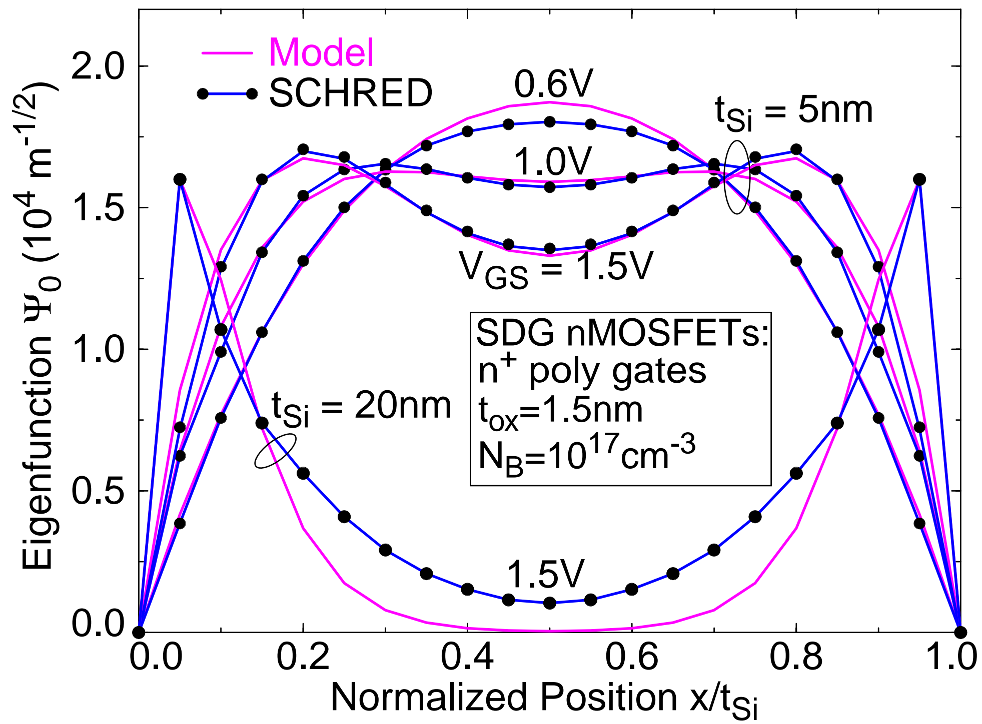
- **S/D charge (impurity and/or carrier) sharing [$V_t(L_{eff})$ & $S(L_{eff})$]** ,
- **DIBL (throughout UTB) [$\Delta V_t(V_{DS})$]** .



Quantization Effects Modeling in UFDG

UFDG is actually a compact Poisson-Schrödinger solver:





1-D SWE analytical solution is derived using a variational approach, then coupled to PE and $Q_i(V_{GfS}, V_{GbS})$ via Newton-Raphson iteration, all with dependence on t_{Si} and Si orientation, as well as E_x.

The QM modeling is also the basis for a physical mobility model for the UTB carrier transport.