Nanodevices for Terahertz

David Ferry
Arizona State University

Nanostructures Researc

CENTER FOR SOLID STATE ELECTRONICS RESEARCH

Dave Ferry

Marco Saraniti

Richard Akis

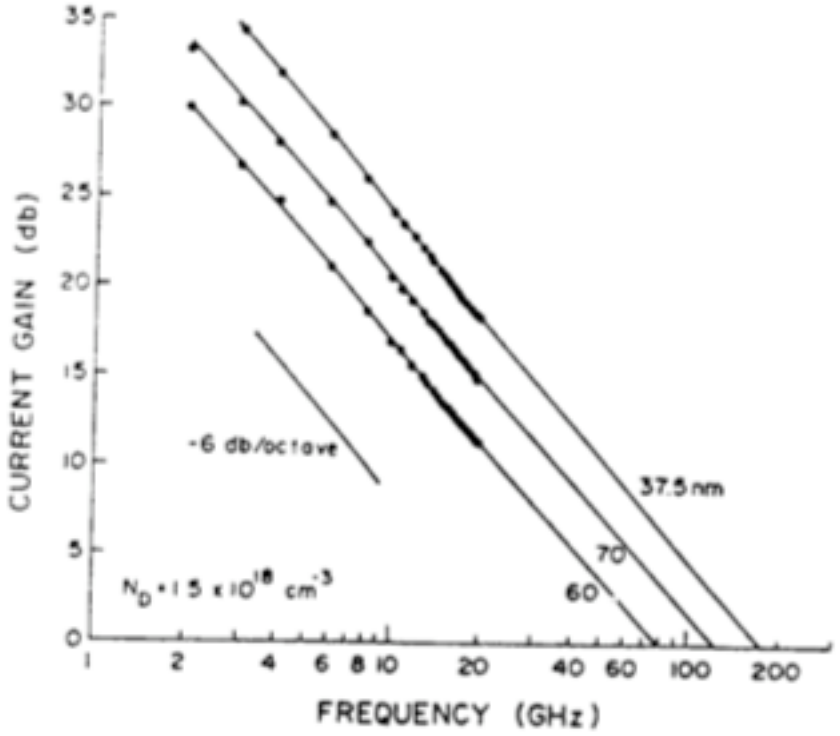
Stephen Goodnick

Nicolas Faralli

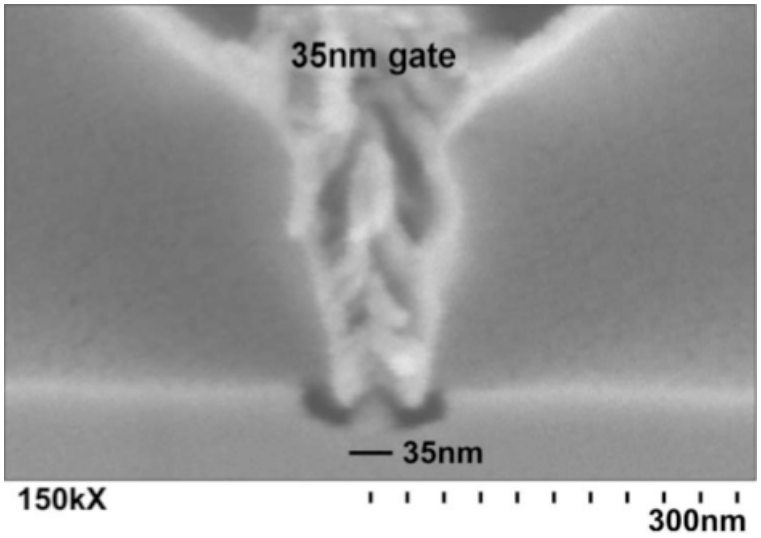
Diego Guerra

Fabio Marino

In 1989, a university laboratory, working on nanoscale GaAs HEMTs and MESFETs could produce devices with f_T ~ 170 GHz. In 20 years, where have we gone? *Where can we go?*



Terahertz transistors have quite small gate lengths!



X. B. Mei *et al.*, EDL **28**, 470 (2007)

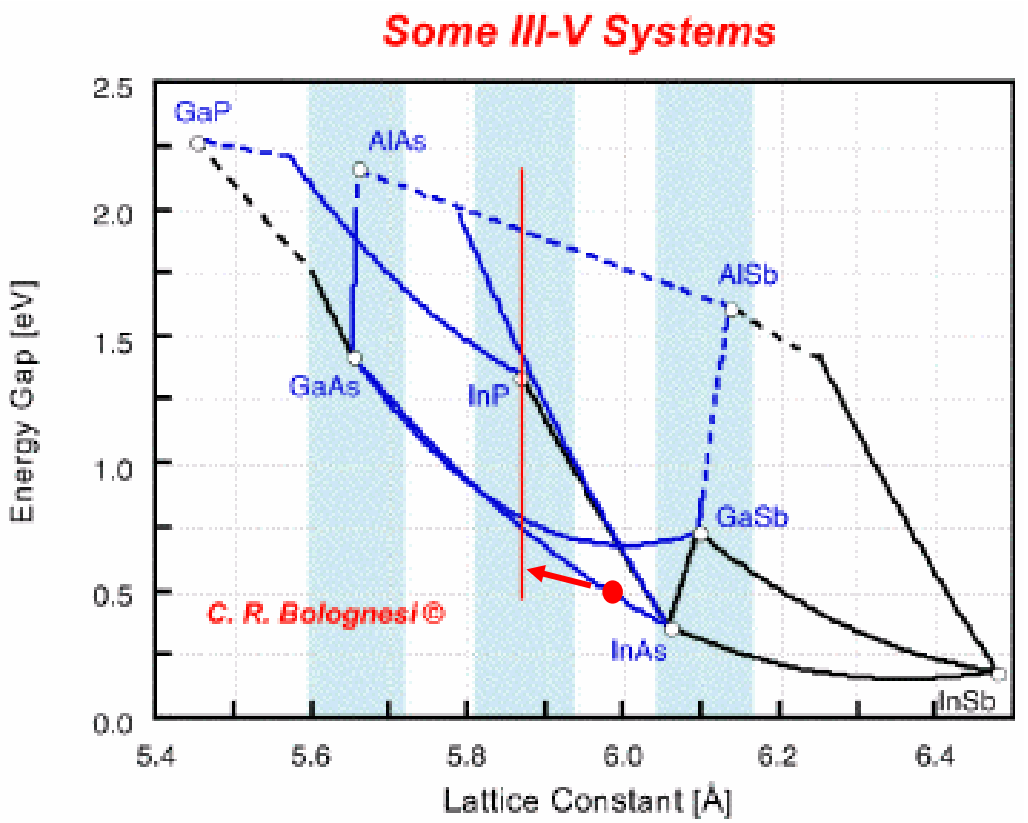
These devices have shown remarkable performance with f_{max} ~ 1.2 THz and f_T ~ 0.6 THz.

But, more can be done!

Here, I will discuss the scaling of these InGaAs quantum well HEMTs, and show the prediction of performance beyond 10 THz.

I will also discuss GaN HEMTs and their relative performance for power and noise.

The first devices of interest to us are: Pseudomorphic InGaAs on InP

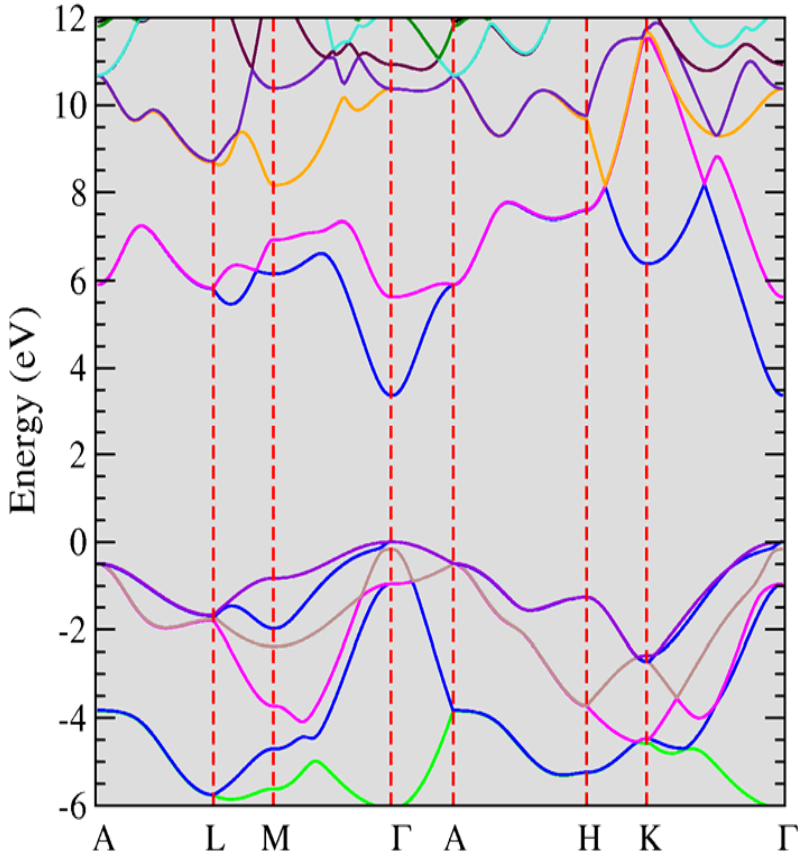


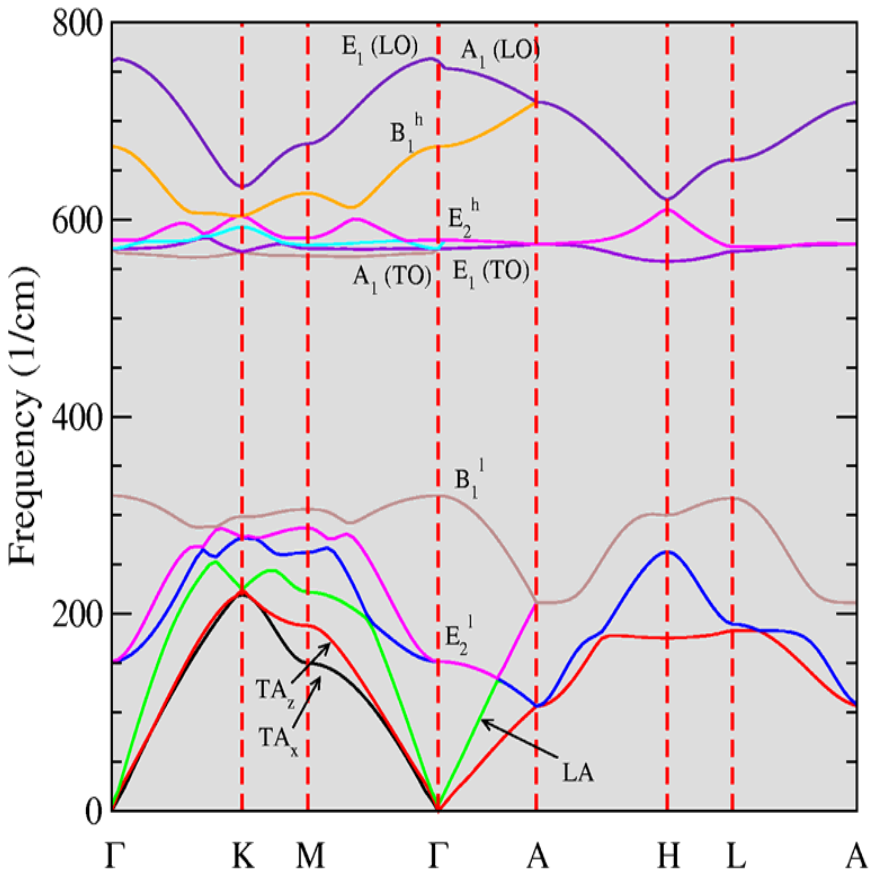
The particular material in which we are interested is $In_{0.75}Ga_{0.25}As$, grown on InP.

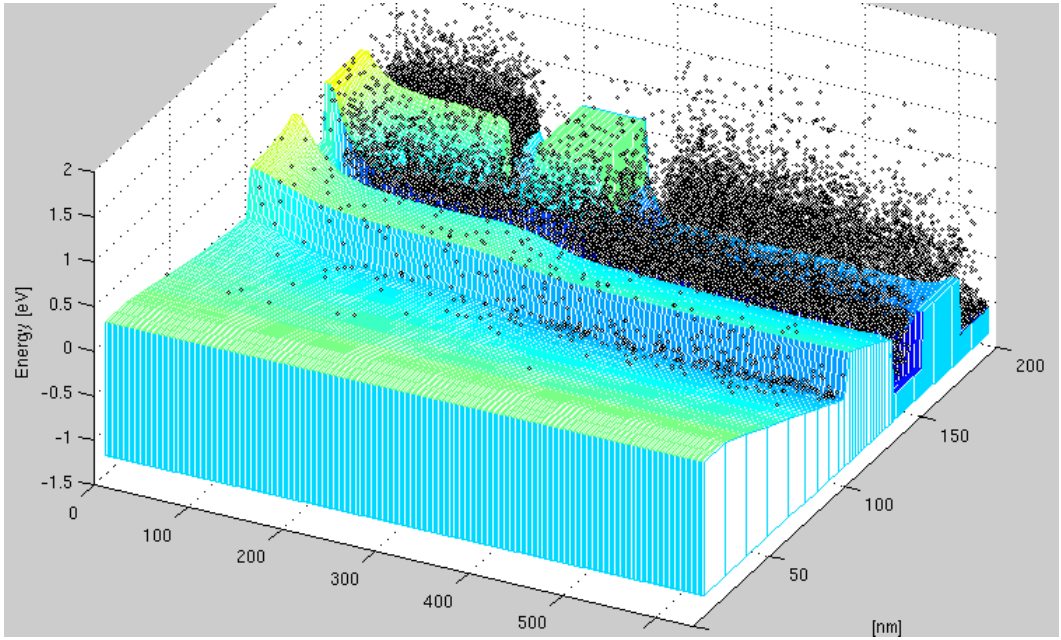
This results in compressive stress on the layer, which widens the bandgap.

Full-Band Monte Carlo Simulations

Central to achieving good agreement with actual devices is the use of a full band simulation—We use an empirical pseudo-potential method to compute the band structure and, subsequently, the phonon dispersion and the electron-phonon coupling "constants"

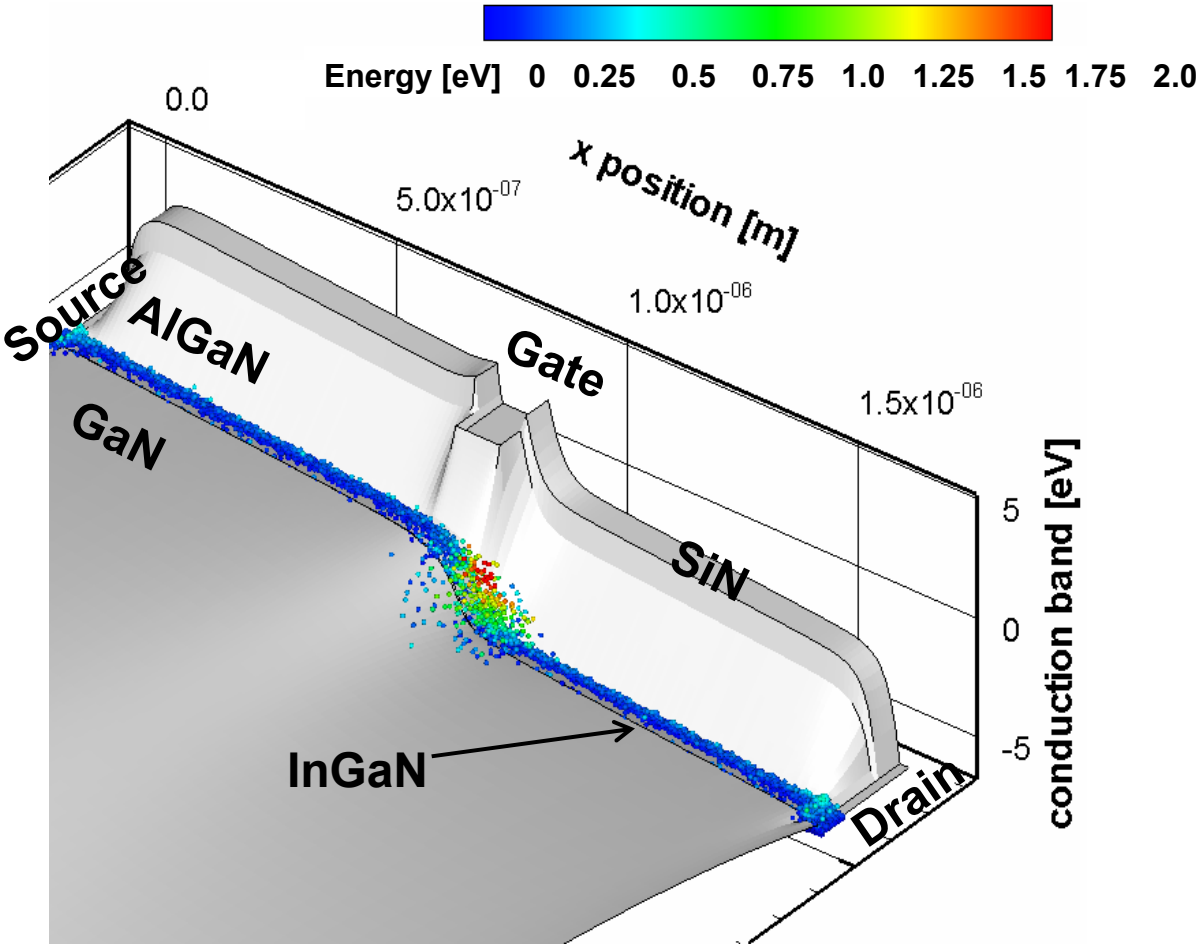






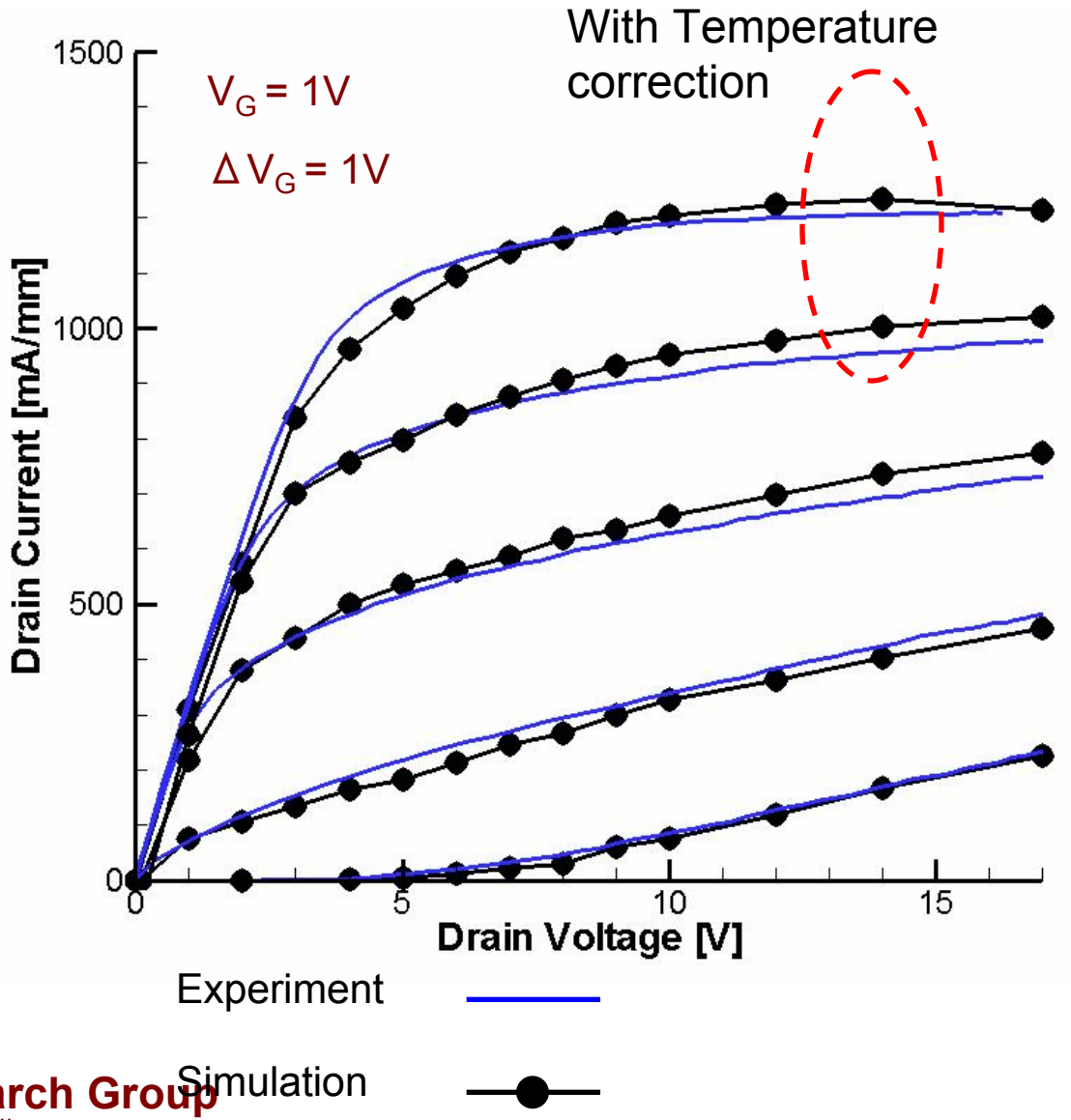
The simulation itself couples a cellular Monte Carlo transport kernel to the self-consistent solutions of Poisson's equation to give the local potential and fields. This allows computation of currents, particle distributions in both space and momentum—which is crucial to establish physical processes in frontier-sized devices.

We first consider a GaN-based power HEMT, similar to one published recently by the Santa Barbara group.



Output Characteristics

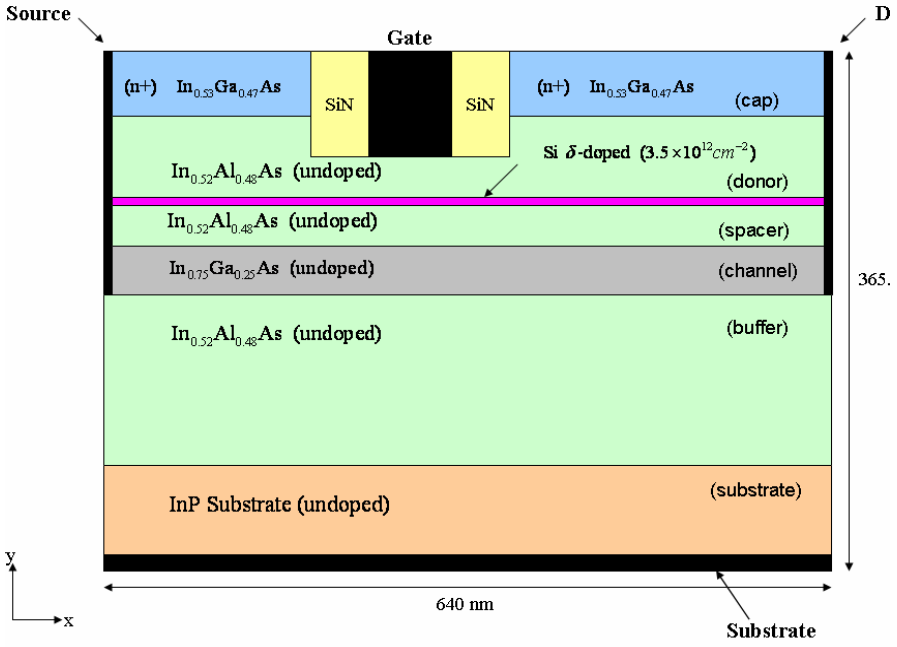
Good agreement is obtained at higher gate biases only when thermal heating in the drain region is included within the simulation.

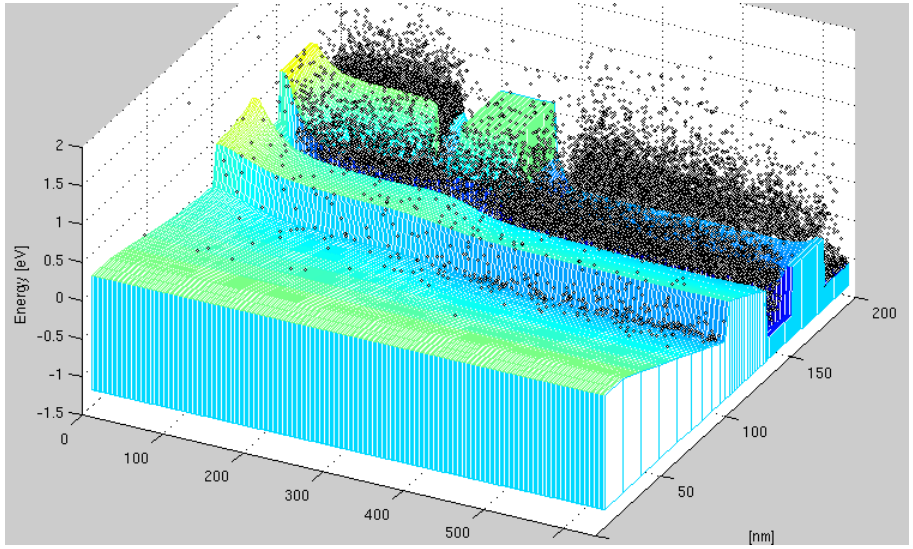


Data furnished by Tomas Palacios (MIT): T. Palacios *et al.*, IEEE Electron Dev. Lett. **27**, 13 (2006).

Next we consider an InP-based HEMT for use near 1 THz. This is a multilayer structure, in which the active channel is a strained InGaAs quantum well. Experimental devices (35 nm gate length) have shown f_T~700 GHz and f_{max}~1.2 THz.

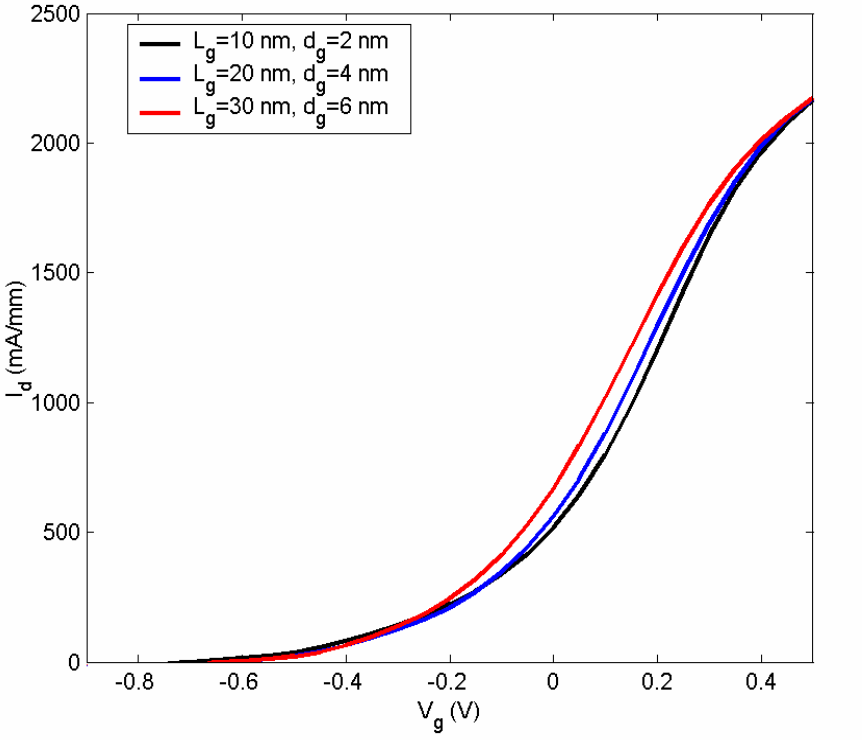
Here, we will examine scaling of the gate length (10-50 nm) for a 300 nm source-drain spacing, to examine what the limits of these devices can be.

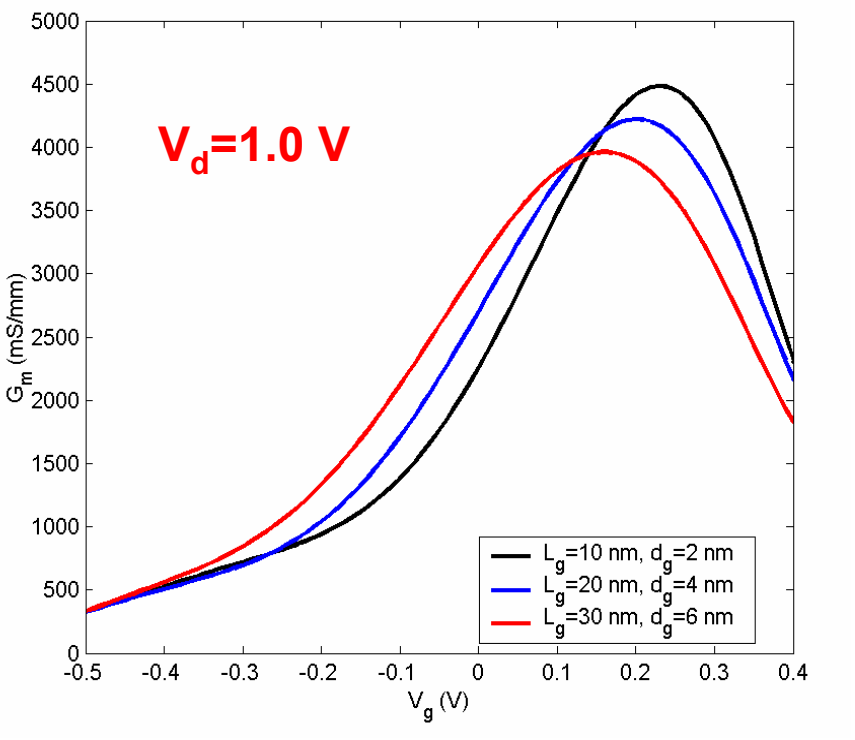




J. Ayubi-Moak *et al.*, IEEE TED 54, 2327 (2007)

Drain current and transconductance for different L_g



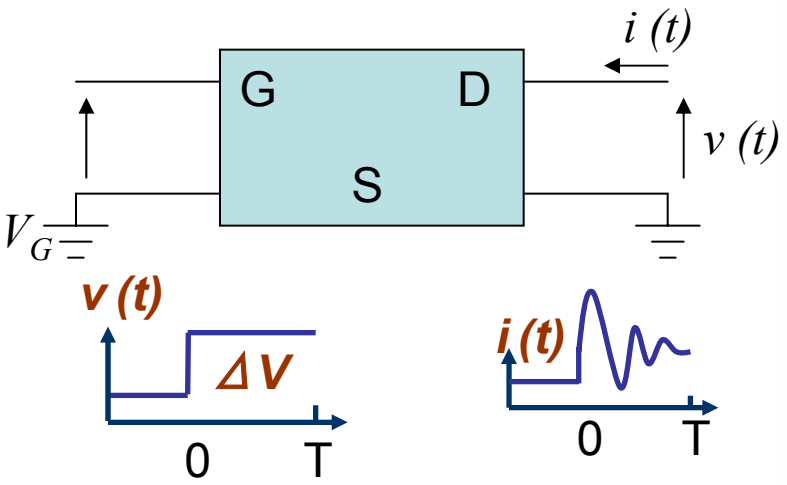


A refined polynomial fit is used to fit the actual simulation data and this is plotted for various devices.

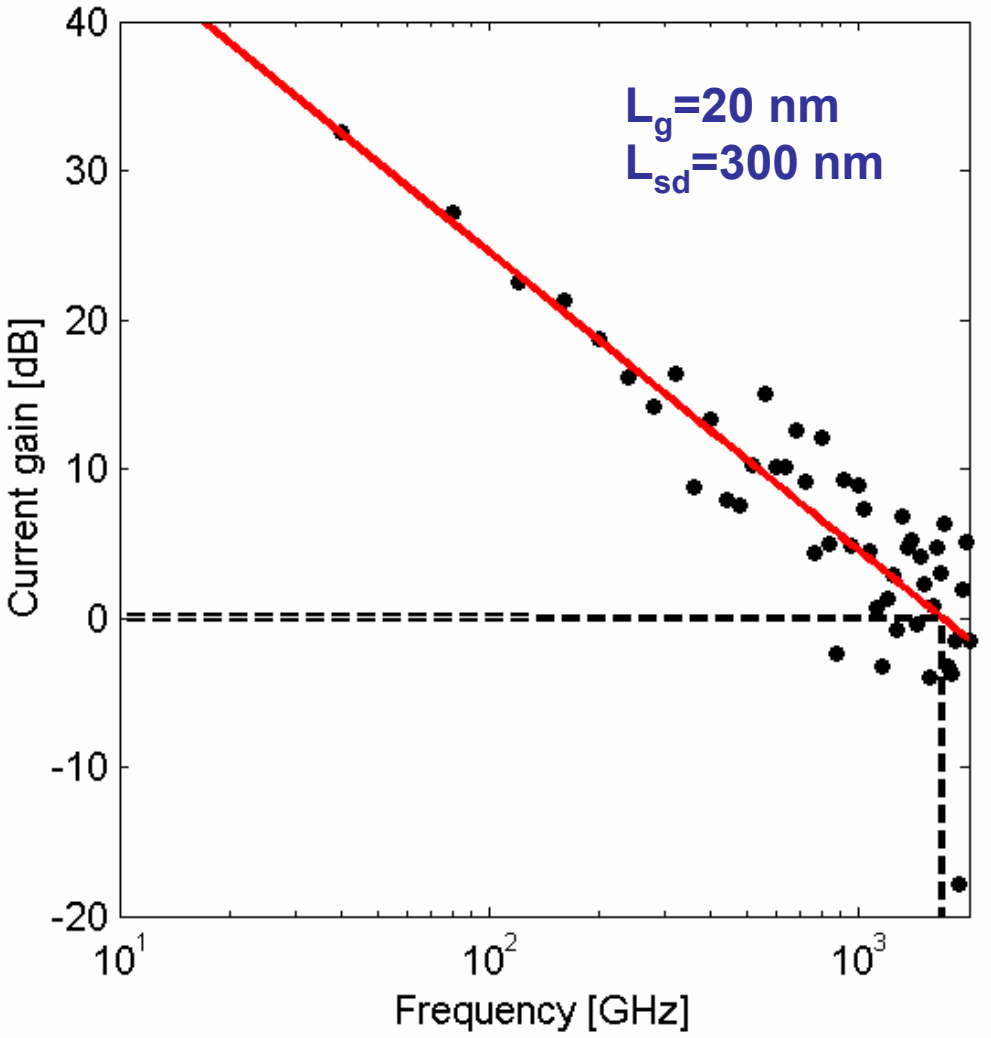
18 nm channel

Calculating the Frequency Response

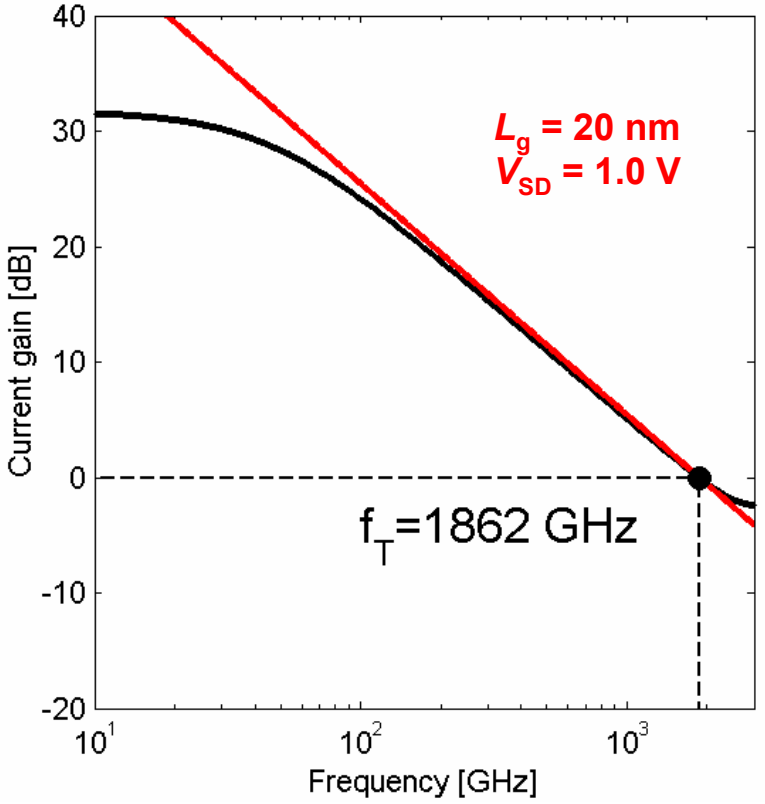
Small signal analysis

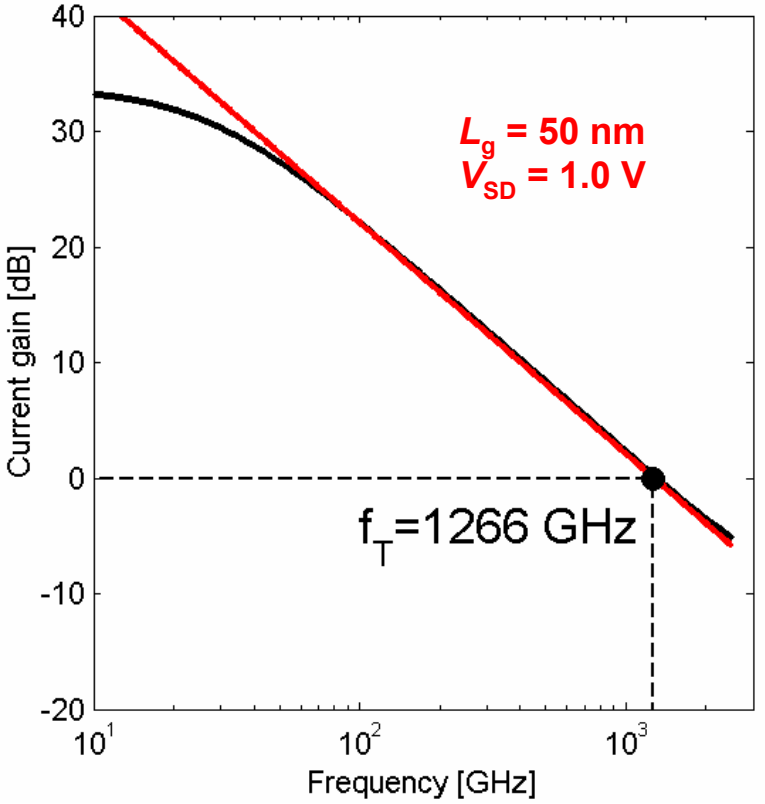


We will discuss f_T and f_{max}

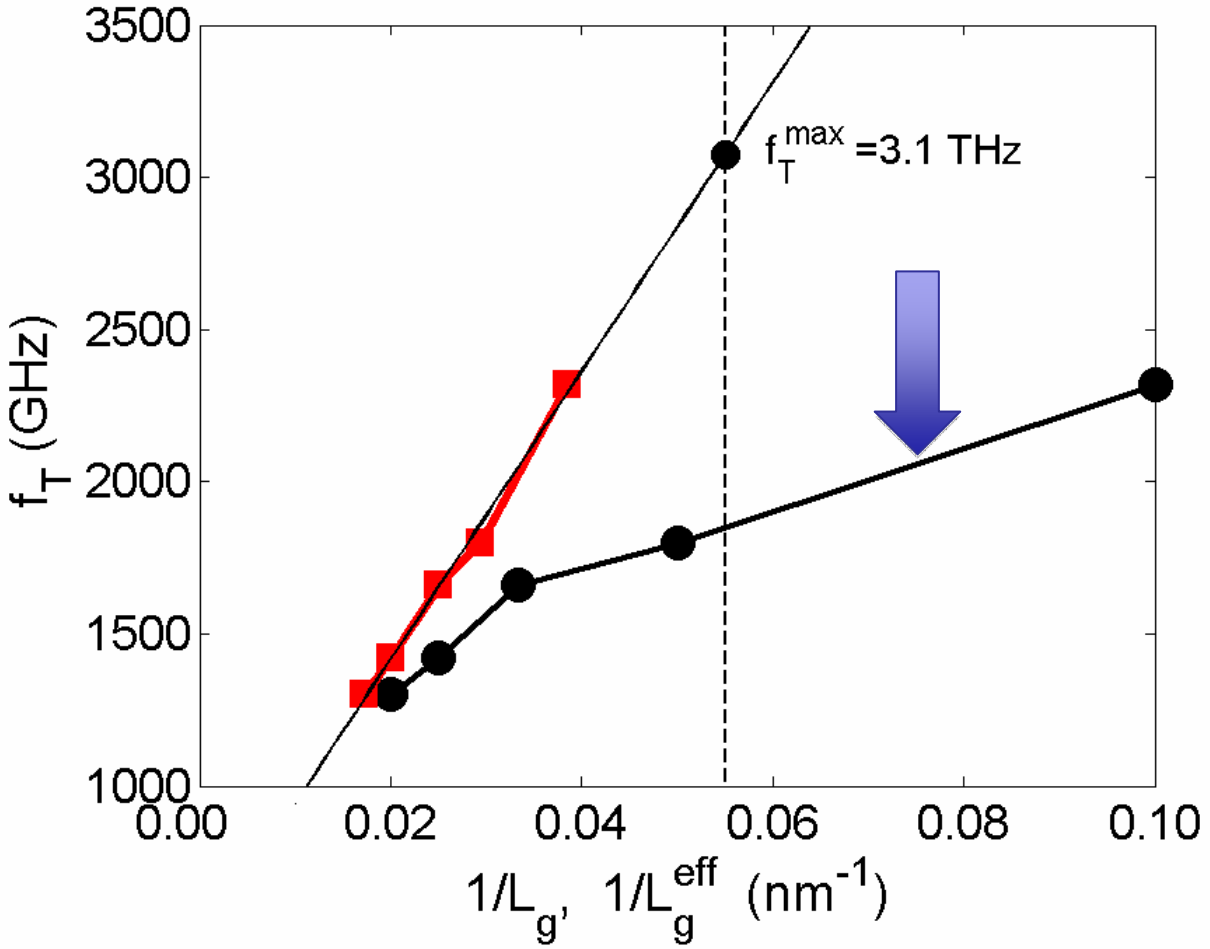


Frequency Response in Scaled Devices





Dependence of Cutoff Frequency on Scaled Gate Length



The nonlinear behavior suggests that our use of the *actual* gate length is in error.

HEMTs have regions between the source and gate and the gate and drain, which are parasitic—the gate fields penetrate into these regions and we have estimate the *effective* gate length.

To do this, we use the normal definition of the cutoff frequency:

$$f_T = \frac{1}{2\pi\tau_{gate}}$$

Since the gate delay is given by the cutoff frequency, this can be used to determine the effective gate length:

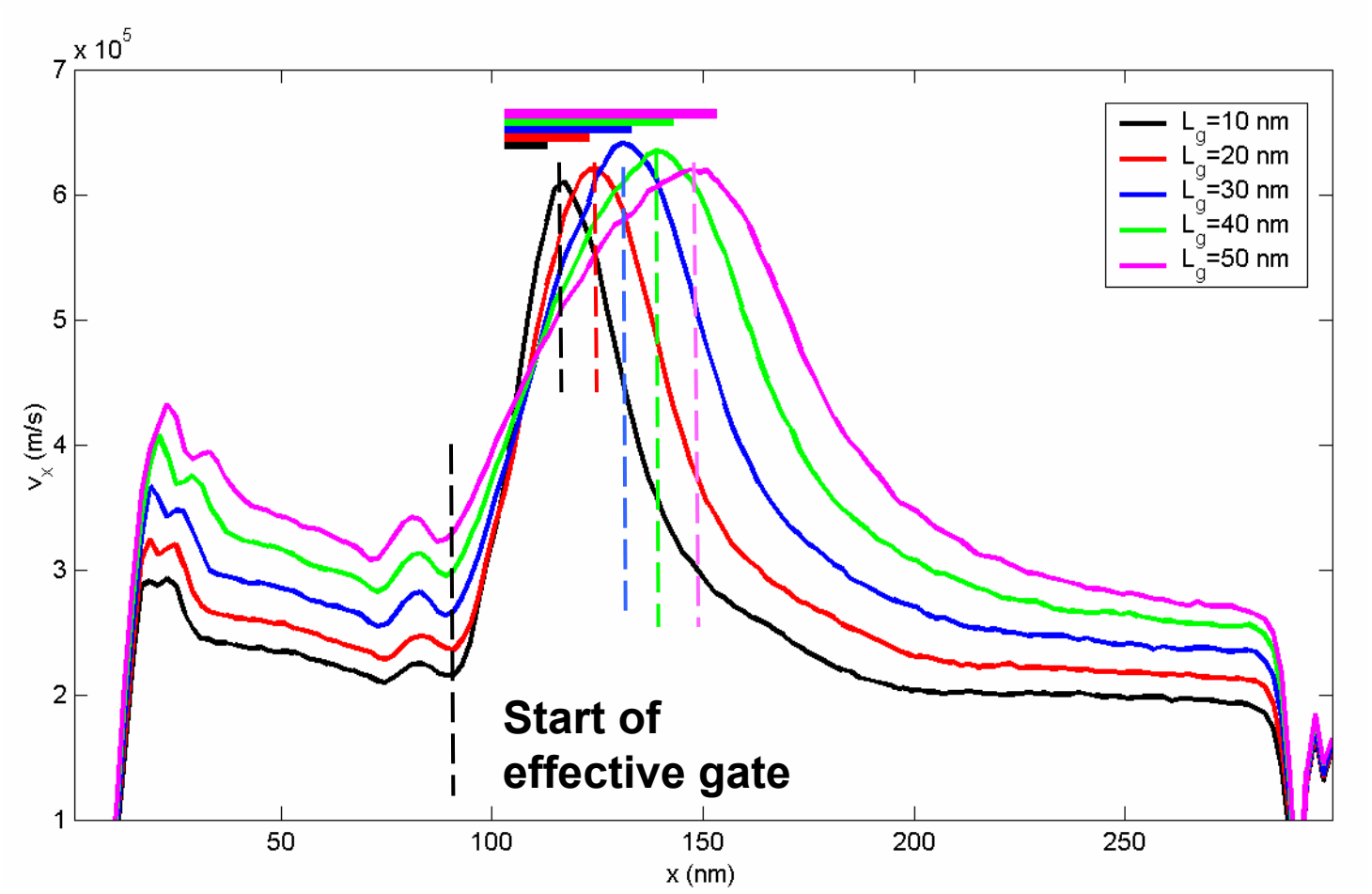
$$\tau_{gate} = \sum_{L_g} \Delta t(x_i) = \sum_{L_g} \frac{\Delta x}{v_i} \longrightarrow$$

velocity at grid point *i*

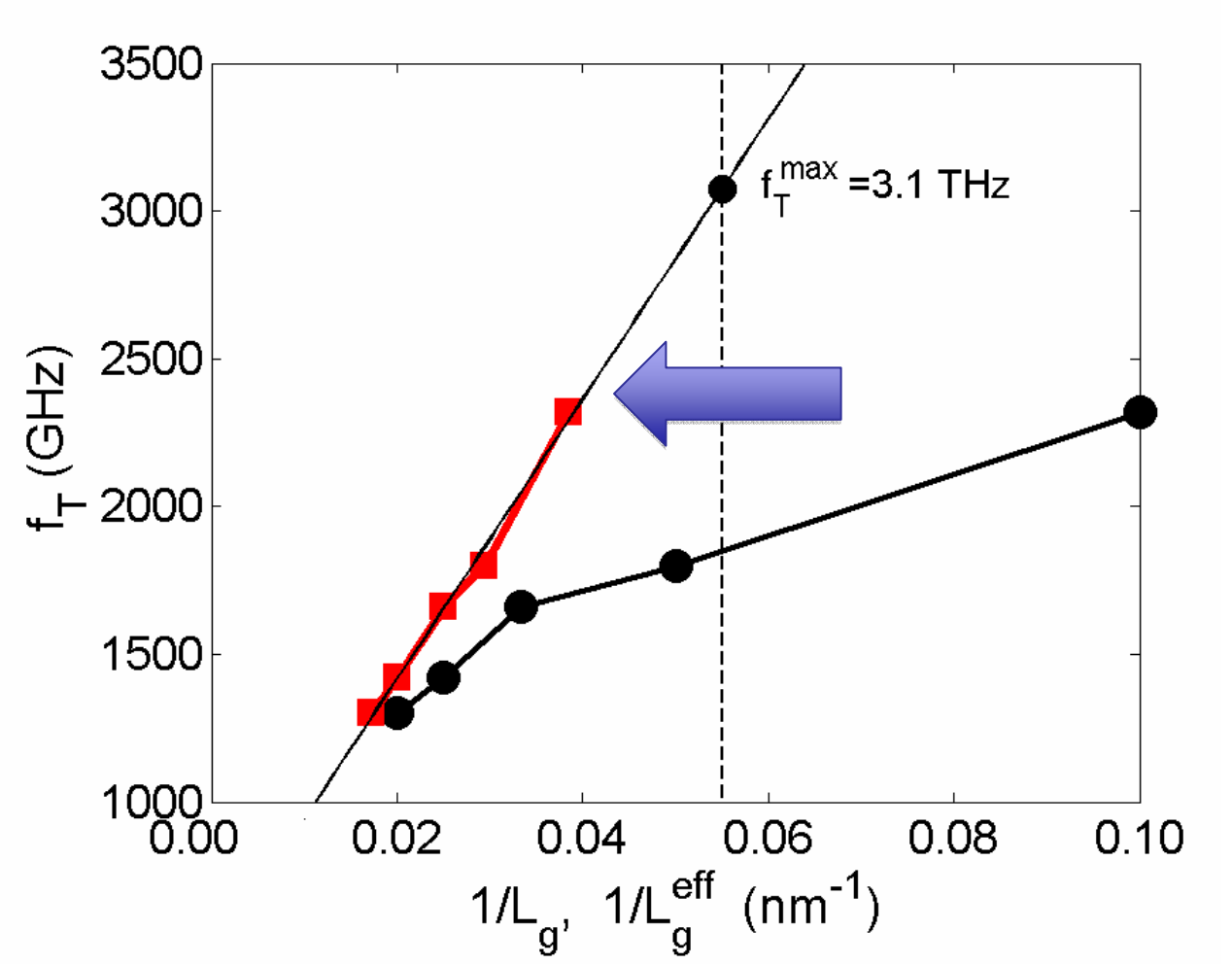
$\Delta x = 2\ nm$ in our simulation grid

The cutoff frequencies computed in this manner agree well with those obtained from the Fourier analysis, provided that t_{gate} is computed over the effective gates

Velocity versus position



Dependence of Cutoff Frequency on Effective Gate Length



Conclusions

- Contact and series resistance significantly lowers device performance
- Studies of properly scaled devices, with 18 nm InGaAs quantum well channels, have shown room for considerable improvement and given a new definition of the role of the effective channel length.
- These suggest that the ultimate limit, for this structure, is above 3 THz.