Nanostructures for Tera-bit Level Charge Trap Flash Memories

Byung-Gook Park, Il Han Park, Jung-Hoon Lee,
Gil Sung Lee, Jang-Gn Yun
Inter-University Semiconductor Research Center
School of Electrical Eng. and Computer Sci.
Seoul National University

Outline

I. **Introduction**

II. NAND Cell Structure

III. NOR Cell and Array Structure

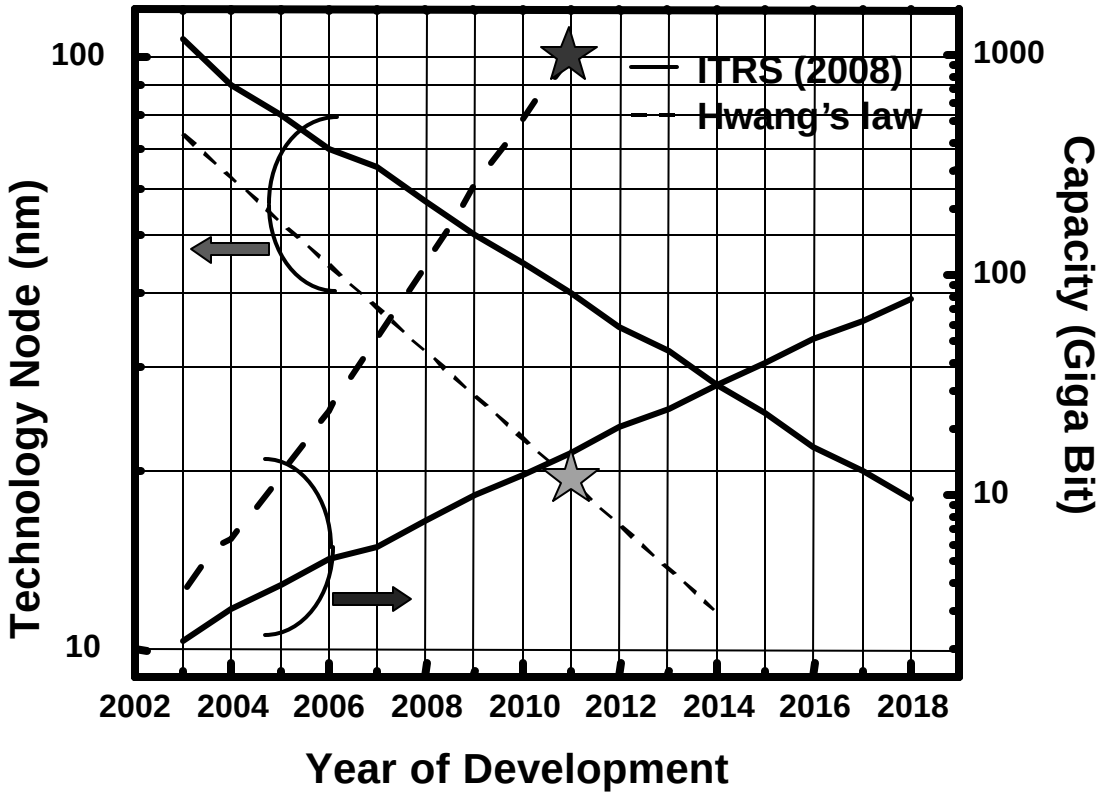
IV. AND Cell and Array Structure

V. STAR NAND Flash Structure

VI. Conclusions

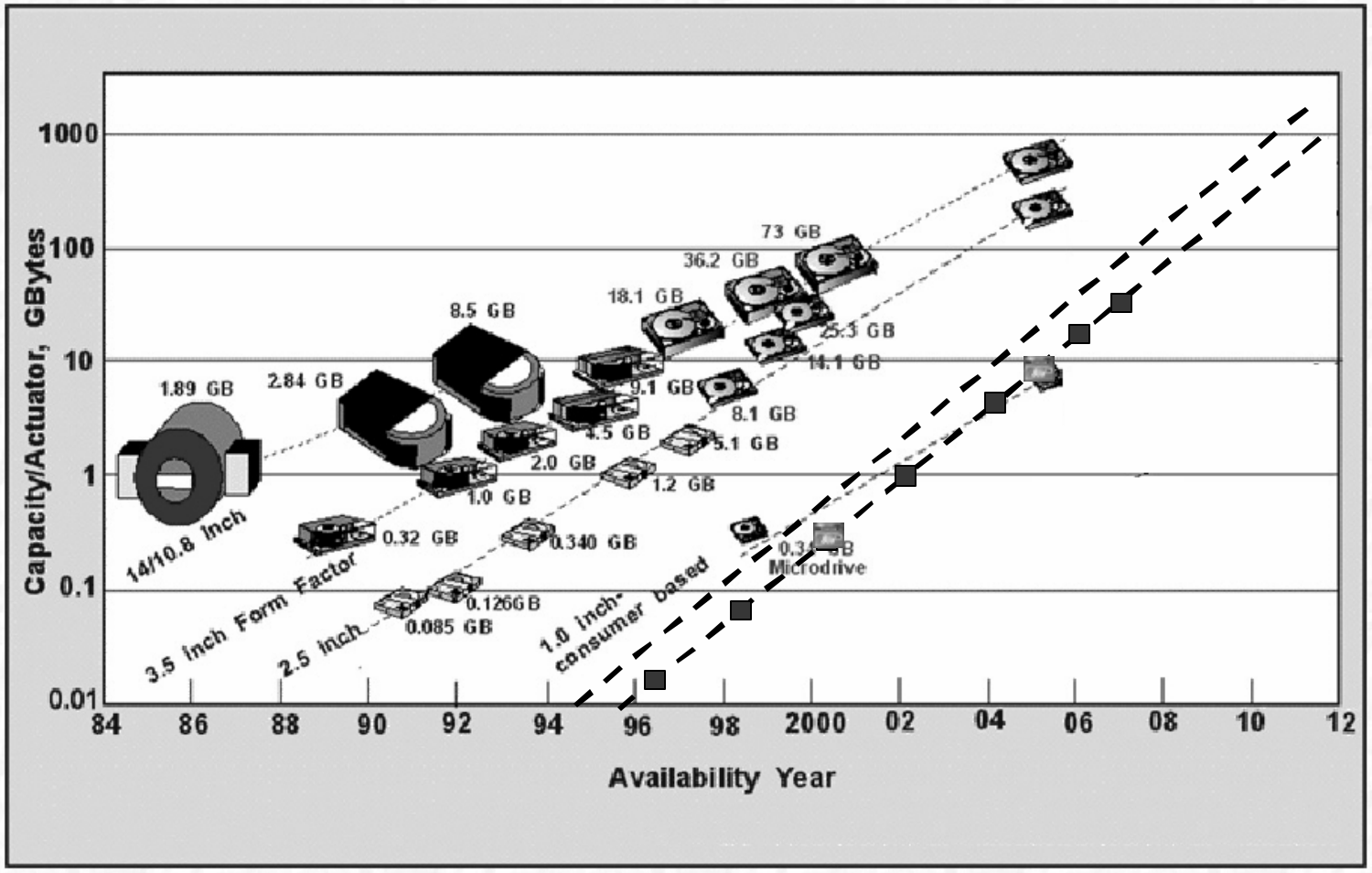
Flash Memory and Mobile Equipments

Expedited Growth Theory - NAND Flash



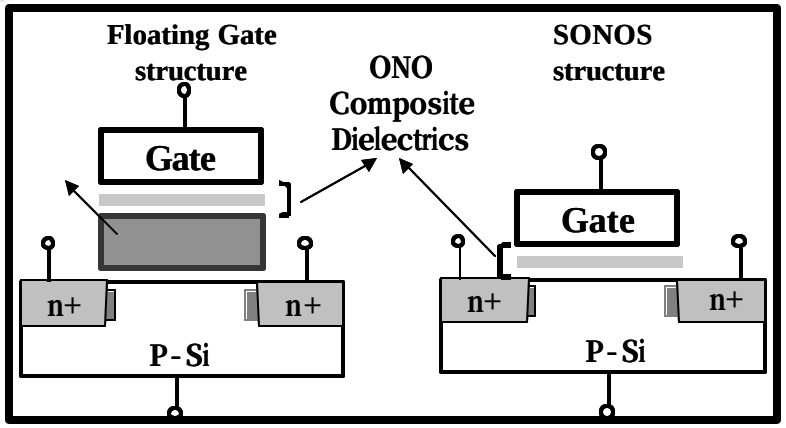
- Expedited growth theory of NAND flash memories
  - ➔ Year 2011 1Tb capacity with 20nm feature size

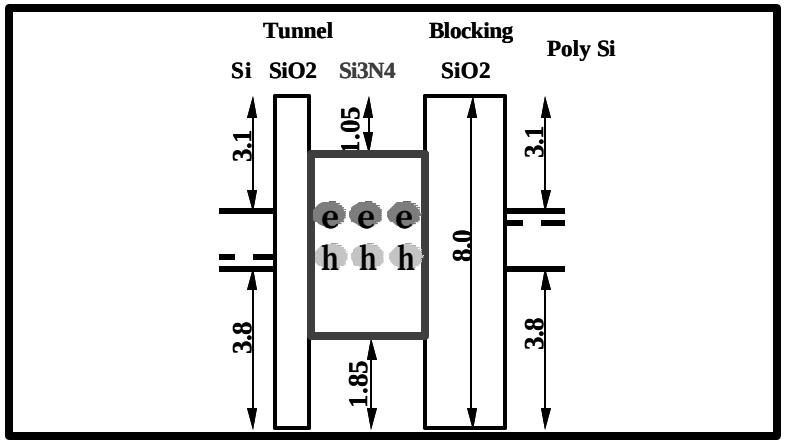
Hard Disk Drive and Flash Memory



Growth of Storage Capacity

Floating Gate vs. Charge Traps





- **No floating gate**
  - *FG-FG space*
  - *FG-active space*
  - *Single gate structure*
- **Defect immunity**
  - *Non-conductive trap layer*
  - *Discrete trap storage*
- **3D structure compatibility**
  - *Insulating storage node*
  - *Simple fabrication*

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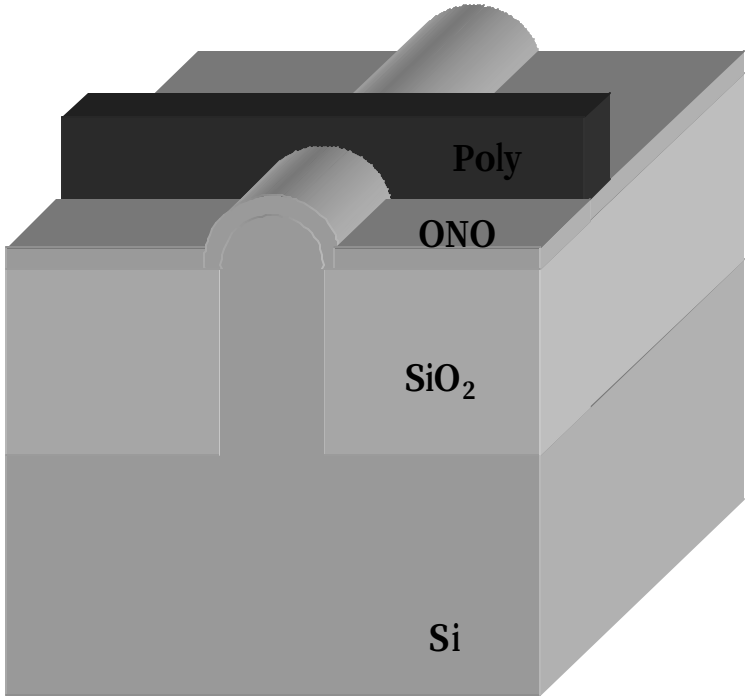
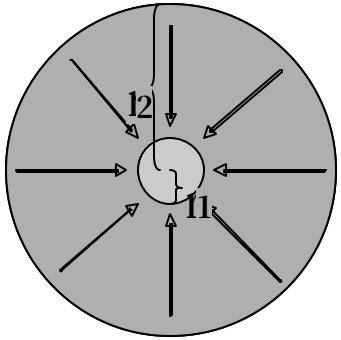
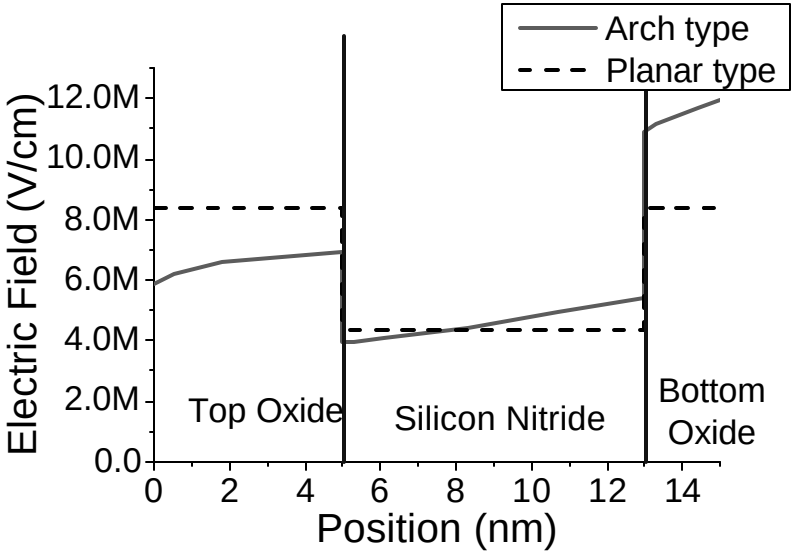
Arch Structure (1)

- Utilization of curved surfaces for field enhancement
  - fast “program” and “erase”
  - increased effective area

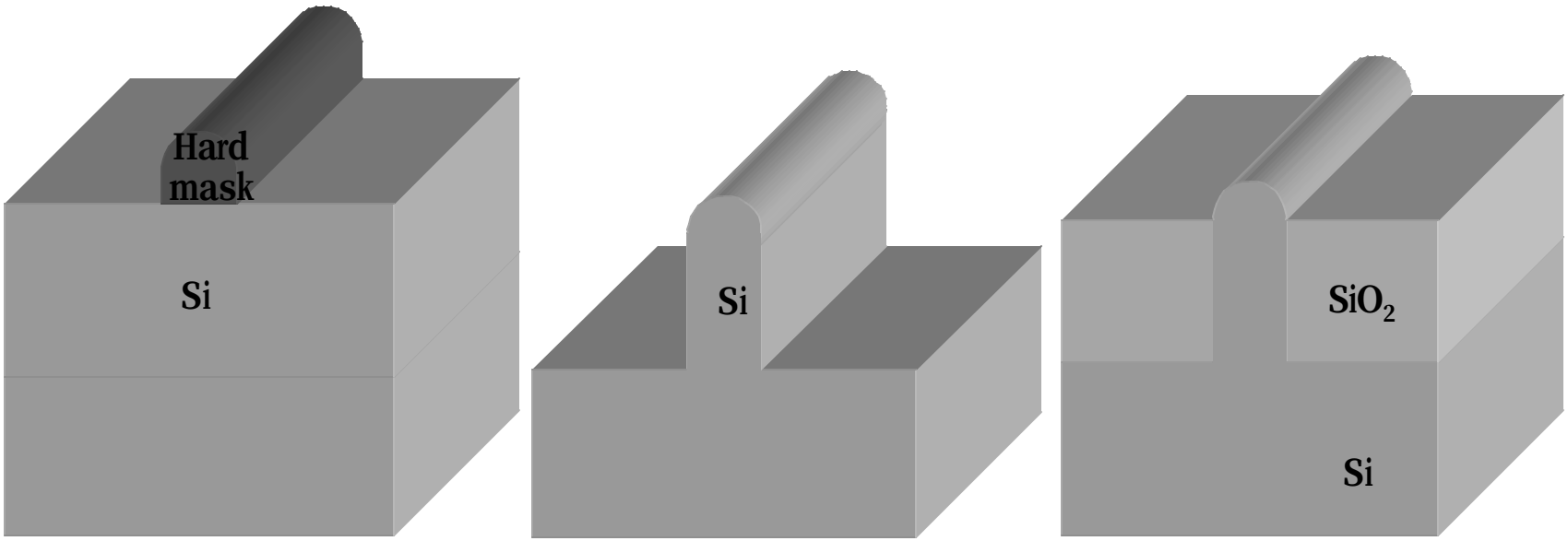






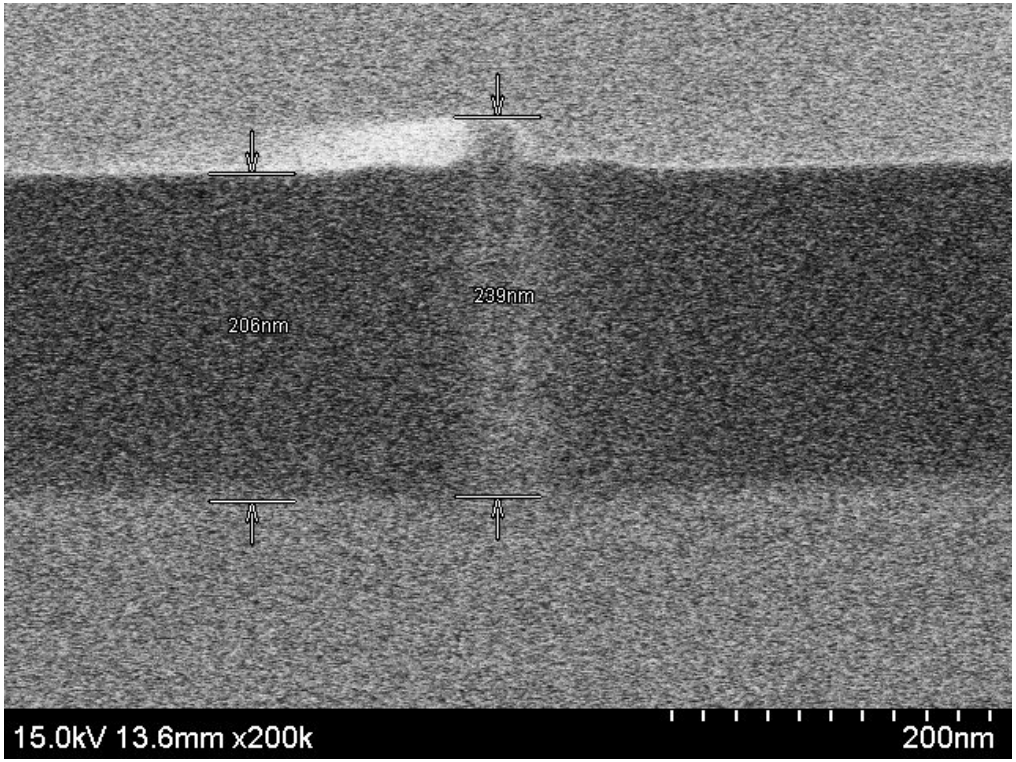
Arch Structure (2)

- Fabrication procedure



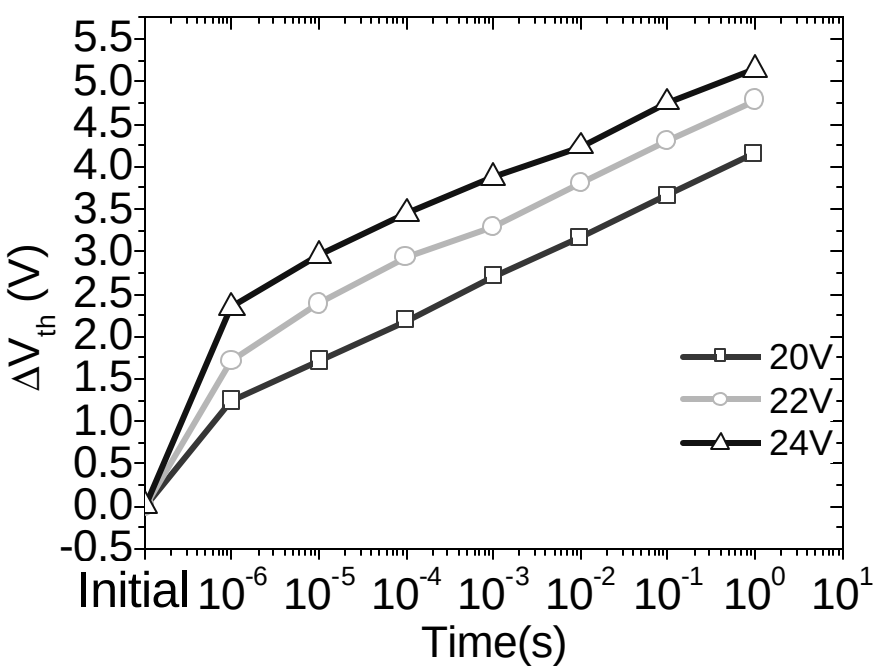
Arch Structure (3)

- Utilization of HSQ mask characteristic
- Planarization by TEOS, HSQ and etch back

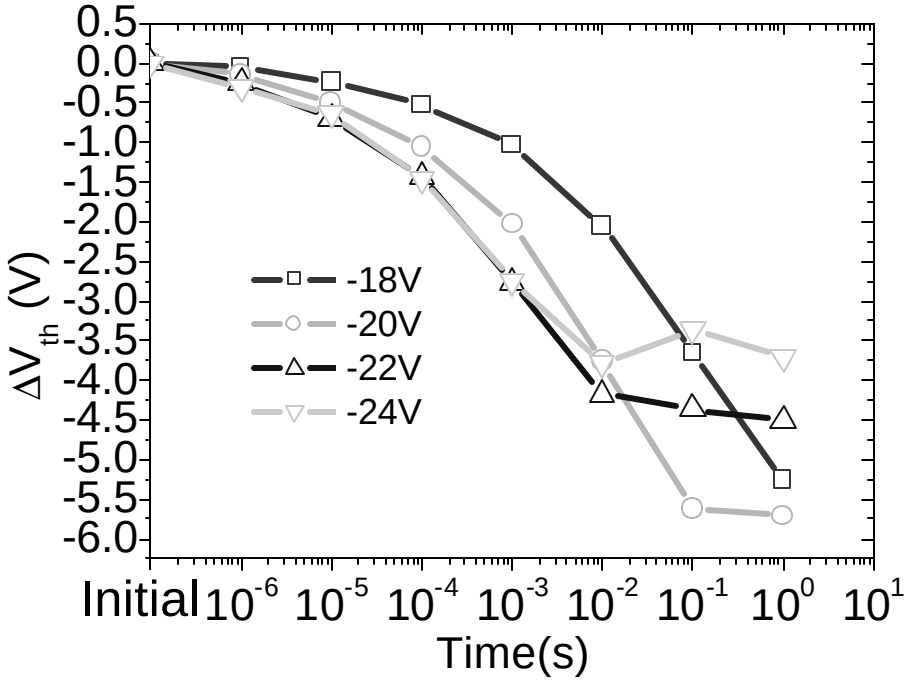


Arch Structure (4)

<Programming characteristics>



<Erase characteristics>



- Radius of Si channel = 15 nm

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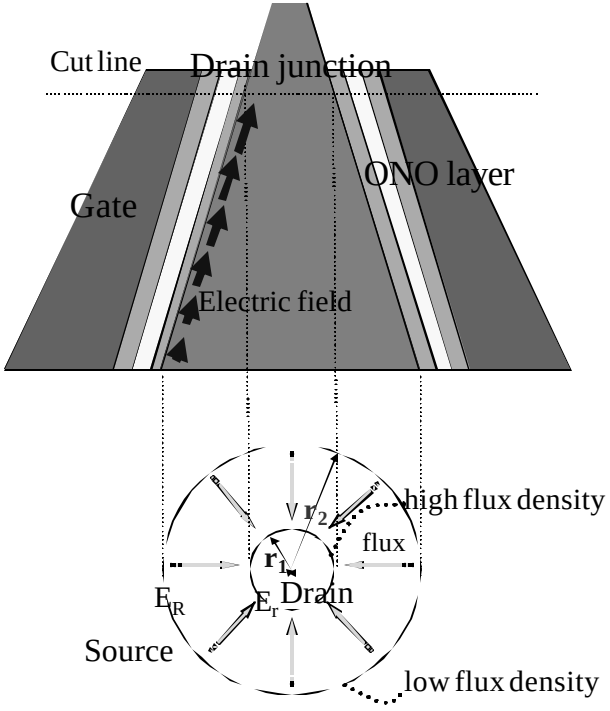
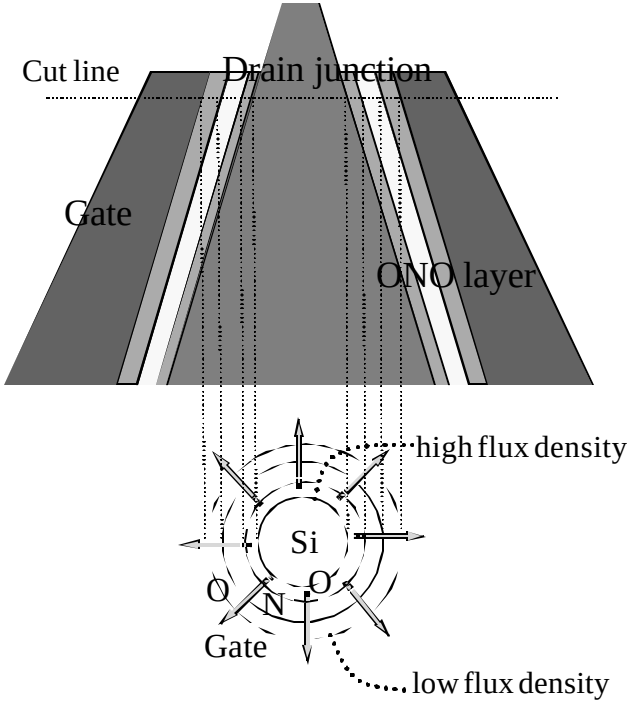
Cone Structure (1)

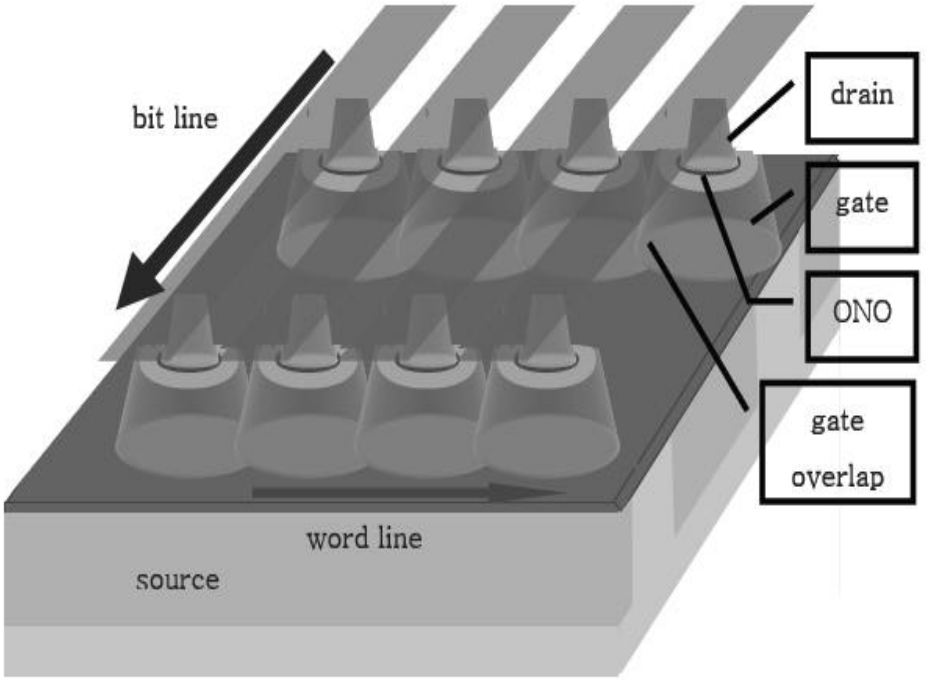
- Utilization of field and current concentration
  - field concentration in the horizontal direction
  - current concentration in the vertical direction





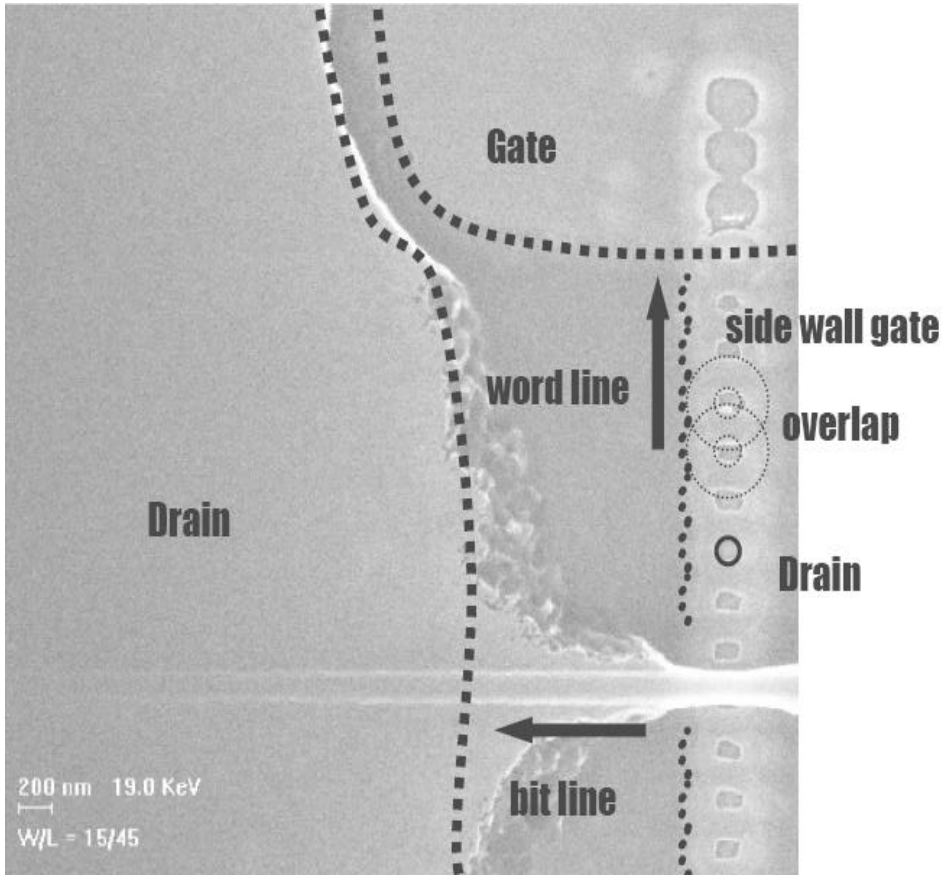
Cone Structure (2)

- Simple array structure
  - common source architecture
  - word line connection through small spacing of cones

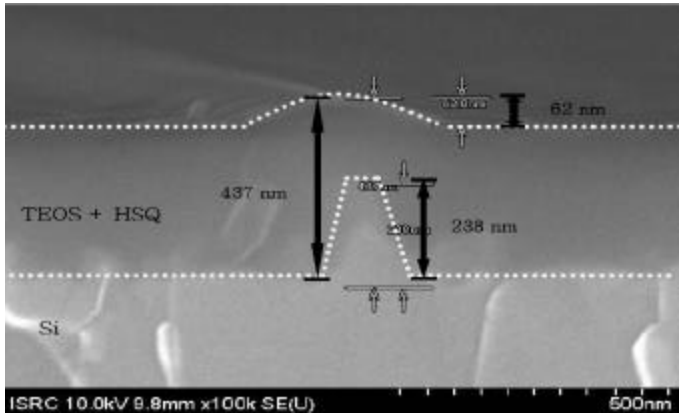


Cone Structure (3)

<Plan view>



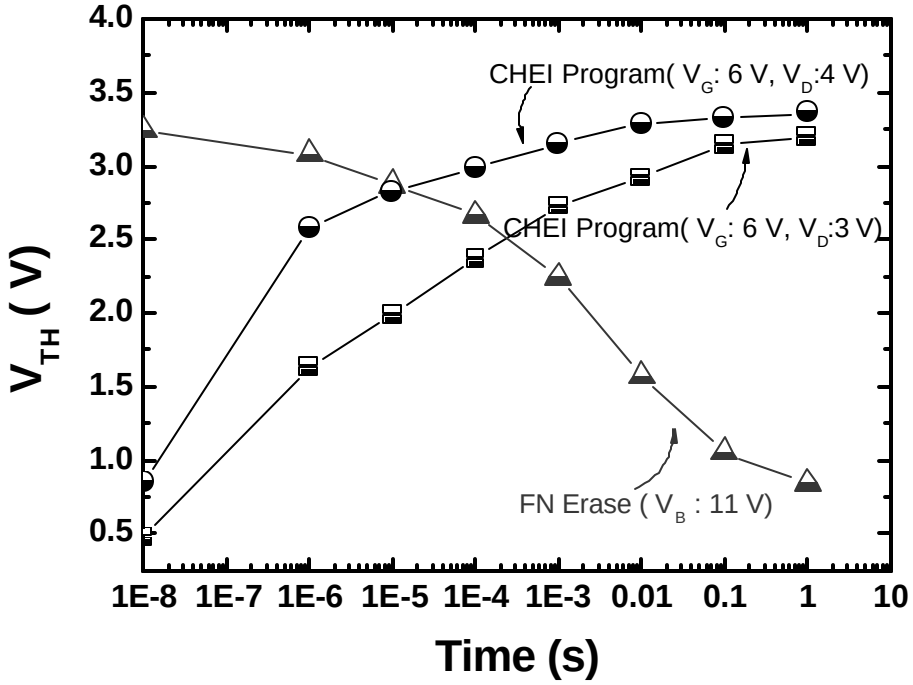
<Cross-sectional view>



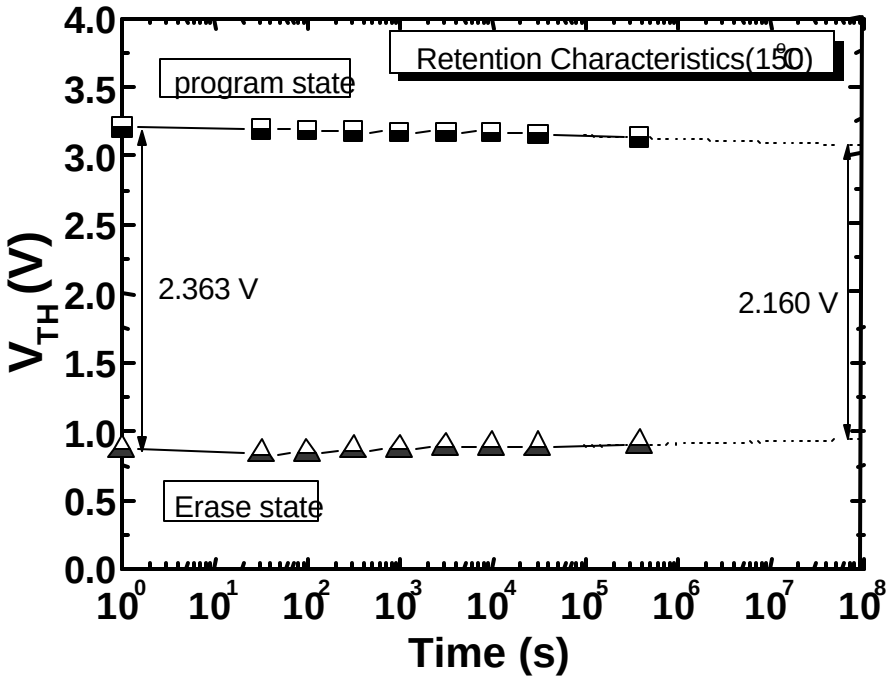
Cone Structure (4)

- Electrical characteristics

<Program/erase characteristics>



<Retention characteristic>



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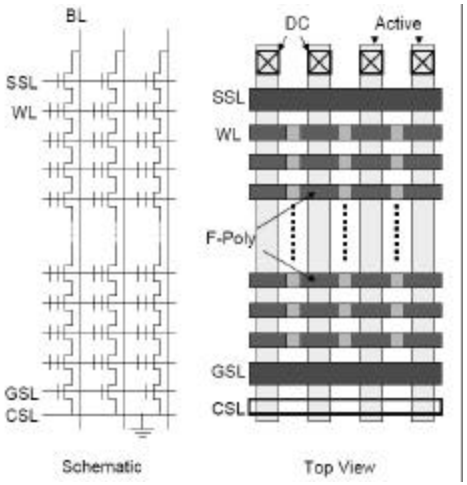
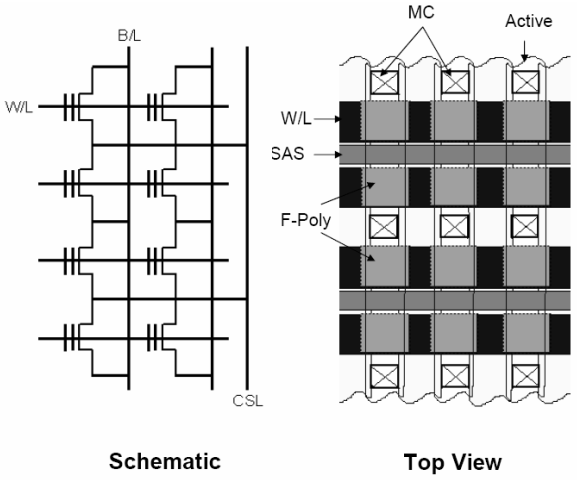
Conventional Flash Memory Structures

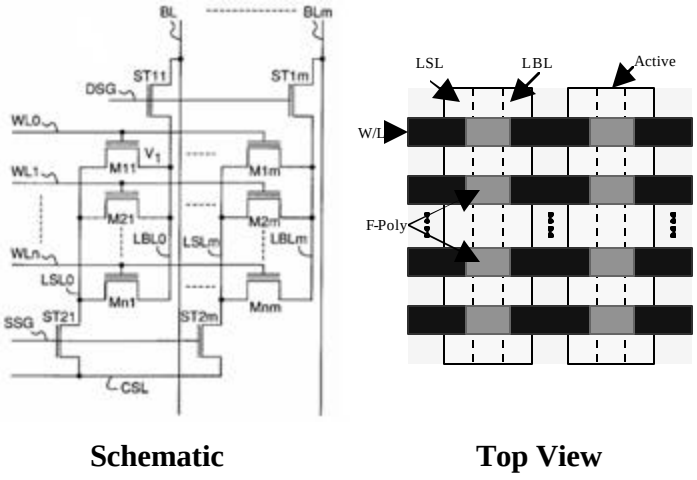
< NAND >



< NOR >



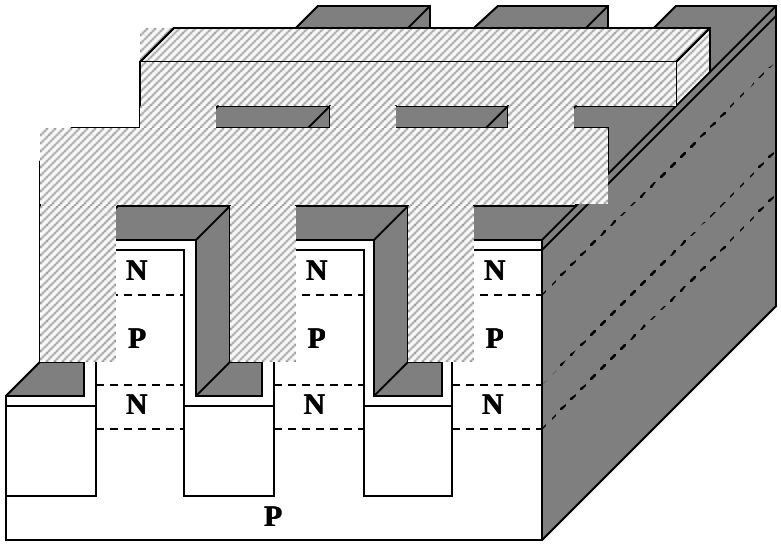
< AND >



	NAND	NOR	AND
program efficiency	high	Low	high
sensing speed	low	high	high
density	high	low	low

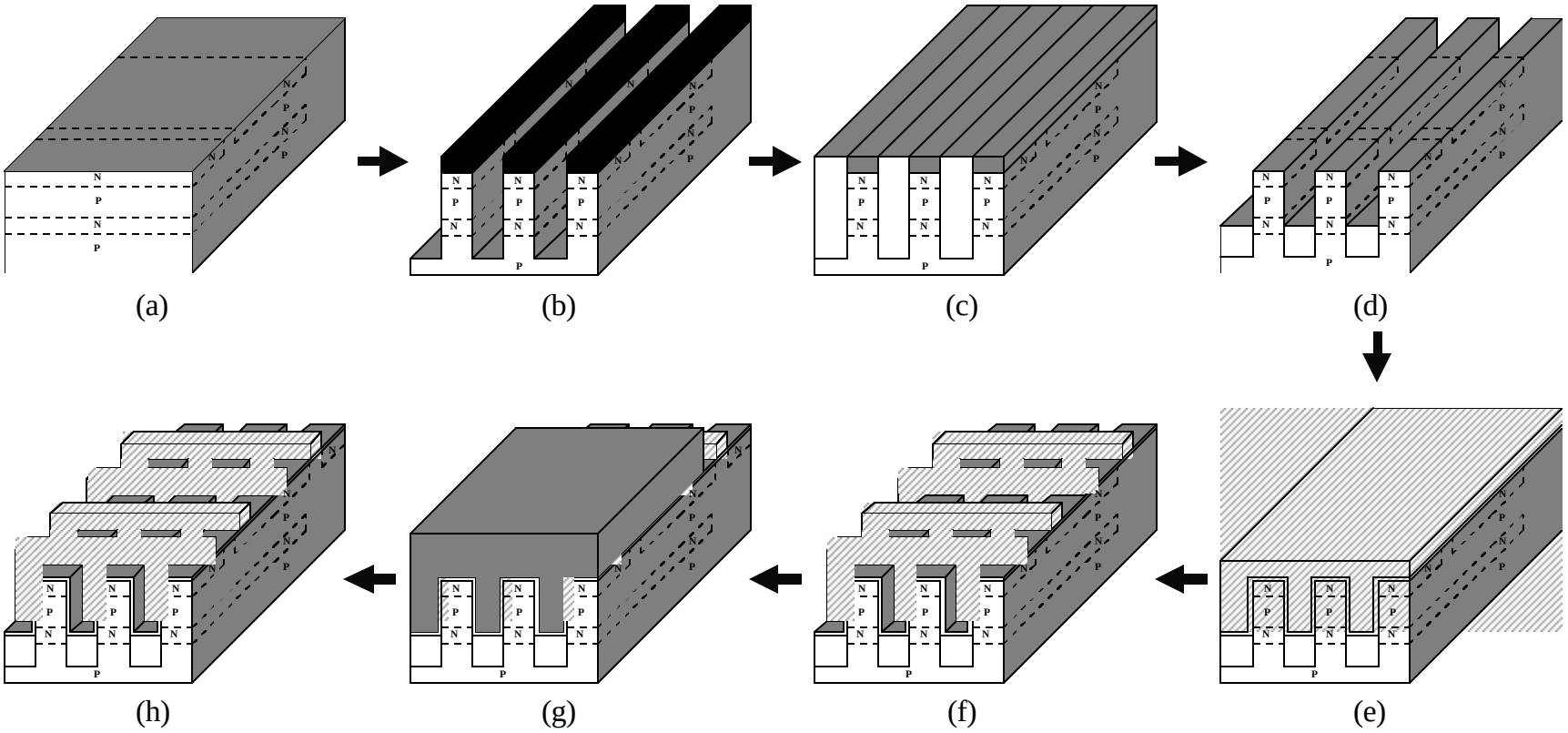
Vertical AND Structure (1)

- Memory cell device with vertical and double gate structures
  - vertical structure, S/D junctions connected by diffusion layer
    → High integration density.
  - double gate structure.
    → High device performance, high sensing speed.



Vertical AND Structure (2)

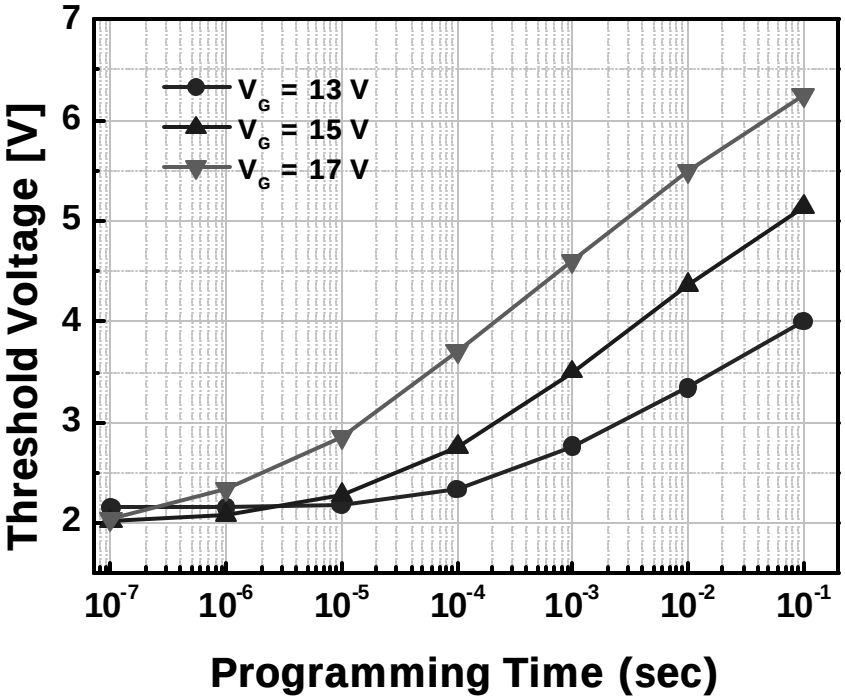
- Fabrication procedure



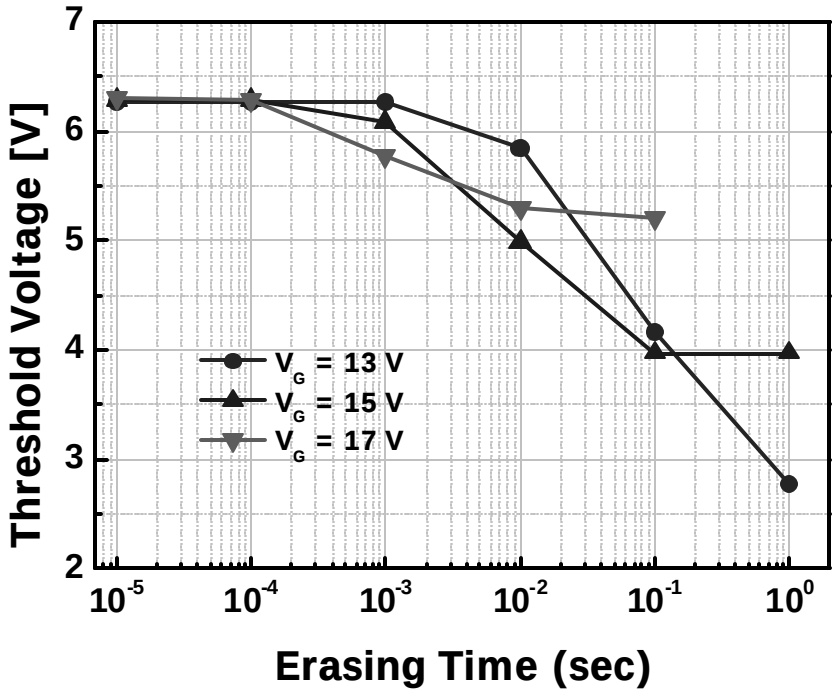
Vertical AND Structure (3)

- Program/erase characteristics

<Program characteristics>



<Erase characteristics>



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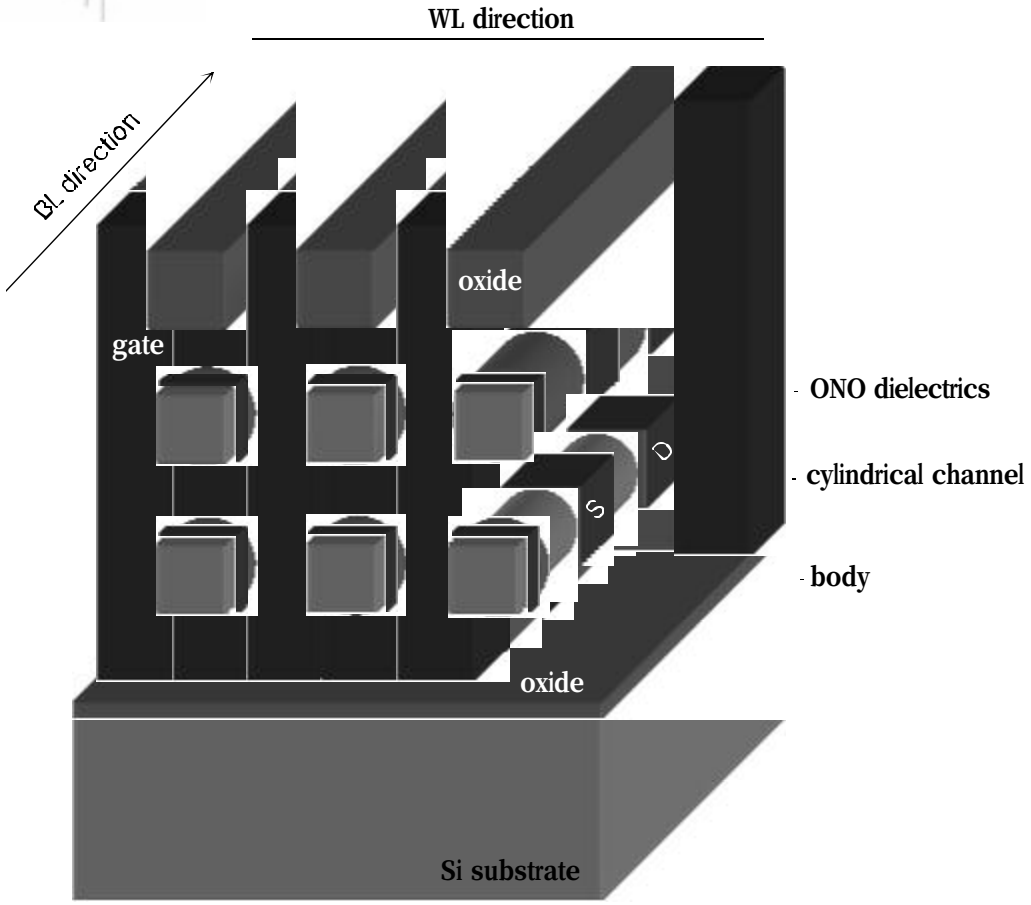
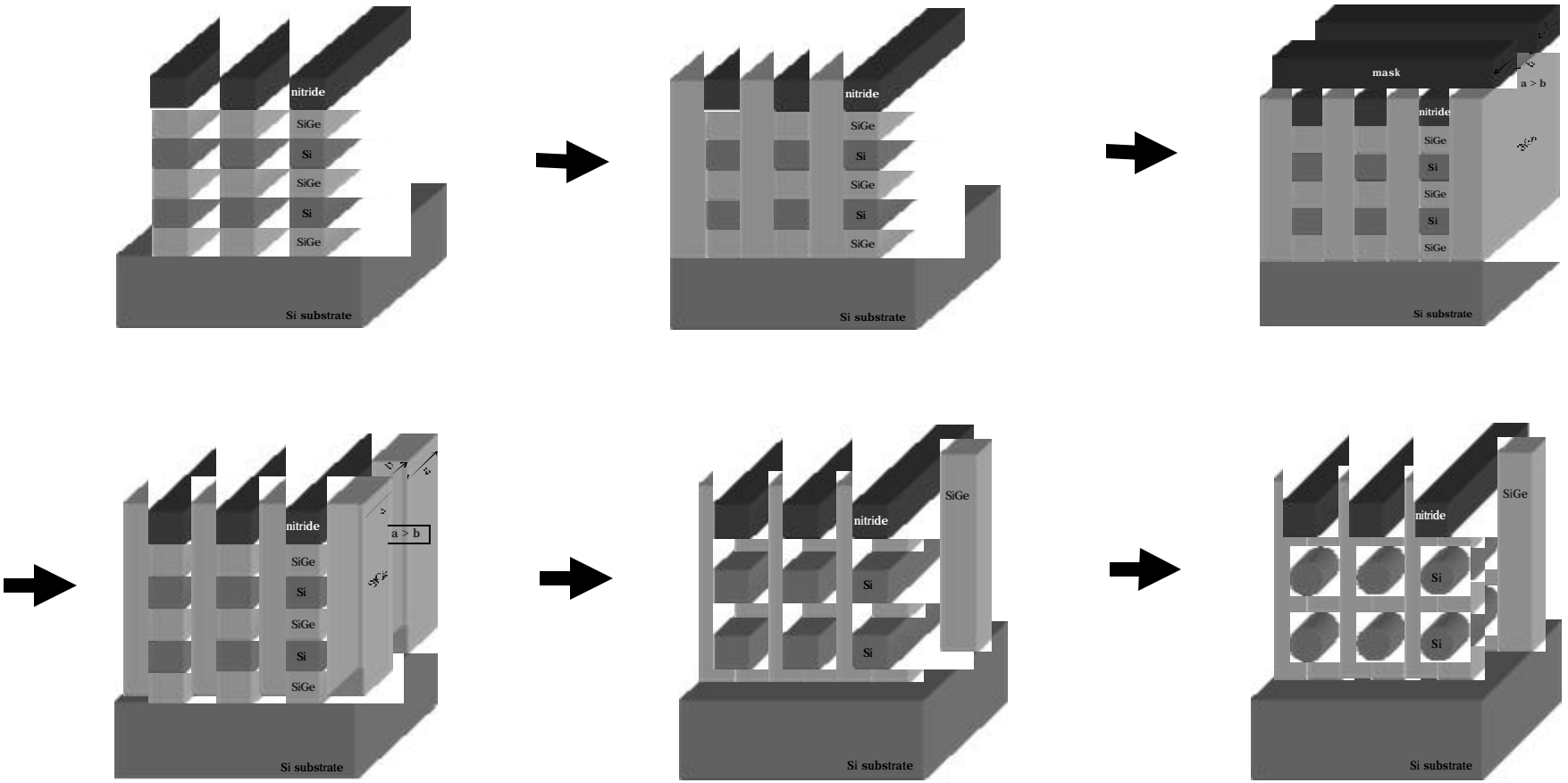
STAR NAND Flash Structure (1)



- Stacked bit-lines
  → high density
- Cylindrical channel and gate-all-around cell structure
  → high performance
- Single-crystal Si channel
  → high performance, uniformity, reliability

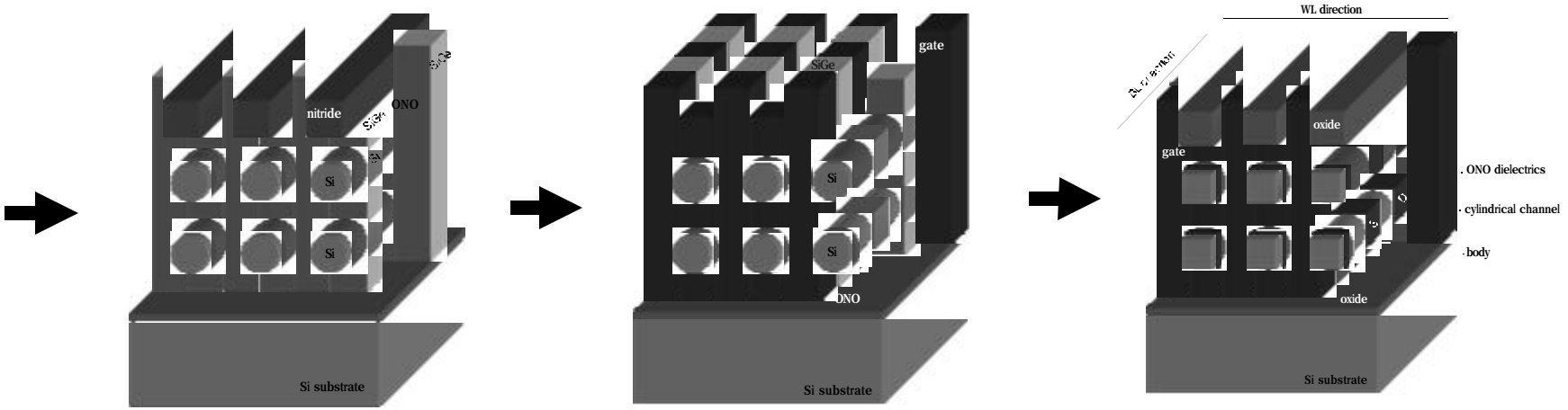
STAR NAND Flash Structure (2)

- Fabrication procedure



STAR NAND Flash Structure (3)

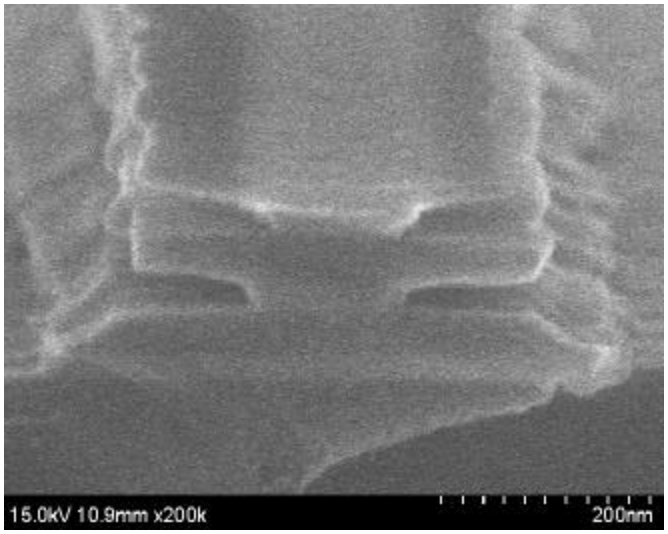
- Fabrication procedure (continued)



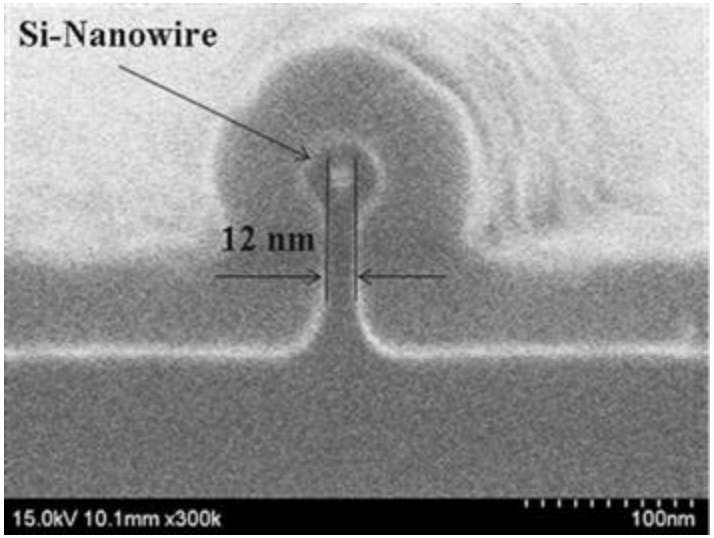
STAR NAND Flash Structure (4)

- Components of stack and nanowire implementation

<Selectively etched SiGe>



<Rounded Si nanowire>



Conclusions (1)

- **Charge trap flash memory including SONOS structure is a promising candidate for the next generation high density flash memories.**
- **For NAND application, arch SONOS flash memory is proposed for field concentration and suppression of back tunneling and is successfully demonstrated.**
- **For NOR application, cone SONOS flash memory is proposed for field and current concentration, and the fabricated cell shows superb electrical characterics.**

Conclusions (2)

- **For AND application, vertical AND structure is proposed for drastic reduction of cell size and the feasibility is demonstrated.**
- **For further increase of density, STacked ARray (STAR) NAND array is proposed.**