Beyond transistor scaling: new devices for low-energy information processing

Prof. Tsu-Jae King Liu

Department of Electrical Engineering and Computer Sciences
University of California, Berkeley CA 94720-1770
tking@eecs.berkeley.edu

Abstract

The rapid growth of the semiconductor industry over the past four decades was enabled by the steady miniaturization of the transistor with each new generation of CMOS technology, which provided for continual improvements in integrated-circuit performance and cost per function. Transistor scaling has slowed recently, however, due to fundamental limits leading to increases in power density. The key to solving this CMOS energy crisis is the development of improved transistor designs, ones which can achieve the required level of performance with lower off-state leakage than a conventional planar CMOS transistor. Such devices can be achieved through improved transistor geometry to improve electrostatic integrity, advanced dielectric materials to optimize the capacitive coupling between the control (gate) electrode and the transistor channel, and/or new transistor designs which do not rely on thermionic emission over a potential barrier. This talk will give an overview of advanced semiconductor device designs that can potentially overcome the energy-efficiency limitations of CMOS technology to help usher in the Age of Ubiquitous Computing.