A Nanoscale Electromechanical Configuring Switch

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Achieving electrically controlled mechanical switching at the nanoscale is of interest for low power, low leakage, and reconfigurable applications. Among issues in nanoscale electronic transistors are tunneling related effects caused by charge injection/impurities and the increase of off-current from the electrodynamics of nanoscale resulting in deteriorating on/off current ratio and poor standby power dissipation. One way of avoiding these limitations of size-dependent electrical effect can be avoided or mitigated using mechanical approaches where dimensions are changed during electrical use. References 1 and 2 show examples of proto-typical nanoscale switches.

In this work, we have employed a mechanical element that forms a channel when moved by electrostatic force leading to current transport between source and drain (Figure 1). What is particularly interesting, scientifically, is the coupling of electrical and mechanical forces at nanoscale, and the resulting characteristics. This is a regime that has not been explored and understood in the community and is the focus of this effort.

Electrostatic force, determined by capacitive coupling of capacitances C_{CS} and C_{GC}, is proportional to V_{CS}^2. This force pulls-in the cantilever at a bias condition called pull-in voltage condition where the source and drain are bridged by a conducting channel. By modulating the spatial extent, this mechanical switching transistor provides a straightforward way of reducing off-state current and short-channel effects of nanoscale transistors. A single lithography step self-aligned process makes this approach particularly appealing for designs requiring a configurable switch. We achieve, using oxidation and single step lithography, silicon pillars with high aspect ratios employing a simple top-down approach. There are several variations possible to this approach, e.g. use of a more flexible materials for a pillar (conducting polymers or polymer-metal nano-composites for a pillar/gate) to affect the voltages by changing the modulus. Another is a device configuration with a side gate (G') which potentially allows for additional control but decreases the net force between source/drain and conducting channel, thus increasing the voltage of initial actuation. Figure 2 shows the SEM images of devices with/without a side gate using a single lithography process and a configuration switch that has been set. This work will summarize the theoretically explored and experimentally observed characteristics of the device.

Critical device design parameters to be considered for low power and low leakage operation include the pillar height (H), aspect ratio and isolation insulator thickness (N). Even though H scales with the voltage most effectively, aspect ratio is limited due to the process issues. Our devices have the aspect ratio of ~100. The insulator thickness (N) needs to be optimized for electrostatic force without causing any breakdown and leakage. Area ratio (A_{rel}) has more room for improvement and is a more scalable parameter. Increasing A_{rel} is achieved by retaining a silicon layer underneath the channel by protecting it from oxidation using a nitride sidewall (Figure 1). Our experimental structures achieve switching below 15 V at sub-200 nm gaps.

[1] Q. Li et al., Nanotechnology 18, 315202 (2007)
[2] J. E. Jang et al., Nature Nanotechnology 3, 26 (2008)

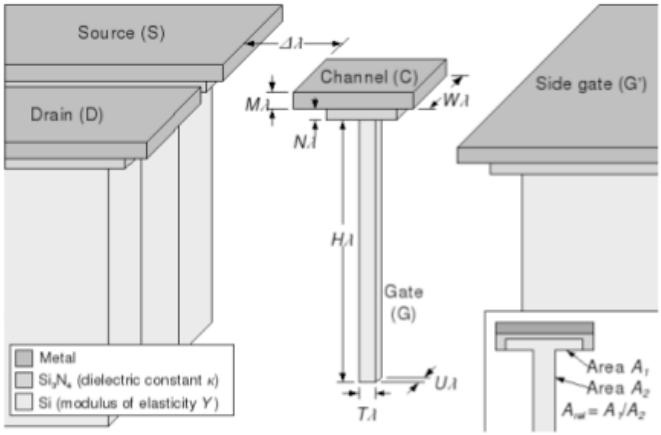

Figure 1. Schematic of electro-mechanical switching transistor and dimensionless scaling parameters

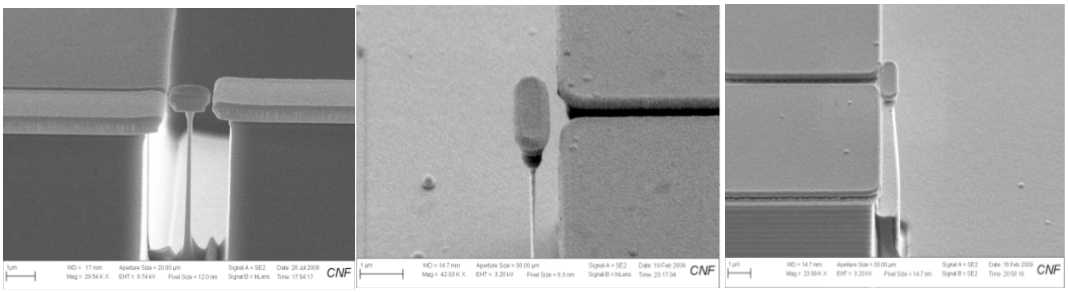

Figure 2. SEM images of devices with/without side gate, and an example of connecting following actuation.