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Ultimately Scaled CMOS: DG FinFETs?

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Summary

The well-publicized roadmap of the Semiconductor Industrial Association (SIA) projects, now via a "More than Moore" law, CMOS technology to be scaled to physical gate lengths (L_g) of <10nm by about 2020. Currently, the mainstream CMOS devices are the bulk-silicon MOSFET and the partially depleted SOI MOSFET, both of which, now with L_g ~ 40nm, require very high body/channel doping densities (N_B) and gradients for control of short-channel effects (SCEs). However, because of uncontrolled, random doping fluctuations (RDF), these conventional MOSFETs, even with recent performance boosters such as strained channels and high-k dielectrics, are near their scaling limit. A new, unconventional CMOS device will be needed to reach the end of the SIA roadmap.

The new devices now receiving the most attention are the planar fully depleted (FD) SOI MOSFET, with a thin BOX and underlying ground plane (GP), and the quasi-planar FinFET. Both devices use undoped, ultra-thin bodies (UTBs), and thus avoid the RDF effects of N_B. We do not believe the former device will reach the end of the roadmap because of complex processing/layout issues related to the selective GPs, perhaps with sizeable biases, and tuned dual-metal gates, with work functions dependent on L_g. The latter requirement stems from the intrinsically high threshold voltage (V_t) of the thin-BOX/GP FD/SOI device (~0.6V for long L_g and midgap gate).

The FinFET is, in our opinion, the device most likely to carry CMOS to the end of the roadmap. It can be designed pragmatically to simplify the processing, yet still perform well and be scalable to L_g < 10nm. We define nanoscale *pragmatic-FinFET* CMOS by the following features: (i) on SOI; (ii) undoped fin-UTBs; (iii) double-gate (DG); (iv) only one (~midgap) gate metal; (v) not strained; (vi) no high-k dielectric; and (vi) gate-source/drain underlap. The latter feature, which gives added SCE control, is effected by optimal S/D processing that defines the lateral doping profile in the extensions, and perhaps enables controlled dopants in the channel for V_t adjustment. Unique features of the pragmatic DG FinFET that underlie its performance include DG control of the electrostatics, bulk (a.k.a., volume) inversion, bias-dependent effective channel length, and high carrier mobility. The main technological issues to be addressed now are the noted S/D processing, control of tall, thin fins, and assurance of the high mobility for short L_g.