The NSF Nanoscale Science and Engineering Center for High-rate Nanomanufacturing
www.nano.neu.edu

Directed Assembly of Nanoelements for the Nanomanufacturing of Devices

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Beyond the ITRS Roadmap

Transistor Scaling and Research Roadmap

Source: Intel
CMOS Scale Limits and Power Considerations

- If the thermal dissipation problem is not solved, we will have to forgo the speed and density that come with nanoelectronics even if we can build very fast and small transistors.
- Even if charge-based devices can be built smaller than CMOS, they can not be operated faster or be cheaper than CMOS.
- Thermal scaling will decide the scaling limit for CMOS. This also means that new (non charge-based) logic devices will be required to go beyond 2020 (beyond CMOS).

What is the solution?

- A new energy efficient, high performance, scalable switch with gain and operational reliability at room temperature that are compatible with CMOS process and architecture.

Nanoelectronics Challenges; Examples of Non-Charge Based Switches

- The room temperature limit is; for 1.5 nm, a switching energy of 0.017 electron volts, and a switching speed of 0.04 pico second.
- The power needed for a 100% duty cycle at the considered limit is a power density of 3.7 million Watts/cm².
- If we consider a 1% duty cycle and 1% active transistors, we get a total power density of 370 W/cm².

Zhirnov, V., et. al., Proceedings IEEE, Nov. 2003

Many Potential solutions Exist
Alternative state variables
- Spin-electron
- Photon
- Phase
- Quantum state
- Magnetic flux quanta
- Mechanical position
- Dipole orientation
- Molecular state
- Orbital symmetry
- Order/disorder

Extending CMOS Crossed Nanowire Structures:
Silver Nanoswitch
Could nanoelectronic devices based on ionic conductors replace silicon?
Terabe, K., Hasegawa, T., Nakayama, T. & Aono, M.

Single Wall Carbon Nanotube Memory Device,

The Path from Nanoscience to Nanomanufacturing
Past and present:
Manipulation of few atoms and SWNTs
STM 1981
AFM 1986
STM manipulation of atoms 1989
AFM manipulation of a SWNT 1999
Molecular logic gate 2002

Future:
Manipulation of billions of atoms and SWNTs
Templates
High rate
High volume
Reliability
Informed public and workforce
Environmentally benign processes
Biosensor
Memory device

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CHN Vision

High-rate Directed Self-Assembly of Nanoelements

State of the Art:
- A pattern is transferred into photoresist. A single mask can be used for thousands of Wafers.

Nanoimprint:
- A pattern is transferred into photoresist using a mold. A mold could also be used for thousands of wafers.

Nanotemplate:
- A layer of assembled nanostructures is transferred to a wafer. A template could also be used for thousands of wafers.

CHN Vision: Guided Self Assembly

High-rate/High-volume Guided Self-Assembly of Nanoelements

State of the Art:
- Pure self-assembly produces regular patterns

Challenge:
- Nanotemplates enable guided self assembly
Electrostatic Assembly of Nanoparticles

Assembly of 300 nm PSL particles (negatively charged) on positively-charged Au microwires

Current Template size is:
2.25 - 4.00 cm²

Microfingers on the template.

The dependence of surface charge on particle size and mol concentration of liquid.

50 nm PSL particles assembled in trenches. (left) partial coverage in 260 nm wide trenches at 2 V for 30 seconds; (right) full coverage in 260 nm wide trenches at 3 V DC for 90 seconds.

50 nm PSL nanoparticles assembly in multi-layers

50 nm particle assembly in a monolayer

Electrostatic Assembly of Nanoparticles

Computational fluid dynamic (CFD) model to aid in preparing templates with uniform deposition
Electrostatic Assembly of Nanoparticles

10-15 nm silica nanoparticles in 30 nm trenches

50 nm PSL nanoparticles in 50 nm trenches

Electrostatic Assembly of SWNT

Positive Au wire

Alignment of carbon nanotubes using 1 MHz AC supply

Negative Au wire

Non-aligned assembly of SWNT on microwires
Electrostatic Assembly of SWNT in Trenches

Assembly into sub 100 nm trenches with 5 V for 1 minute

SWNTs Assembled within polymer trenches

SWNT on gold after dissolving polymer

Highlights of Guided Self-Assembly of Polymer Melts at High Rates

Use nanotemplates in high rate environment

Nanotemplates used as tooling surface in high rate process

Injection Molder

Polymer A + B Blends/block copolymers

Complex shapes can be manufactured
Assembly of Polymer Using Electrostatically Addressable Templates

Conducting Polymer – Polyaniline (PANI)

Transfer of assembled PANi nanowires to PS and PU polymer substrates

Nanoscale Characterization and Reliability Testbed Highlights

Innovative MEMS devices characterize nanowires (also nanotubes, nanorods and nanofibers) and conduct accelerated lifetime testing allowing rapid mechanical, electrical, and thermal cycling during UHV SPM observation
High Density Memory Chip

Current process
- Uses conventional optical lithography to pattern carbon nanotube films
- Switches are made from belts (ribbons) of nanotubes

Electrodes (~100nm with 300 nm period)

ON state (Nantero, 2004)

Nanotemplate will enable single CNT electromechanical switch

Testbeds: Memory Devices and Biosensor

Q1b. How does concept design translate into high-rate manufacturing and how is it validated through the testbeds?

Use Templates in High Rate Nanomanufacturing

Create Nanotemplates: Design, Manufacture, and Functionalize

Carbon nanotube on silicon trenches

Carbon nanotubes assembled from solution

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High Volume Wet Chemical Synthesis of SWNTs with Uniform, Tunable Properties

1. Cyclacene precursors, both acenes and fullerene-acene adducts, have been synthesized.

Concurrent Assessment Processes

- Full systems analysis to assess technology development of nanotemplating
- Create environmentally benign processes and products
- Identify significant cost barriers
- Inform policymakers and generate public discourse during process development
- Establish comprehensive assessment practices for success of technology
Partnerships

Industry

Government Labs

Facilities

Researchers

Students

Faculties

Researchers

Students

Universities and other Outreach

Wolfe Laboratories, Inc.
Foster-Miller
Nantero
tsi
tyco electronics
Konarka technologies
Motorola
intel
DRAPER
Bentley

NEU

SEM, fabrication, nanoscale contamination control

UML

High volume polymer processing

UNH

Synthesis, self-assembly

Characterization labs at NEU, UNH and UML:
material characterization and analysis including STM/AFM, NSOM,
SIMS, SEM, TEM, XRD, AEM, XPS,

Team Strength and Synergy

Semiconductor & MEMs fab
10,000 ft² class 10 and 100 cleanroom
6 inch completer Wafer fab, nanolithography capabilities

Plastics processing labs
40,000 ft² +
Compounding, and forming equipment

Fully-equipped synthetic labs
10,000 ft² +
A unique partnership
CHN’s Path to Nanomanufacturing

Testbeds: Memory Devices and Biosensor
Level 3

Use Templates in High Rate Nanomanufacturing
Level 2

Create Nanotemplates: Design, Manufacture, and Functionalize
Level 1

Reliability & Defects, and Modeling

Societal Impact and Outreach

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