INVITED LECTURE 20th U.S.-Korea Forum on Nanotechnology, Sept. 14-15, 2026

From Atoms to Architectures: Two-Dimensional Materials for Energy-Efficient AI and Emerging Computing

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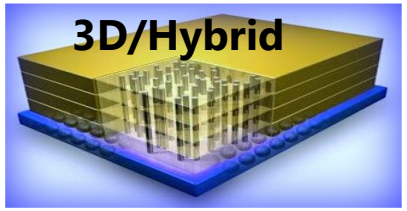
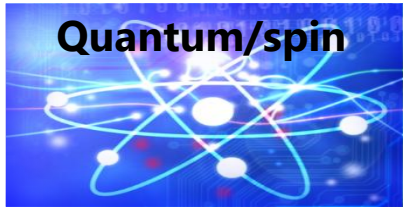
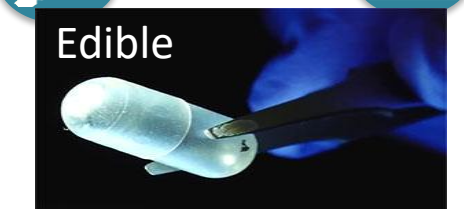
With Young Hee Lee
August 21, 2026, HBUT, Wuhan

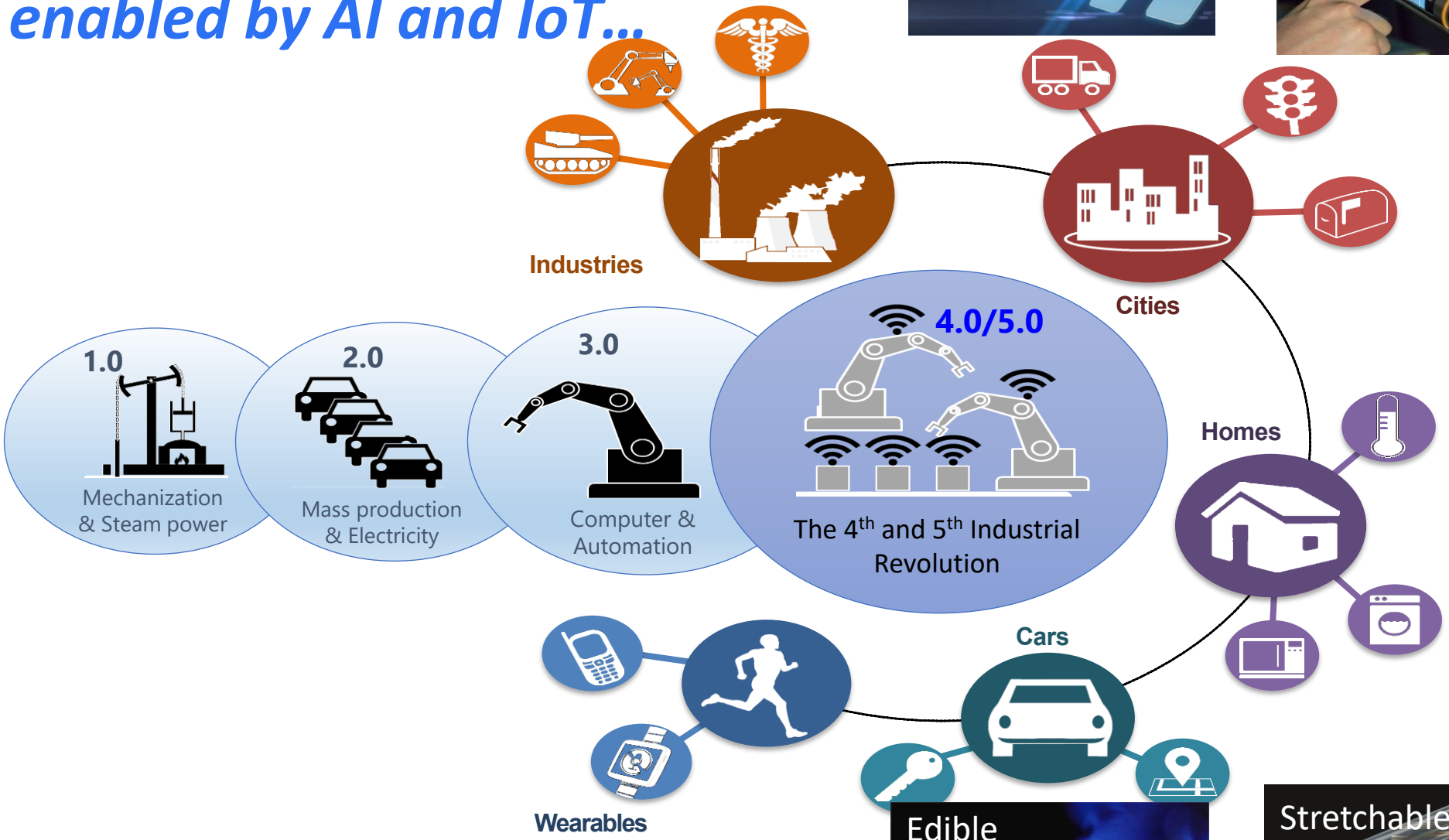
Next-gen Electronics

- enabled by AI and IoT…









The NEED: small and energy-efficient

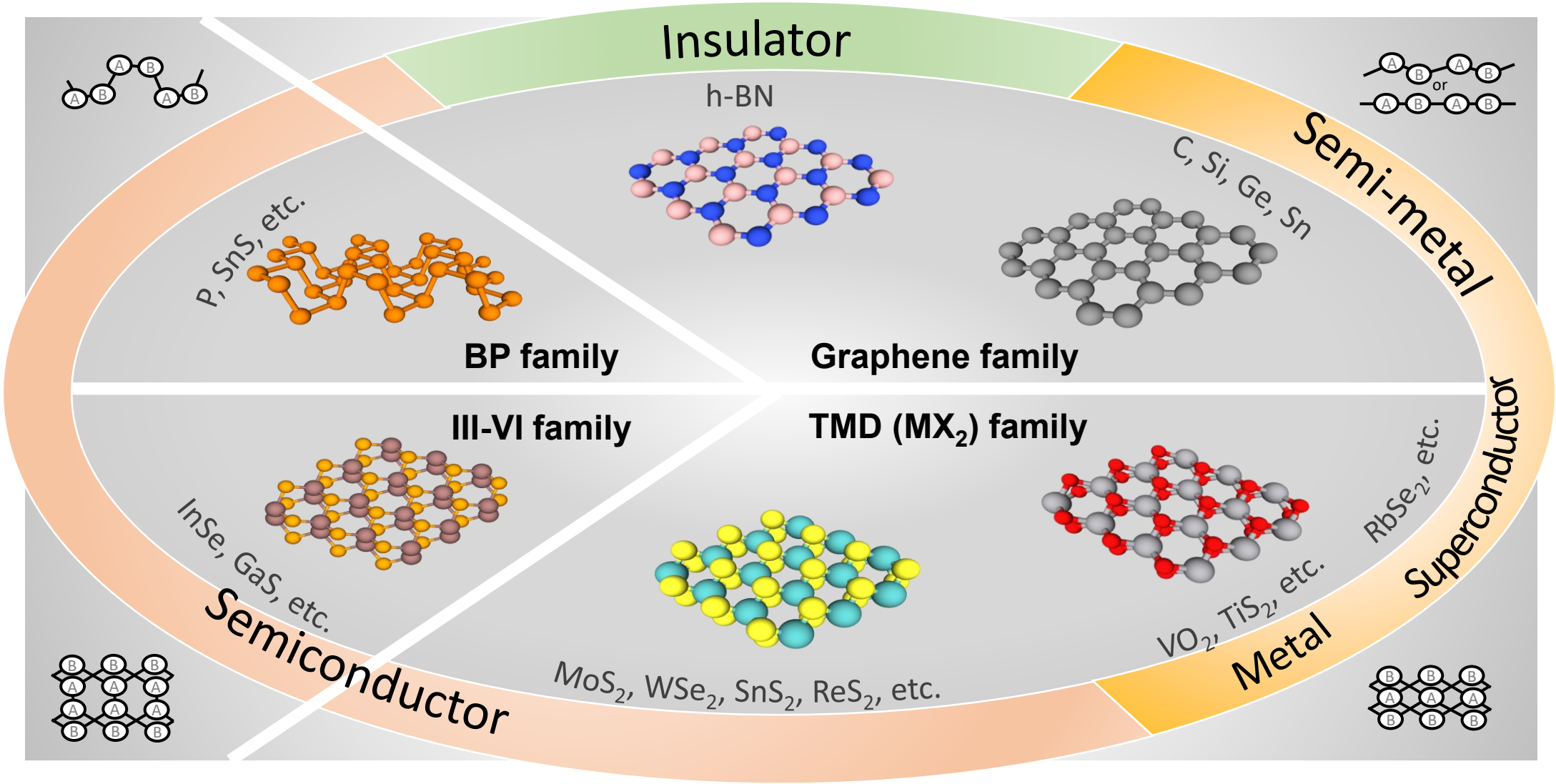
Energy efficiency also enables true invisibility…

How do we design energy-efficient electronics?

I will use 2D materials:
Graphene & beyond

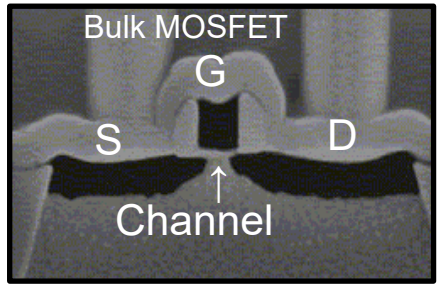
2D van der Waals materials - atomically-thin, transparent, flexible, biocompatible…

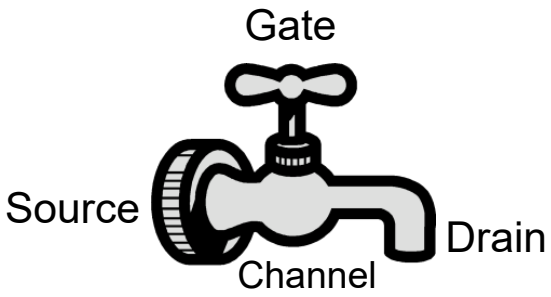
P. Ajayan, P. Kim and K. Banerjee, ***Physics Today***, Sept 2016.



Energy-efficient transistors with 2D materials

IEEE Trans. Electron Devices, 62(11), Nov 2015.





➢ **How to scale channel length below 5 nm?**

Natural length:

$$\lambda = \sqrt{a\, t_{ch} \cdot t_{ox} \cdot \frac{\varepsilon_{ch}}{\varepsilon_{ox}}}$$

steepness of the potential variation from S/D to Channel

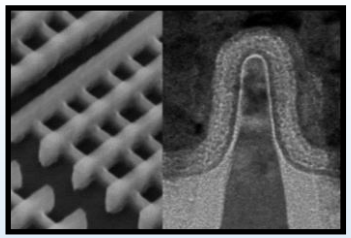
For good electrostatics:

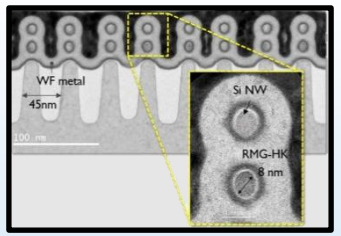
$$L_{ch} \geq (3-5)\lambda$$

Need to reduce λ!!

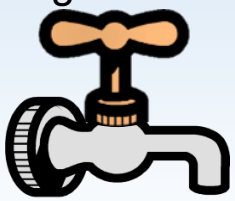
Enhance the Gate

$a \quad t_{ox} \quad \varepsilon_{ox}$

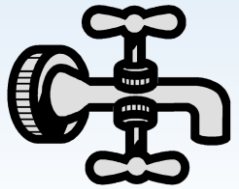




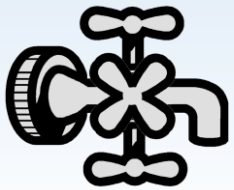
High-*K* MG



FinFET/Tri-gate



NW/NS Gate-All-Around



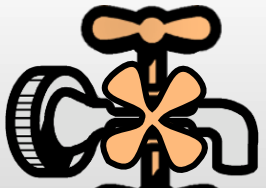
Thin the Channel

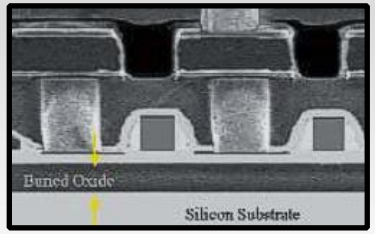
t_{ch}

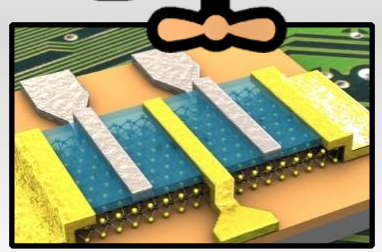
PDSOI

FDSOI

2D FET







Why 2D ? – 2D semiconductors (MoS_2, WSe_2, etc) offer atomically-thin channel, and **other favorable properties**, hence, extreme scalability (**smallest λ**)

Physics of Contacts to 2D Semiconductors

Edge, Top, and Hybrid (edge+top) contacts…

PHYSICAL REVIEW X 4, 031005 (2014)

Computational Study of Metal Contacts to Monolayer Transition-Metal Dichalcogenide Semiconductors

Jiahao Kang,[1] Wei Liu,[1] Deblina Sarkar,[1] Debdeep Jena,[2] and Kaustav Banerjee[1]
[1]*University of California, Santa Barbara, California 93106, USA*
[2]*University of Notre Dame, Notre Dame, Indiana 46556, USA*
(Received 27 June 2013; revised manuscript received 23 February 2014; published 14 July 2014)

Among various 2D materials, monolayer transition-metal dichalcogenide (mTMD) semiconductors with intrinsic band gaps (1–2 eV) are considered promising candidates for channel materials in next-generation transistors. Low-resistance metal contacts to mTMDs are crucial because currently they limit mTMD device performances. Hence, a comprehensive understanding of the atomistic nature of metal contacts to these 2D crystals is a fundamental challenge, which is not adequately addressed at present. In this paper, we report a systematic study of metal-mTMD contacts with different geometries (top contacts and edge

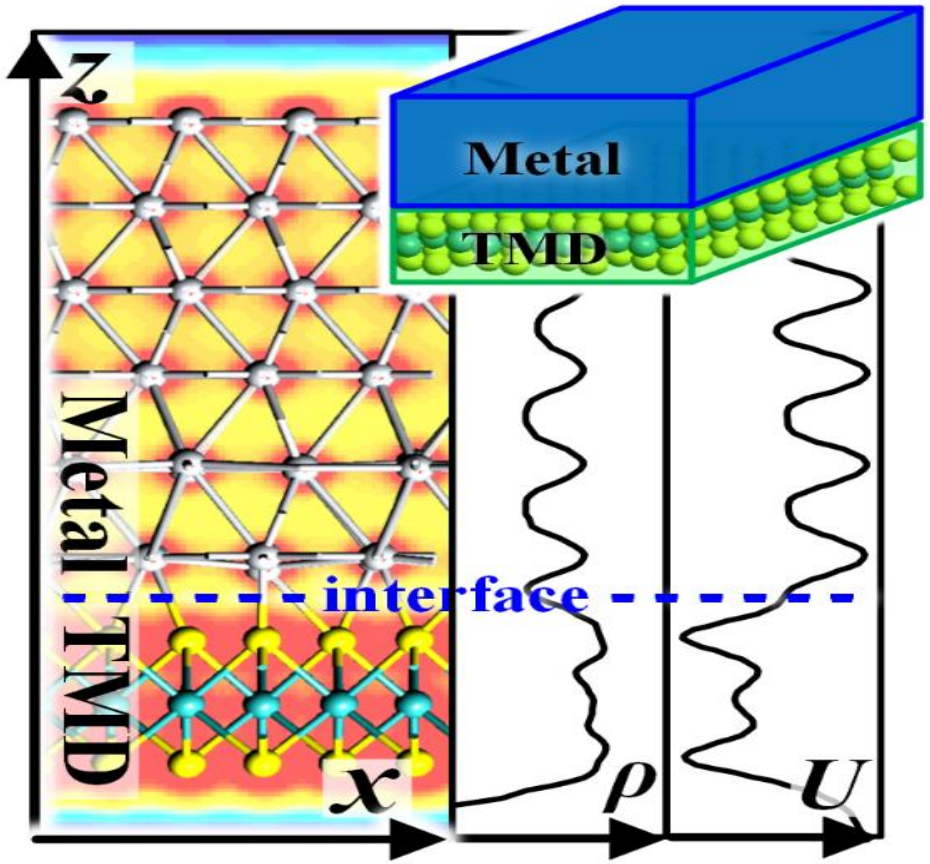
nature materials
REVIEW ARTICLE
PUBLISHED ONLINE: 20 NOVEMBER 2015 | DOI: 10.1038/NMAT4452

Electrical contacts to two-dimensional semiconductors

Adrien Allain[1], Jiahao Kang[2], Kaustav Banerjee[2]* and Andras Kis[1]*

The performance of electronic and optoelectronic devices based on two-dimensional layered crystals, including graphene, semiconductors of the transition metal dichalcogenide family such as molybdenum disulphide (MoS_2) and tungsten diselenide (WSe_2), as well as other emerging two-dimensional semiconductors such as atomically thin black phosphorus, is significantly affected by the electrical contacts that connect these materials with external circuitry. Here, we present a comprehensive treatment of the physics of such interfaces at the contact region and discuss recent progress towards realizing optimal contacts for two-dimensional materials. We also discuss the requirements that must be fulfilled to realize efficient spin injection in transition metal dichalcogenides.

Contacts/Interfaces for 2D-Device Design



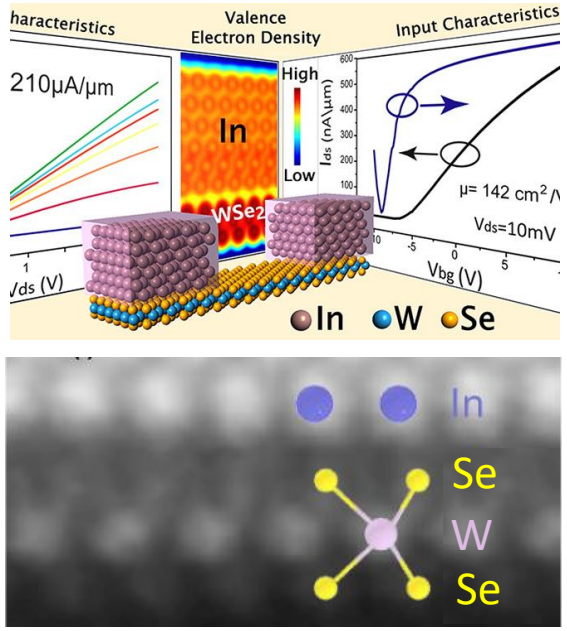
Phys. Rev. X, 4(3), 031005, 2014.
Nat. Mater., 14(12), 2015.

- ***Ab-initio* framework** for metal–TMD contacts
- **Identified the true origin of contact resistance:**
  - van der Waals gap (tunnel barrier)
  - strong Fermi-level pinning
  - high sheet resistance of 2DS
    - —not work function alone
- Revealed importance of **hybridization and metallization**
- **Laid scientific foundation for** near-quantum-limit contact resistance

Established paths to high-performance 2D transistors…demonstrated by Intel, TSMC, etc.

Foundational Theory and Experiments - 2D-FETs for post-Si era

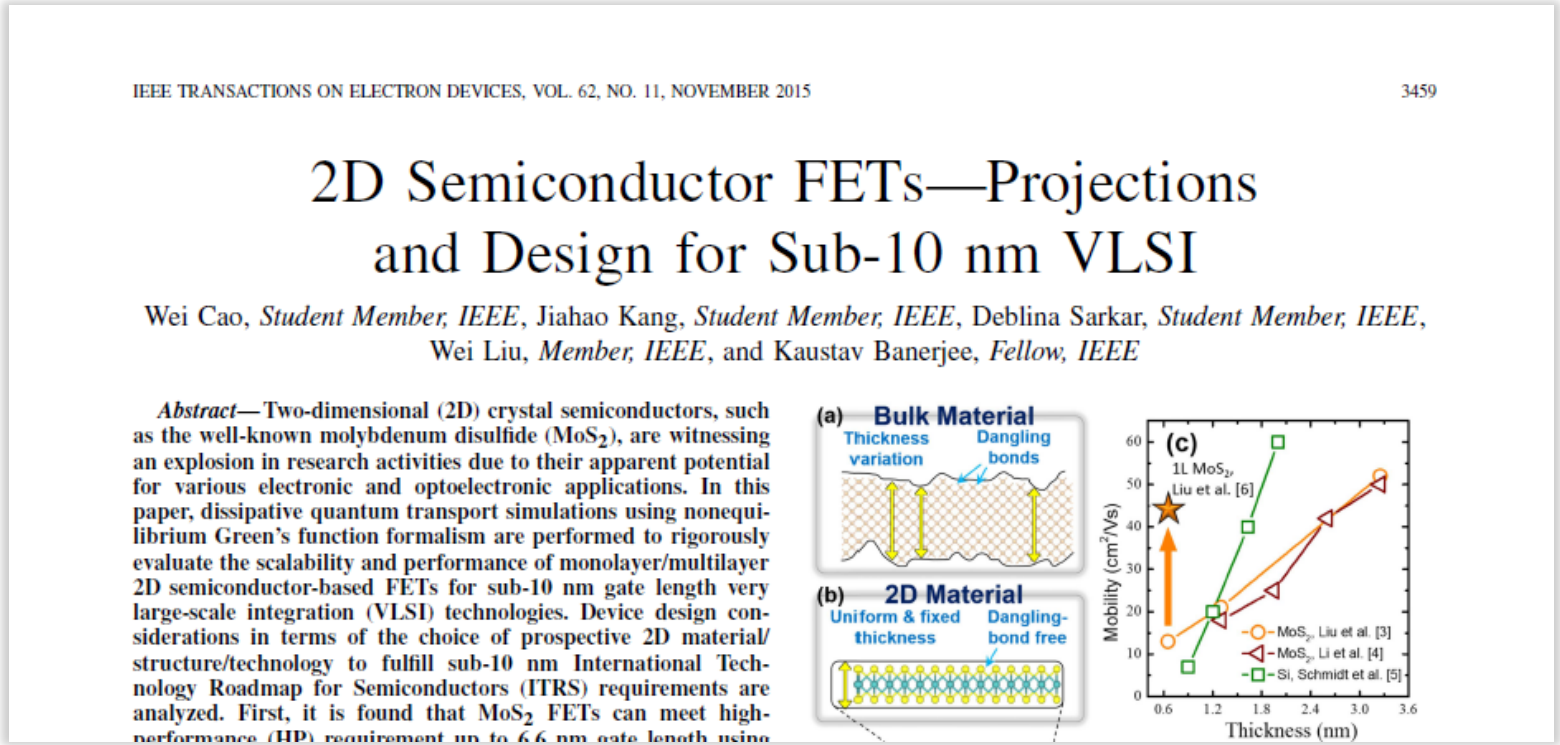
First 1L-WSe_2 FET (n-type)



Nano Lett. *13(5), pp. 1983-1990, 2013.*

Comprehensive Predictive Technology Scaling Projections using VLSI Relevant Metrics

WSe_2 and WS_2 good for both LP and HP FETs



IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 62, NO. 11, NOVEMBER 2015 3459

2D Semiconductor FETs—Projections and Design for Sub-10 nm VLSI

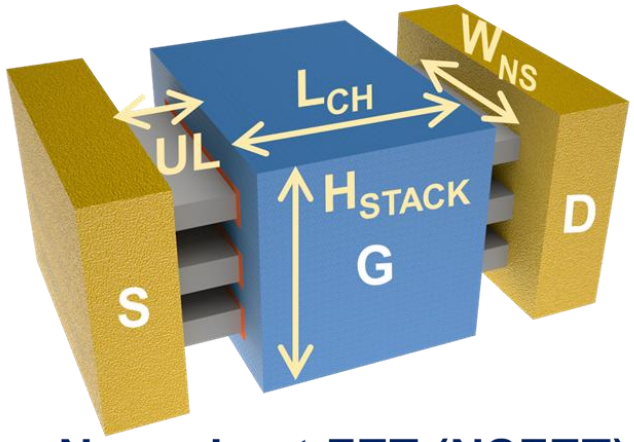
Wei Cao, *Student Member, IEEE*, Jiahao Kang, *Student Member, IEEE*, Deblina Sarkar, *Student Member, IEEE*, Wei Liu, *Member, IEEE*, and Kaustav Banerjee, *Fellow, IEEE*

***Abstract*—Two-dimensional (2D) crystal semiconductors, such as the well-known molybdenum disulfide (MoS_2), are witnessing an explosion in research activities due to their apparent potential for various electronic and optoelectronic applications. In this paper, dissipative quantum transport simulations using nonequilibrium Green's function formalism are performed to rigorously evaluate the scalability and performance of monolayer/multilayer 2D semiconductor-based FETs for sub-10 nm gate length very large-scale integration (VLSI) technologies. Device design considerations in terms of the choice of prospective 2D material/structure/technology to fulfill sub-10 nm International Technology Roadmap for Semiconductors (ITRS) requirements are analyzed. First, it is found that MoS_2 FETs can meet high-**

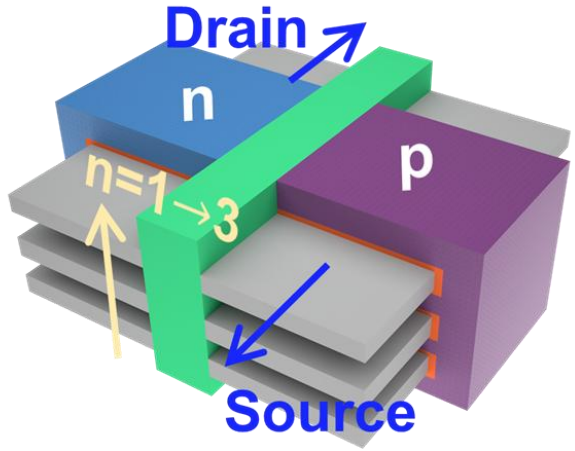
2D-FETs now on all major industrial transistor roadmaps!

Ultimate CMOS Scaling – 3D FETs with 2D

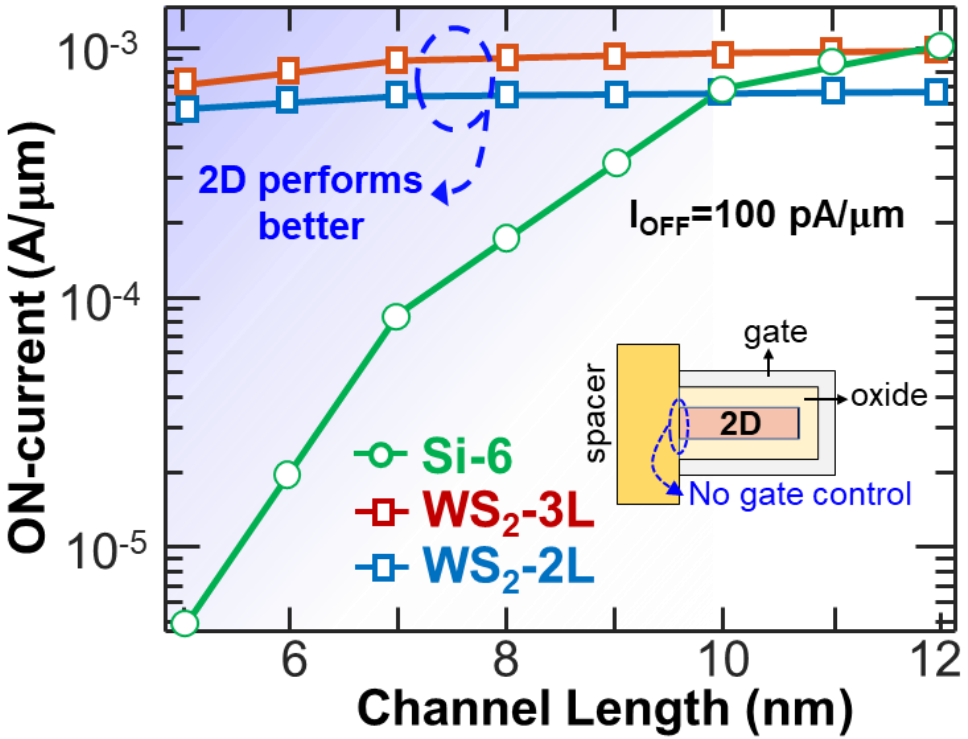
Nature Electronics, 7, 1147–1157, Dec 2024.



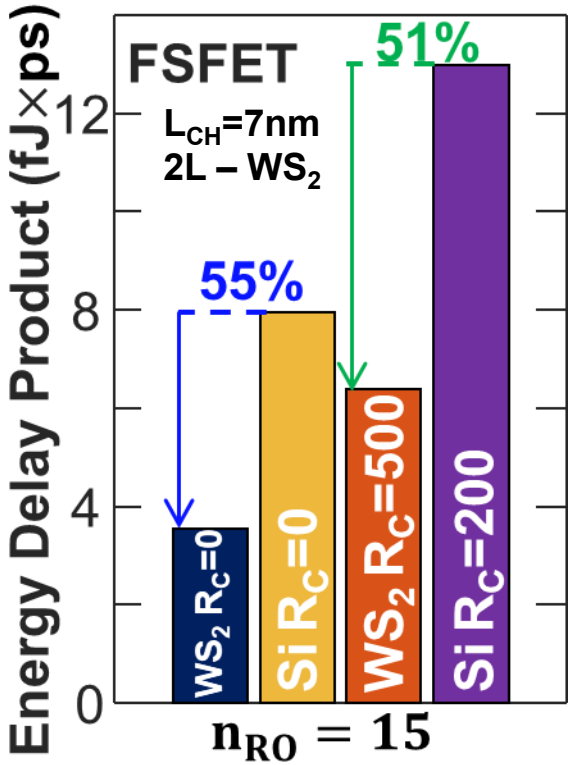
Nanosheet FET (NSFET)



Forksheet FET (FSFET)

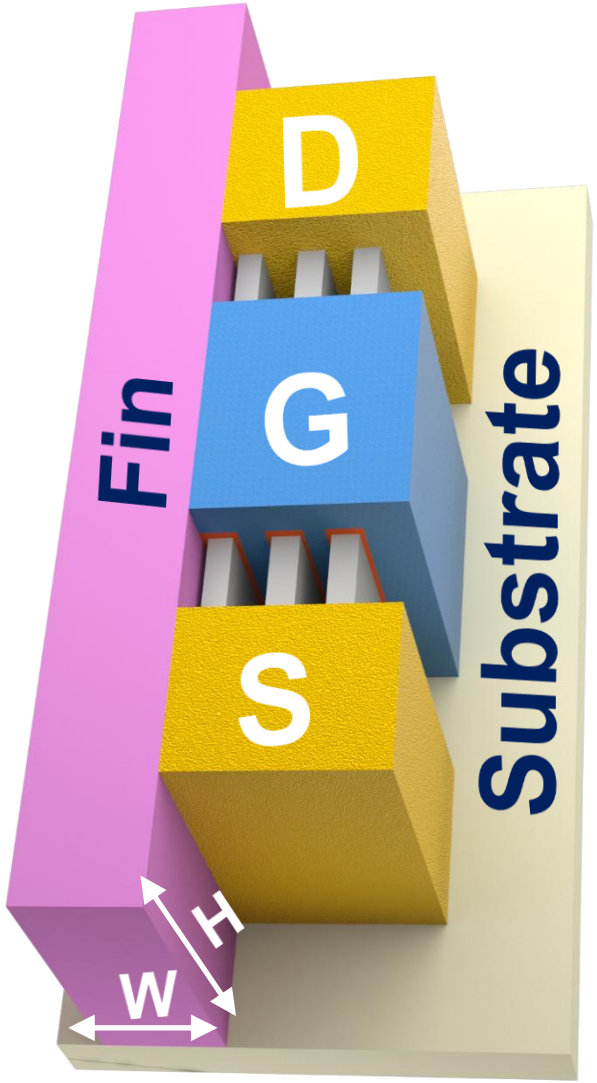


Scalable



Energy-efficient

The Nanoplate-FET – *A new 3D MOSFET uniquely enabled by 2D*



Nature Electronics, 7, p. 1147–1157, Dec 2024.

- Exploits **lateral stacking** of 2D layers, resembling a “stack of plates”
- Enhanced **integration density** by up to 10-fold with iso-performance metrics
- Major **process advantages** over the Nanosheet-FETs
- Varying channel widths w/o increasing **lateral footprint**

News – ***Next-gen 3D transistors transform energy-efficient electronics***

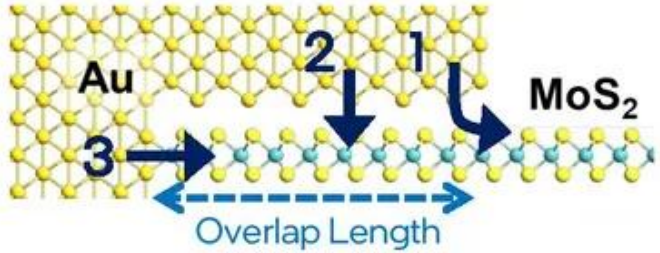
Collaboration with Intel on 3D Gate-All-Around FETs with 2DS

A. Pal et al., ***IEDM*** 2022.

Enabling the engineering of contacts to 2D channel materials

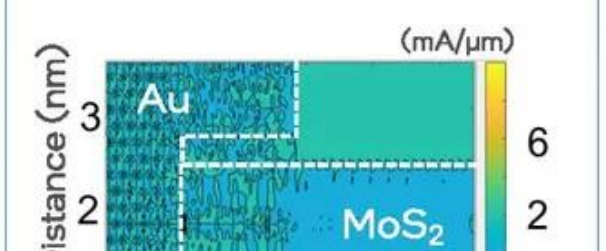
First comprehensive set of numerical and analytical models of 2D contacts

Hybrid contact and its current paths



Contacts are a key limiter to 2D transistor performance

Atomistic simulation of current in a hybrid contact



Atomistic simulations show paths to high performing contacts for 2D transistors

News **-** Intel Charts Course to Trillion-Transistor Chips: 2D Transistor Materials, 3D Packaging Research

Energy-Efficient Transistors with 2D – Beyond CMOS

$$Power = CV_{DD}^2 f + I_{leak} V_{DD}$$

dynamic static

- **How to achieve simultaneous power scaling?**

Supply voltage (V_{DD}) scaling is a powerful knob to reduce power!

$$SS = \frac{\partial V_G}{\partial \psi} \frac{\partial \psi}{\partial \log(I_D)} = \frac{\partial V_G}{\partial \psi} \frac{kT}{q} ln10$$

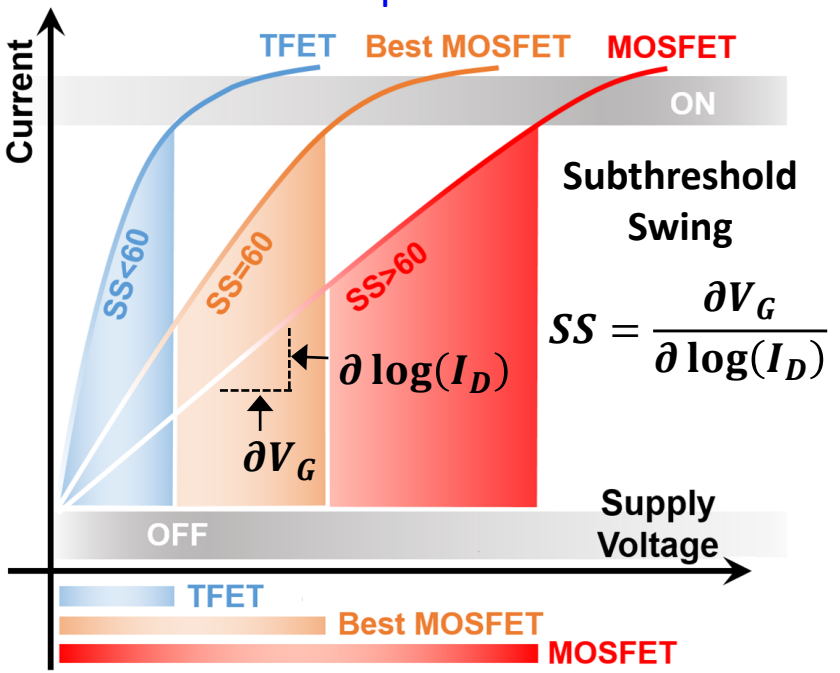
$$I_D \propto exp(q\psi/kT)$$

ψ: channel potential

$$\geq 1 \times 60mV/dec$$

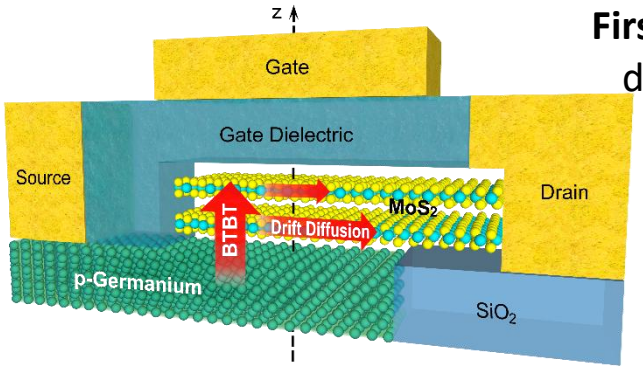
(All MOSFETs – 1D, 2D, or 3D channel materials)

electrostatics current modulation efficiency (transport mechanism dependent)



2D Enabled TFET?

- 2D semiconductors can offer **near-ideal electrostatics, smaller band-tails**
- can be judiciously combined with other 2D or 3D semiconductors to form heterojunction-Tunnel-FETs **offering sub-60 mV/dec**



First 2D-channel TFET offering SS = ~30 mV/dec over 4 decades of drain current and ultra-low OFF current
Nature, 526, 91-95, 2015.

2D-2D Lateral HTJ TFETs can potentially offer superior performance
IEDM 2015, pp. 12.3.1-12.3.4.

2D-TFET: Excellent candidate for low-power computing (neuromorphic, etc) and ultra-sensitive biosensing
(P. Ajayan, P. Kim, K. Banerjee, ***Physics Today***, vol. 69, no. 9, pp. 38-44, 2016)

Brain inspired neuromorphic computing with 2D-TMD TFETs

Collaborative work with Intel…

2D-TFETs with much lower off-state current — can greatly improve power efficiency of neuromorphic chips

Nature Communications 15, 3392, 2024.

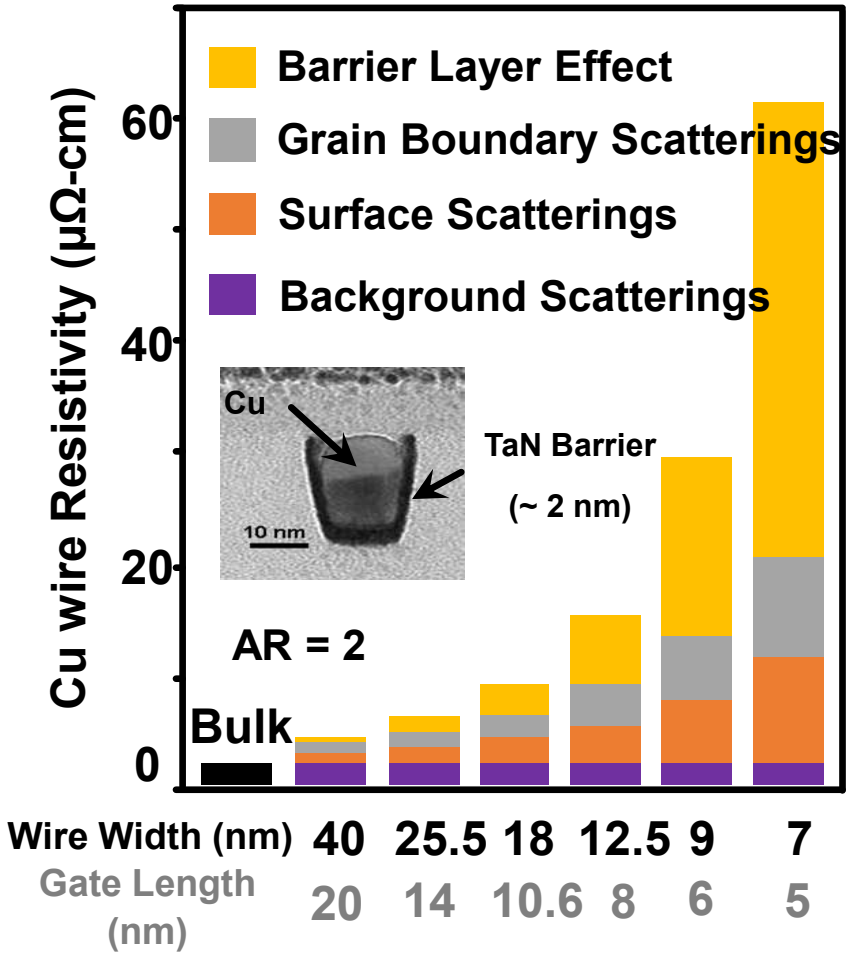
Exciting future of beyond-CMOS energy-efficient transistors

- ***A comprehensive overview of the history, present status, and future of transistors***
- ***co-authored with industry leaders and pioneers***

Interconnect Scaling Challenges

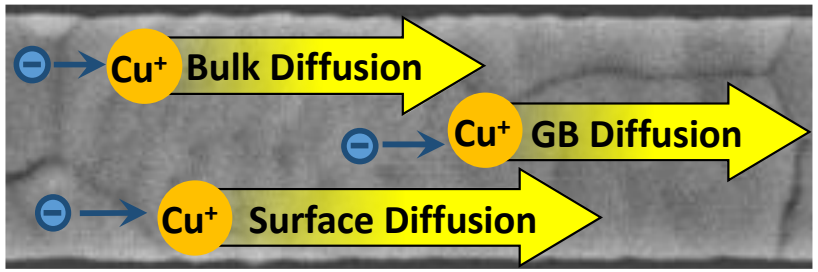
K. Banerjee and A. Mehrotra, ***IEEE Circuits and Devices Magazine***, pp. 16-32, Sept. 2001.

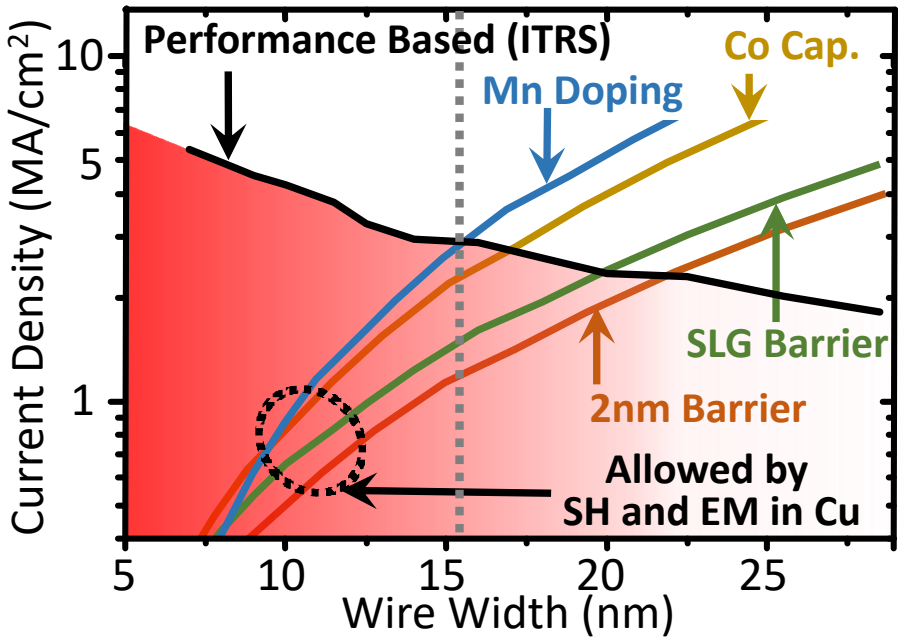
Rapidly Increasing Cu Resistivity



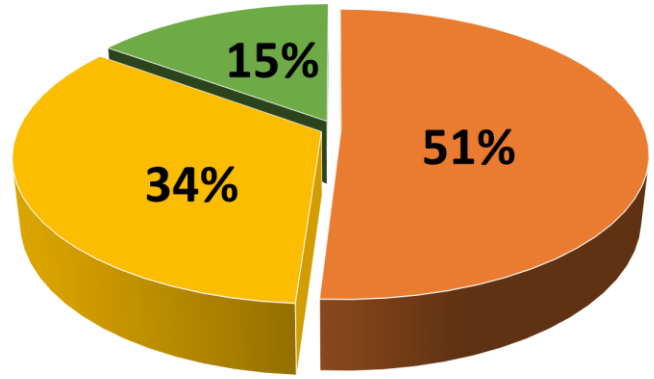
Diminishing Current Carrying Capacity

Cu Migration Under Current Stress





Interconnect Cap. dominates energy consumption



Interconnects

Logic (Gate Capacitance)

Logic (Diffusion Capacitance)

$$Power = CV_{DD}^2 f + I_{leak} V_{DD}$$

dynamic static

Cap. from wires and increased number of buffers

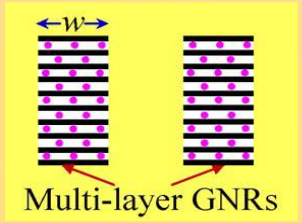
N. Magen et al., (**INTEL**), ***SLIP***, pp. 7-13, 2004.

Intercalated Graphene – Ultra-Energy-Efficient Interconnect Technology

2004 – Discovery of Graphene

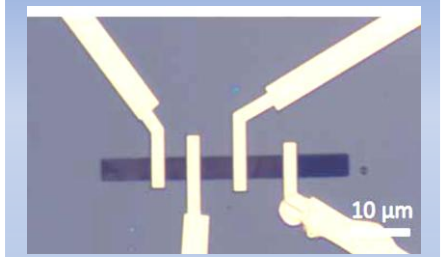
Science 2004

2008 – First Proposal for Intercalated Graphene Interconnects



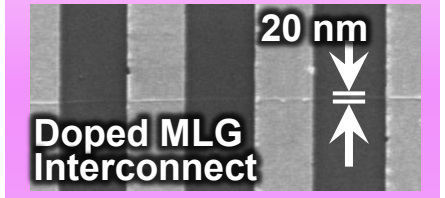
IEDM 2008 (**UCSB**)

2016 – $FeCl_3$ Intercalation of Graphene



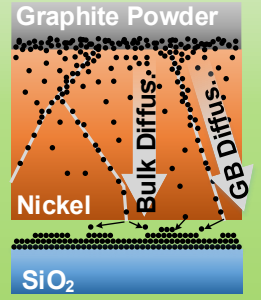
EDL 2016 (**UCSB**)

2017 – 20-nm Intercalation Doped MLG (I-MLG)



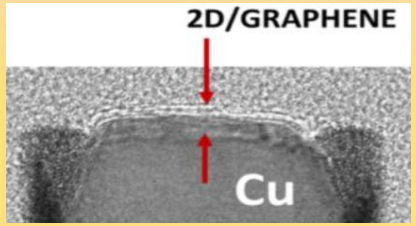
Nano Letters 2017 (**UCSB**)

2018 – CMOS-Compatible I-MLG Synthesis



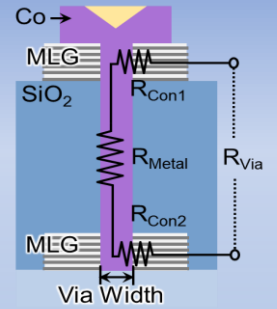
IEDM 2018 (**UCSB**)

2019 – Graphene Capping Layer for Cu



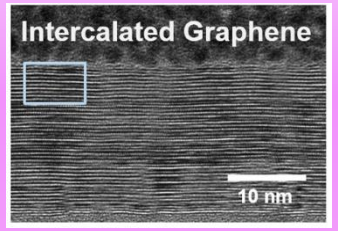
IEDM 2019 (**Intel**)

2020 – CMOS-Compatible Multi-level MLG Interconnects



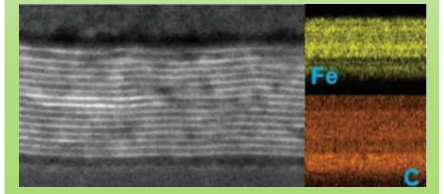
IEDM 2020 (**UCSB**)

2023 – Intercalated Graphene Interconnects



ACS Appl. Nano Mat. 2023 (**TSMC**)

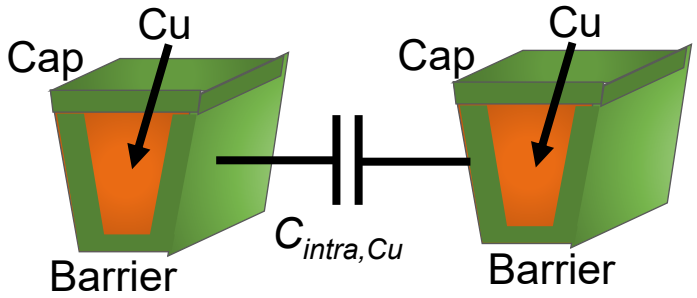
2023 – Intercalated Graphene Interconnects

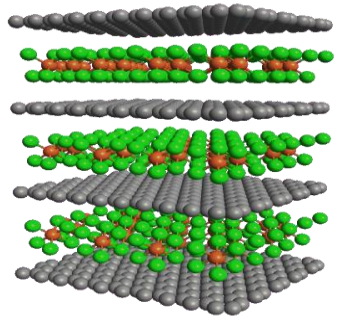


IEDM 2023 (**TSMC**)

Intercalated Multilayer-Graphene (I-MLG) Interconnects

Nano Letters vol. 17, no. 3, 2017.

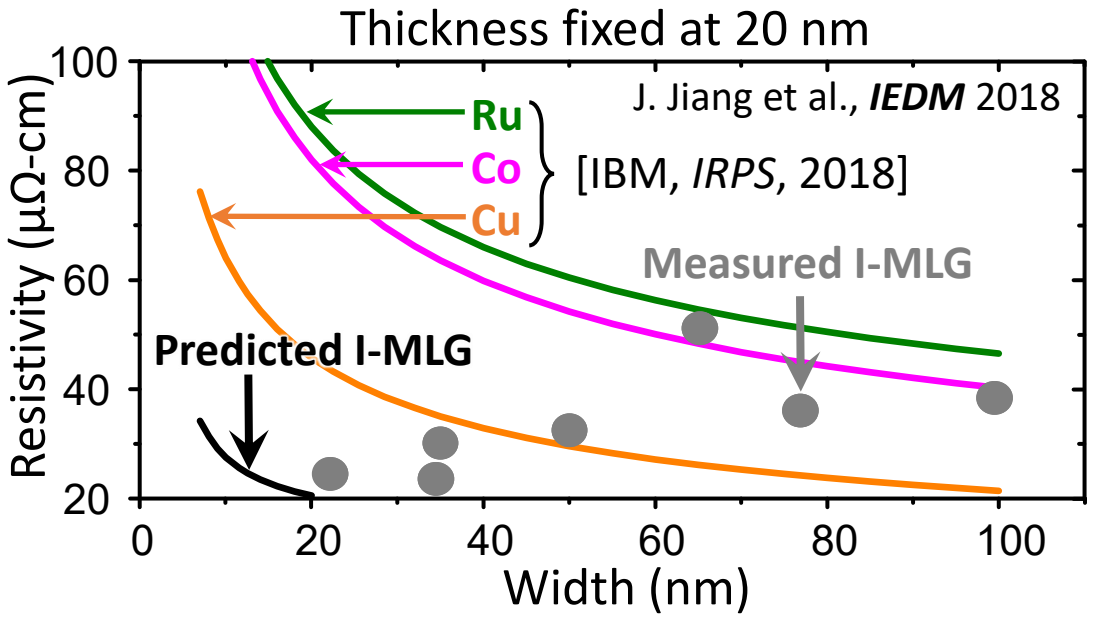




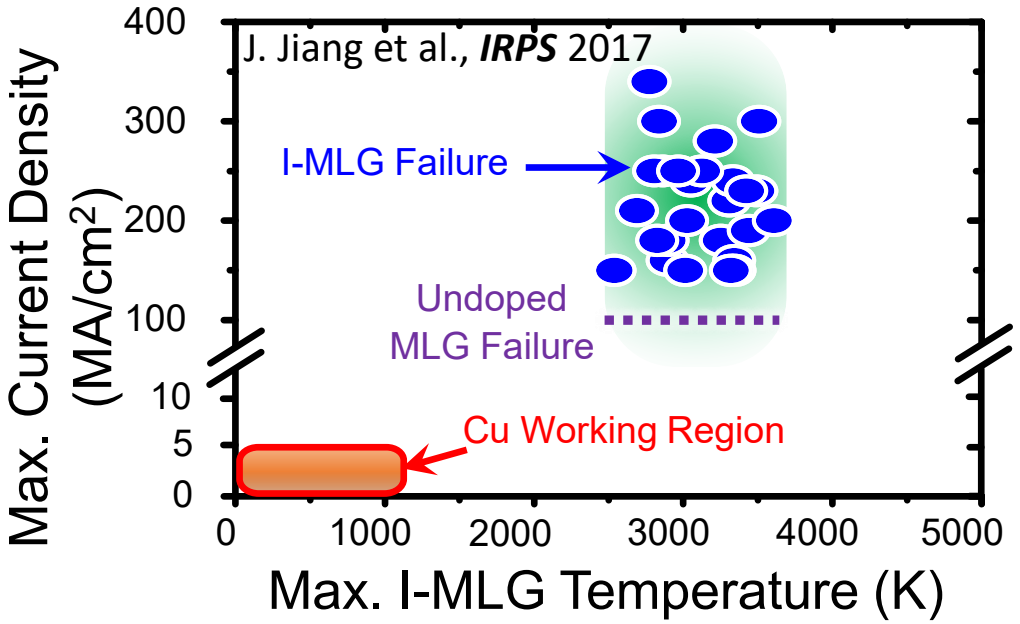
>80% more energy-efficient w.r.t Cu!!!

Intercalation Doped Multi-layer graphene (I-MLG)

Lower resistivity w.r.t. Cu beyond 20 nm width



100X better reliability w.r.t Cu!!!

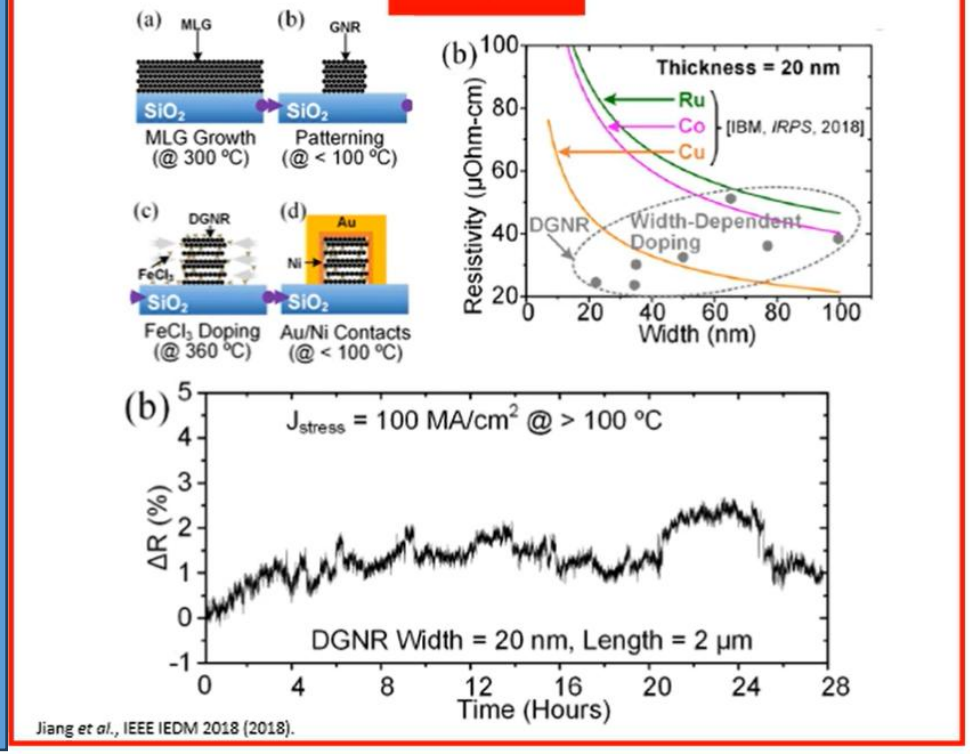


I-MLG Interconnects Independently Validated by TSMC (IEDM 2023) and by Samsung (IEDM 2024)

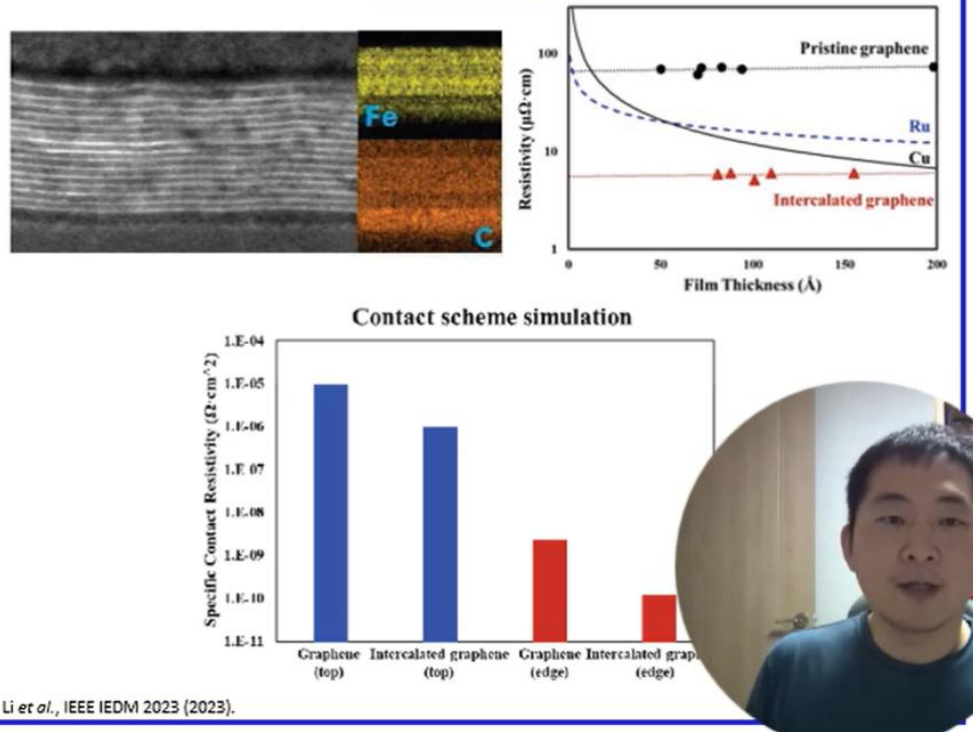
- UCSB demonstrated Ni-assisted graphene growth with EM properties for interconnect.
- TSMC showed the low ρ of ~ 5 μΩ-cm by $FeCl_3$ intercalation.

SAMSUNG IEDM 2024

UCSB



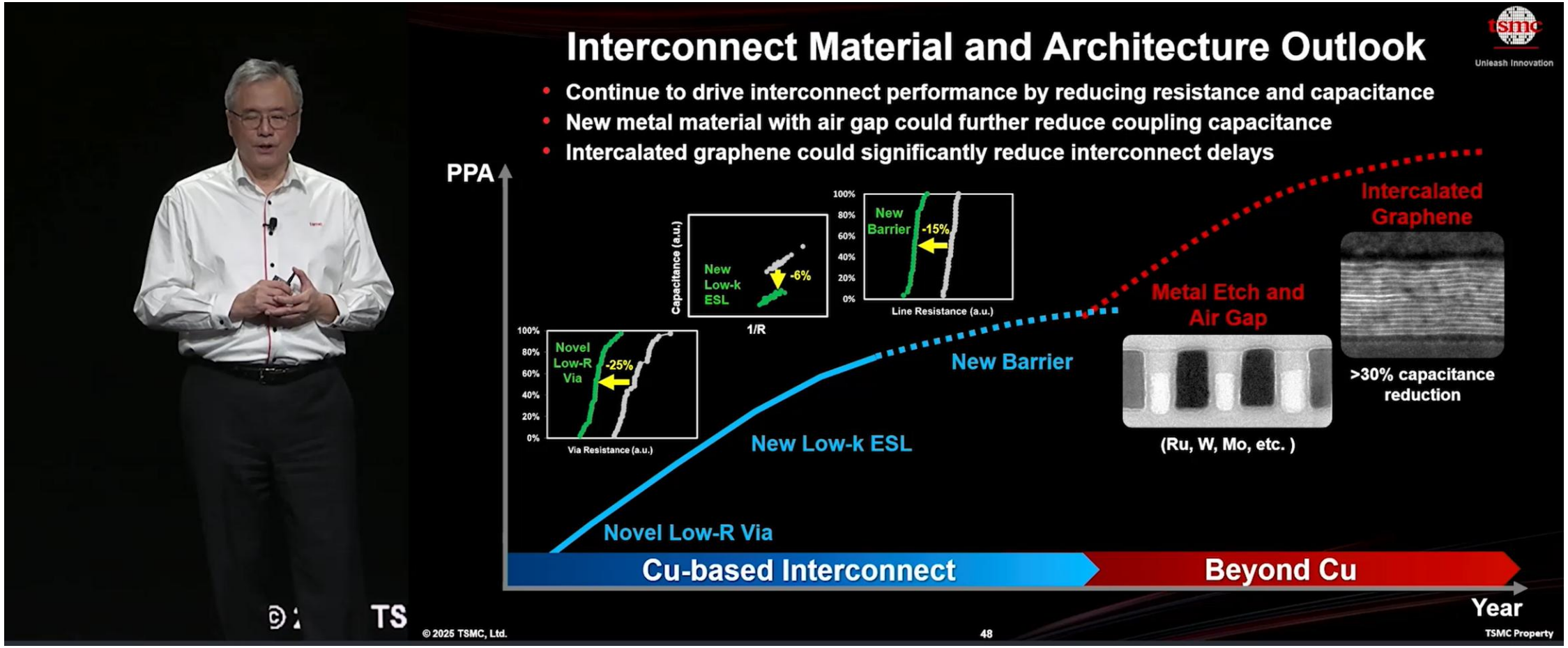
TSMC



Keun Wook Shin et al., (Samsung) IEDM 2024

I-MLG Interconnects Included in TSMC's Interconnect Technology Roadmap in 2025

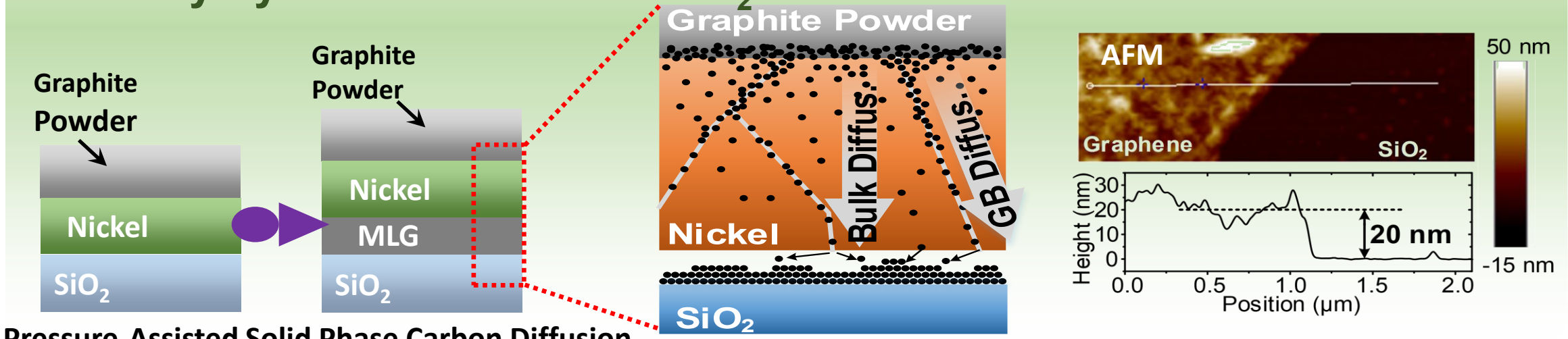
From Concept (IEDM 2008) to World's Largest Foundry Roadmap in ~16 years!!!



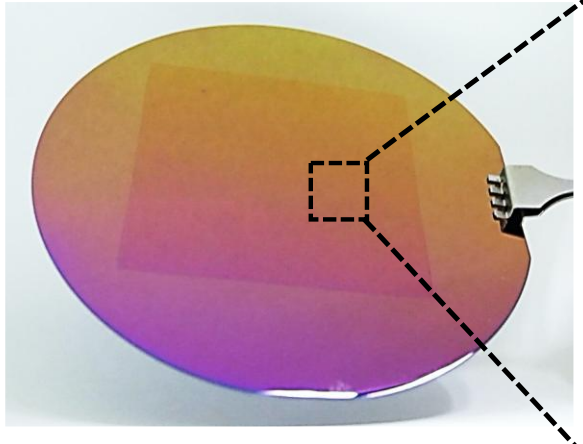
CMOS-Compatible Intercalated-Graphene Interconnects

J. Jiang, et al., ***IEDM*** 2018, pp. 34.5.1-34.5.4.

Directly Synthesized MLG on SiO_2 at 350°C

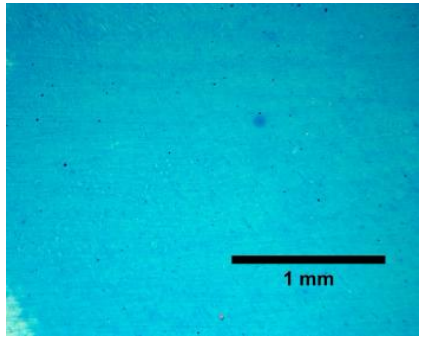


Pressure-Assisted Solid Phase Carbon Diffusion

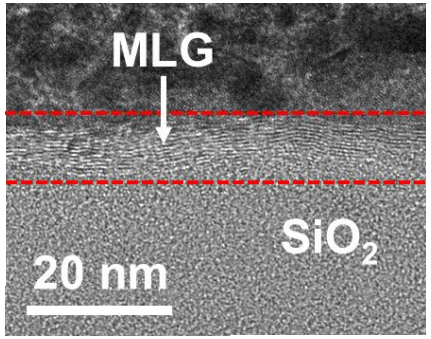


4-inch wafer

Bottom MLG

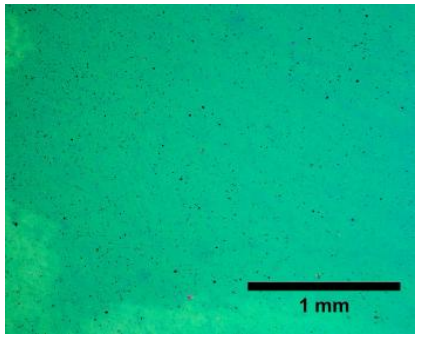


Optical image

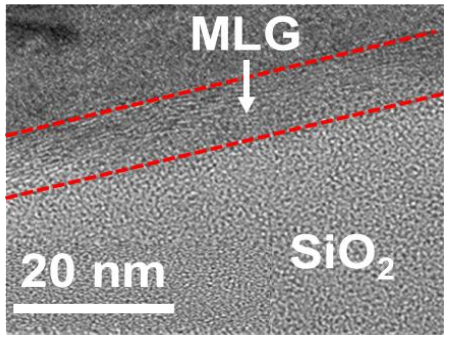


TEM image

Top MLG



Optical image

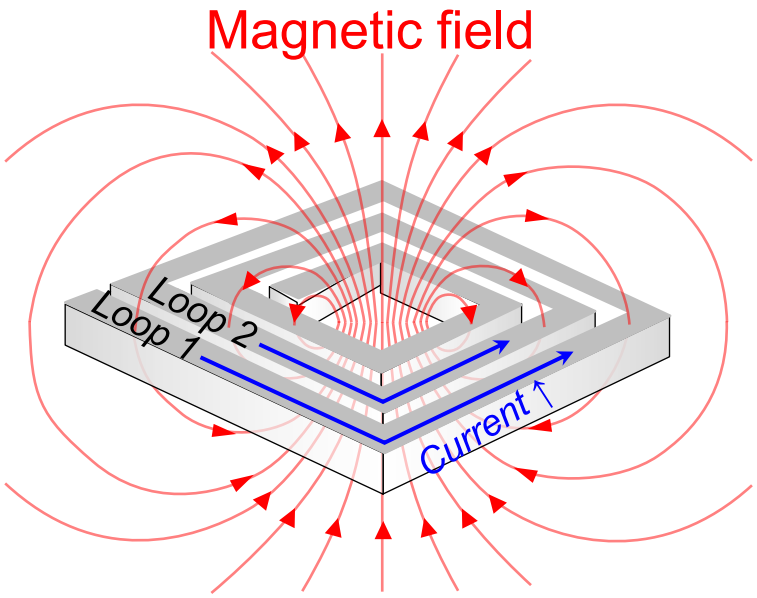


TEM image

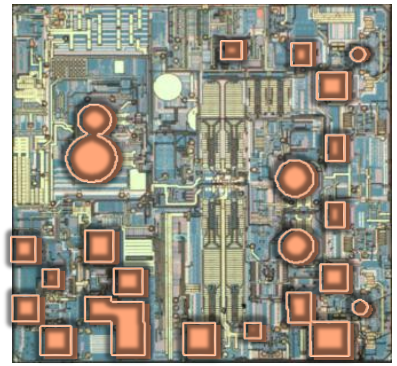
K. Agashiwala ,et al., ***IEDM*** 2020, pp. 31.1.1-31.1.4. / ***IEEE T-ED***, Vol. 68, No. 4, pp. 2083-2091, April 2021.

Inductors (invented in 1831)

- **One of 3 passive circuit elements:** resistor, inductor, capacitor
- Provide **"Inductance" (*L*)**
  current -> magnetic field -> electromotive force (emf)
- Energy storage, oscillation, filtering, tuning, etc

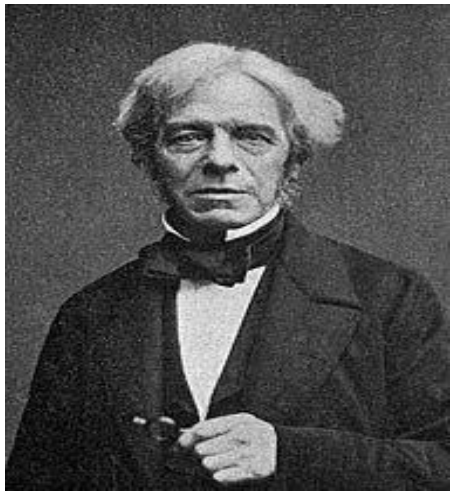


Induced emf: $u(t) = -L_M \, di(t)/dt$

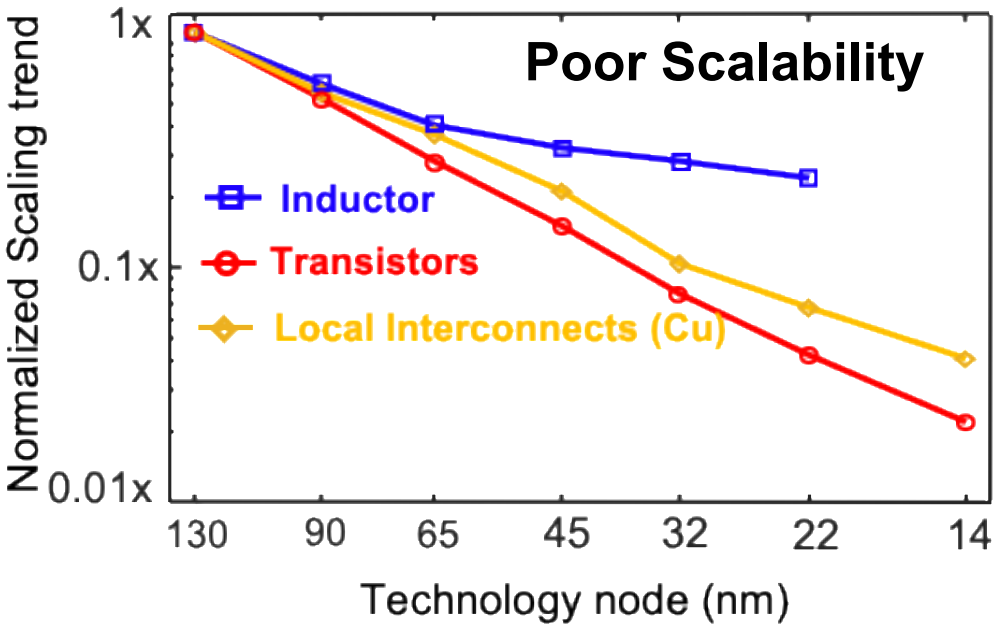


Qualcomm RFIC

up to 50% chip area occupied by inductors

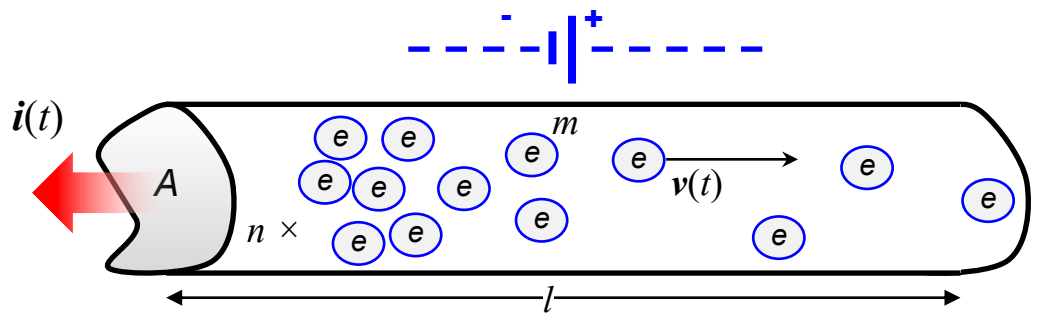


Michael Faraday
(1791 – 1867)



Exploiting Kinetic Inductance

Nature Electronics 1, 46-51, 2018.



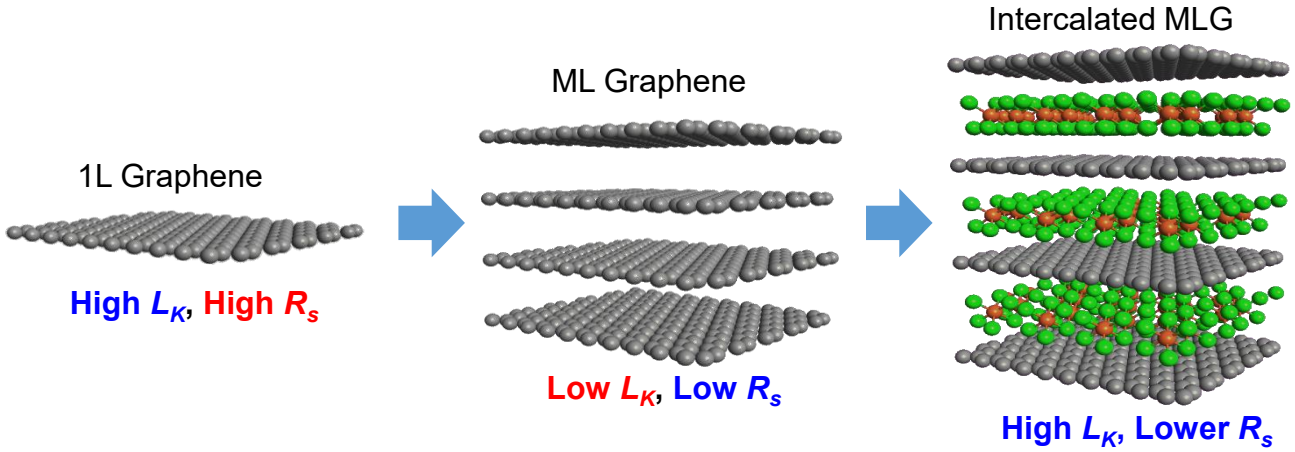
Carrier inertia induced emf:

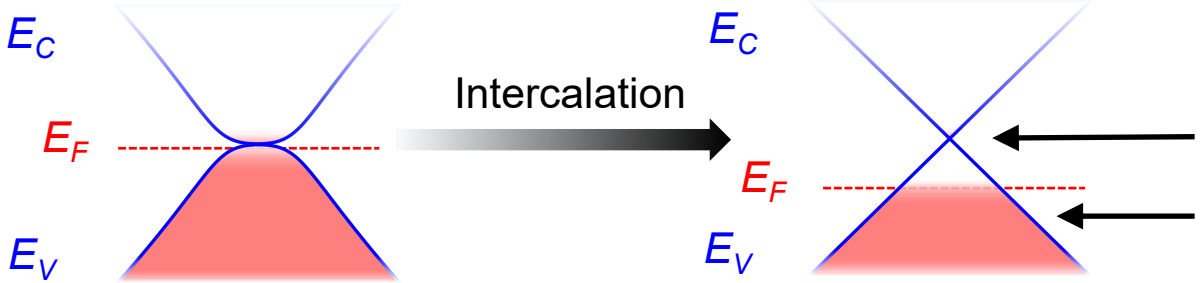
$$u(t) = - L_K \, \mathrm{d}\, i(t) / \mathrm{d}t$$

$$E_K = \tfrac{1}{2} M v^2 \qquad E_K = \tfrac{1}{2} L_K i^2 \qquad \Big\} \; L_K = \tau / \sigma_0$$

Kinetic Inductance of Graphene

	τ (s)	L_K	L_M
Metal	$<10^{-14}$	**pH**	**nH**
CNT/Graphene	$>10^{-12}$	**nH**	**nH**



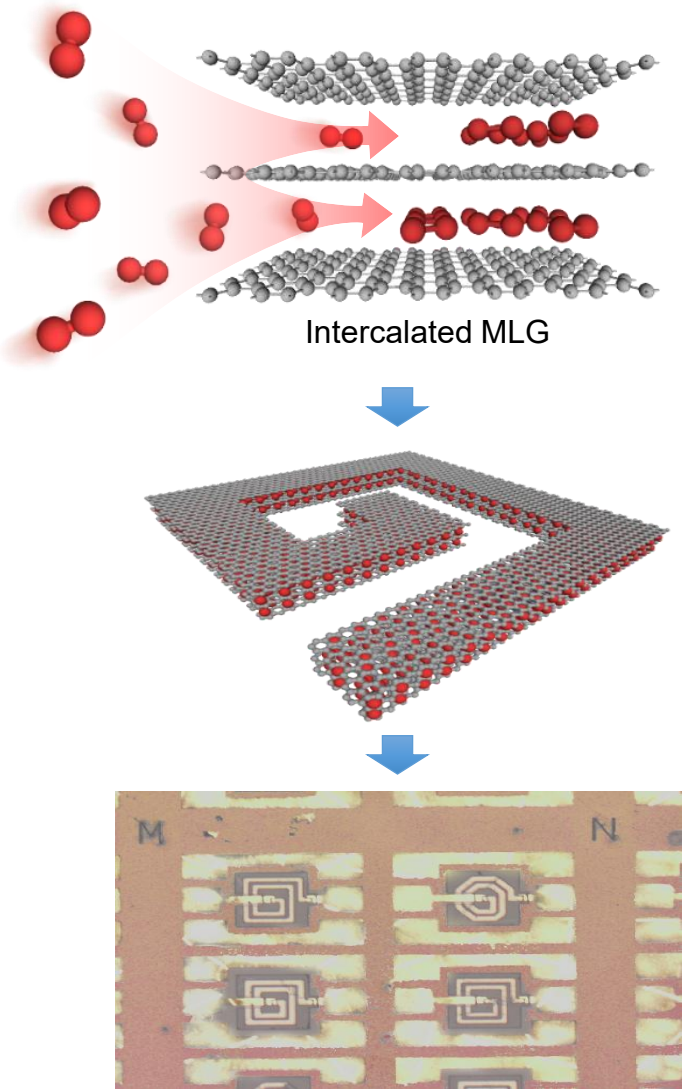


Interlayer Decoupling (Increasing Kinetic Inductance)

Doping (Reducing Resistance)

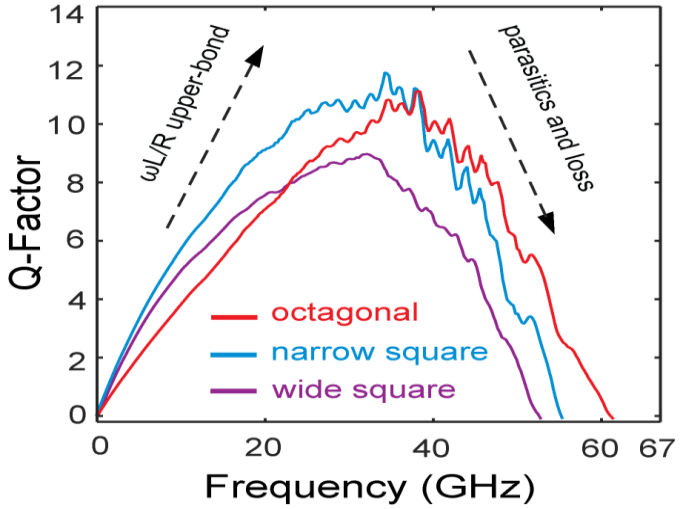
On-Chip Graphene Kinetic Inductors

***Nature Electronics** 1, 46-51, 2018.*

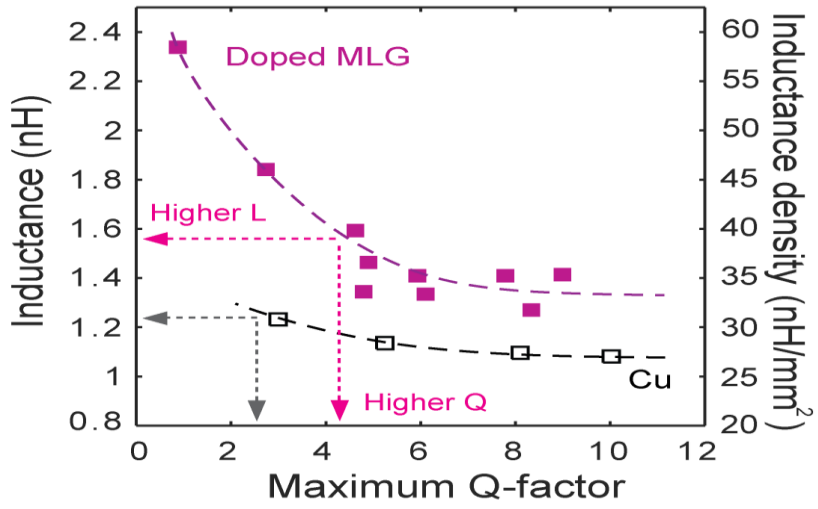


- **Highest inductance-density materials ever made** by intercalation of MLG
- Intercalation leads to higher **kinetic inductance** and **low resistance**
- Both **higher Q-factor** and **higher inductance** density compared to Cu

Sufficient Q-factor up to 12



1.5X inductance density



Inductor design not limited by laws of electromagnetic induction anymore!!!

On-chip graphene inductors overcome a 200-yr old limit

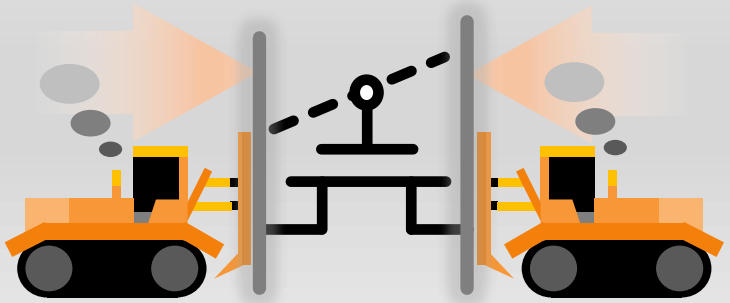
- **exploits kinetic inductance at room temperature**

Intercalation Chemistry *combined with a concept in* ***Condensed Matter Physics*** *to overcome a long-standing* ***Microelectronics Miniaturization*** *challenge!!*

potentially unlocking major advances in wireless, AI, and quantum technologies

3D Integration for the AI-Era

Moore's Scaling Law

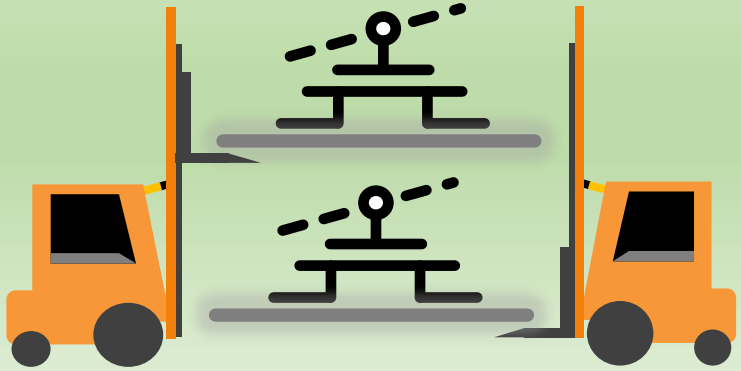


Scaling Challenges:

- Photolithography
- Process
- Reliability
- Variability

Cost of R&D!!!

3D Integration



More Functionality without Scaling + Energy-efficient

- Higher Integration Density
- Smaller Interconnect Delay/ Energy consumption
- Heterogeneous Integration

3-D ICs: A Novel Chip Design for Improving Deep-Submicrometer Interconnect Performance and Systems-on-Chip Integration

K. Banerjee, et al., *Proc. of IEEE*, 2001.

Invited Paper

Performance of deep-submicrometer very large scale integrated (VLSI) circuits is being increasingly dominated by the interconnects due to decreasing wire pitch and increasing die size. Additionally, heterogeneous integration of different technologies in one single chip is becoming increasingly desirable, for which planar (two-dimensional) ICs may not be suitable. This paper analyzes the limitations of the existing interconnect technologies and design methodologies and presents a novel three-dimensional (3-D) chip design strategy that exploits the vertical dimension to alleviate the interconnect related problems and to facilitate heterogeneous integration of technologies to realize a system-on-a-chip (SoC) design. A comprehensive analytical treatment of these 3-D ICs has been presented and it has been shown that by simply dividing a planar chip into separate blocks, each occupying a separate physical level interconnected by short and vertical interlayer interconnects (VILICs), significant improvement in performance and reduction in wire-limited chip area can be achieved, without the aid of any other circuit or design innovations. A scheme to optimize the interconnect distribution among different interconnect tiers is presented and the effect of transferring the repeaters to upper Si layers has been quantified in this analysis for a two-layer 3-D chip. Furthermore, one of the major concerns in 3-D ICs arising due to power dissipation problems has been analyzed and an analytical model has been presented to estimate the temperatures of the different active layers. It is demonstrated that advancement in heat sinking technology will be necessary in order to extract maximum performance from these chips. Implications of 3-D device architecture on several design issues have also been discussed with especial attention to SoC design strategies. Finally, some of the promising technologies for manufacturing 3-D ICs have been outlined.

***Keywords*—3-D ICs, heterogeneous integration, interconnect performance, optical I/Os, power dissipation, system interconnects, system-on-a-chip design, VLSI design.**

Manuscript received August 30, 2000; revised February 28, 2001. This work was supported by the Defense Advanced Research Projects Agency AME Program and the MARCO Interconnect Technology Focus Center.

The authors are with the Center for Integrated Systems, Stanford University, Stanford, CA 94305 USA (e-mail: kaustav@ee.stanford.edu).

Publisher Item Identifier S 0018-9219(01)04184-6.

I. Motivation for 3-D ICs

The unprecedented growth of the computer and the information technology industry is demanding very large scale integrated (VLSI) circuits with increasing functionality and performance at minimum cost and power dissipation. VLSI circuits are being aggressively scaled to meet this demand. This, in turn, has introduced some very serious problems for the semiconductor industry. Continuous scaling of VLSI circuits is reducing gate delays but rapidly increasing interconnect delays. The International Technology Roadmap for Semiconductors (ITRS) [1] predicts that, beyond the 130-nm technology node, performance improvement of advanced VLSI is likely to begin to saturate unless a paradigm shift from present IC architecture is introduced. Also, increasing interconnect loading affects the power consumption in high-performance chips. In fact, a significant fraction of the total chip power consumption can be due to the wiring network used for clock distribution, which is usually realized using long global wires. Additionally, interconnect scaling has significant implications for traditional computer-aided-design (CAD) methodologies and tools which are causing the design cycles to increase, thus increasing the time-to-market and the cost per chip function. Furthermore, increasing drive for the integration of disparate signals (digital, analog, RF) and technologies (SOI, SiGe HBTs, GaAs, and so on) is introducing various system-on-a-chip (SoC) design concepts, for which existing planar (two-dimensional) IC design may not be suitable.

A. Interconnect Limited VLSI Performance

In single Si layer (2-D) ICs, chip size is continually increasing despite reductions in feature size made possible by advances in IC technology such as lithography and etching

"Established the blueprint for modern chiplets and advanced packaging"

Heterogenous Monolithic-3D Integration with 2D vdW Materials

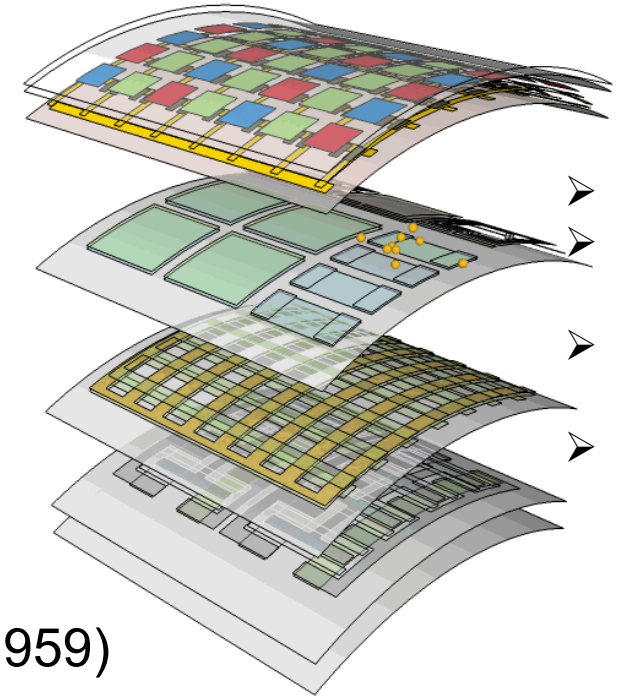
J. Jiang et al., ***IEEE J-EDS,*** vol. 7, 2019.

– the holy grail

"What could we do with layered structures with just the right layers?"

Richard Feynman, "There's plenty of room at the bottom" (1959)

Heterogenous 3D-integration of 2D-materials for ultra-energy-efficient electronics



- **Low-T deposition of 2D**
- **Thinner body - lower thermal resistance**
- **Improved lateral heat dissipation**
- **Higher integration density**

Integrating 2D in mainstream electronics...from lab to fab

IEEE Spectrum - "Graphene Interconnects Aim to Give Moore's Law New Life"

nature electronics

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Research Highlight | Published: 30 November 2018

INTERCONNECTS

CMOS-compatible graphene

Stuart Thomas

Nature Electronics **1**, 612 (2018) | Cite this article

4184 Accesses | **9** Citations | **31** Altmetric | Metrics

2018 IEEE Int. Electron Devices Meet. (in the press); https://ieee-iedm.org/program/

Semiconductor industry's very first,

Transfer-free, Low temperature,

Graphene interconnect technology

& 300 mm scale equipment

Destination 2D

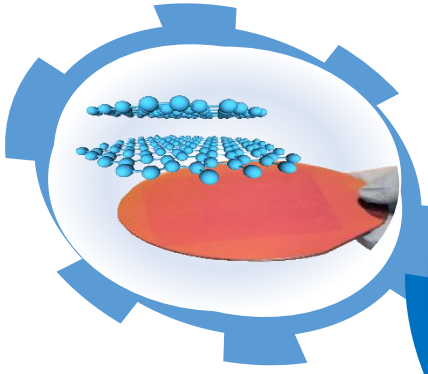
FUELING FUTURE ELECTRONICS

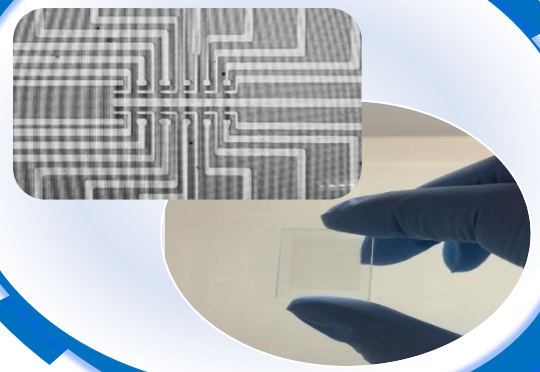
https://destination2d.com/

The future of sustainable electronics is 2D!!!

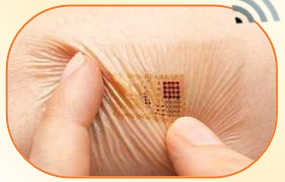
2D vdW Materials

Uniquely Enabled Electronics – Transistors, Sensors, Memories, Interconnects, Inductors, Monolithic-3D ICs…





Toward a smarter & sustainable life…



UCSB Nano Research Lab

-Korea Forum on Nanotechnology, Sept. 14, 2026