Fabrication and Characterization of bulk FinFETs for Future Nano-Scale CMOS Technology

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Fabrication of Bulk FinFETs

- by Spacer Technology
- by Selective Si$_3$N$_4$ Recess

Device and SRAM Cell Characteristics

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Introduction: Technology Roadmap Beyond Bulk LDD CMOS
Introduction

◆ Driving Force of CMOS Scaling-down:
  → High Performance and High Integration Density

◆ A Promising Device Structure
  → Double/Triple-Gate MOSFETs (or FinFETs)

◆ Why Double/Triple-Gate Transistor?
  → Robustness against SCE
  → Higher Current Drivability
  → Good Subthreshold Swing
**Introduction**: Types of Double-Gate Transistors

(a) Type I

(b) Type II

(c) Type III

Process technology of FinFET is easy and compatible with conventional fabrication process

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* H. P. Wong et al., IBM, vol. 87, no. 4, p.537, 1999, Proceedings of the IEEE

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## Types of Double/Triple-Gate Transistors

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Double-Gate Transistor (SOI FinFET)

◆ FinFET
  ◆ simple, self-aligned double-gates
  ◆ good process compatibility
  ◆ thickness control of fin body
  ◆ RIE damage on the channel, high S/D resistance

* D. Hisamoto et al., UC Berkeley, p.1032, IEDM 1998
Body-Tied Double/Triple-Gate MOSFET Using Bulk Wafer (Bulk FinFET)

- Low wafer cost
- Low defect density
- Less back-bias effect
- High heat transfer rate to substrate
- Good process compatibility

Schematic 3-D View

World 1st Cost-Effective Double/Triple-Gate MOSFETs

* J.-H. Lee., Korea/Japan/USA patent

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Cross-Sectional Views (Body Structure) for 3-Dimensional Device Simulation

SOI FinFET

Bulk FinFET

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**3-D Simulation Results**

\[ V_T = \Phi_{MS} + 2\phi_B + \frac{qN_{sub}t_b}{2C_{ox}} \]

for fully depleted body

\[ V_T \] and DIBL versus Fin Width

Subthreshold Swing versus Fin Width

* J.-H. Lee et al., KNU, p. 102, Si Nanoelectronics Workshop 2003

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3-D Simulation Results

3-D Schematic View of Heat Transfer from Body to Substrate

Device Temperature versus Gate Voltage

Device Temperature versus Gate Voltage

300 325 350 375 400 425 450 475

Gate Voltage (V)

0.0 0.2 0.4 0.6 0.8 1.0

L_G=30 nm
T_{ox}=1.5 nm
V_{DS}=0.9 V

substrate electrode @ temperature=300 K

ΔT~130 °C

* J.-H. Lee et al., KNU, p. 102, Si Nanoelectronics Workshop 2003

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Fabrication Steps by Using Spacer Technology

4 Stack Layer Growth and Deposition

SiN 80 nm
SiO₂ 30 nm
SiN 25 nm
SiO₂ 30 nm
Si

Poly-Si Spacer 30 nm

SiN Removal Using Phosphoric Acid

Photo Lithography, SiN Etching, Poly-Si Depo., and Dry Etching
**Fabrication Steps**

SiO₂, SiN, and SiO₂ Dry Etching

Fin Dry Etching

Top Si Width 25 nm
Bottom Si Width 100 nm
Si Fin Height 230 nm

Fin body

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Fabrication Steps

Thin Ox., Filling, and Densification

SiO$_2$

Chemical Mechanical Polishing (CMP)

Wet Etch-back

Field Oxide Thickness 80 nm
First Body-Tied Triple-Gate MOFET (Bulk FinFET)

As\(^+\), 20 keV 3x10\(^{15}\)/cm\(^2\), 2 Fin

I\(_\text{D}-V_{\text{GS}}\) Characteristics of 40 nm bulk NFiNFET

* T. Park et al., SNU/KNU, Nanomes03 2003
* T. Park et al., SNU/KNU, Physica E19, p.6, 2003

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Modified Structure of Bulk FinFET

- Clear Sidewall Open
- Planarization of the Top Surface of Poly-Si Gate
  - Easy nano-scale patterning of gate poly-Si

* E. Yoon, J.-H. Lee, and T. Park, Korea/Japan/USA/Germany patent

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Key Process Steps of Modified Bulk FinFET

1. Active Photo
2. T/E, Ashing, s/o
3. Filling, CMP
4. SiN Strip, IIP
5. SiN Add. Etch
7. Poly-Si
SEM Views of Key Process Steps

SiN Liner Deposition

SiN Recess Etch
SEM Views of Key Process Steps

Gate Etch Profiles

Along Gate Line

Across Gate Line

* T. Park et al., Samsung/SNU/KNU, Symp. on VLSI Tech., 2003
SEM and TEM Views of Key Process Steps

Along Gate Line

12 nm fin body

* T. Park et al., Samsung/SNU/KNU, IEDM., 2003

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**Bulk FinFET Measurement**

$I_D$-$V_{GS}$ plot: $I_D$, DIBL, SS, and $I_{sub}$

- $V_{DS}=-0.05$ V
- $V_{DS}=0.05$ V
- $V_{DS}=1$ V
- $V_{DS}=-1$ V
- $V_{DS}=1.0$ V
- $V_{DS}=1.5$ V
- $V_{BS}=0$ V
- $L_G=100$ nm
- $H_{Fin}=100$ nm
- $W_{Fin}=25$ nm
- $T_{Ox,top}=5.5$ nm
- $T_{Ox,top}=1.8$ nm

- Measured $I_D$-$V_{GS}$ of N and P type bulk FinFETs with drain bias
  - high $I_{on}$ (~200 $\mu$A/µm @ $V_{GS}=1.5$ V) compared to that of first lot devices
  - low $I_{off}$ (<0.2 nA/µm @ $V_{DS}=1.0$ V)
  - $I_{sub}/I_D < \sim 10^{-7}$
Static Noise Margin (SNM)

Bulk FinFET

Planar MOSFET

W/L
Load: 35 nm/90 nm
Pass: 35 nm/90 nm
Pull-Down: 50 nm/90 nm

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Summary

- Briefly introduced key features of double/triple-gate FinFETs
- Bulk FinFETs were compared with SOI FinFETs
  - Nearly the same device scalability
  - Better wafer quality
  - Better characteristics regarding the body connected to sub.
- Bulk FinFETs have been demonstrated experimentally
  - First nano-scale bulk FinFET realized by using spacer technology
  - Modified bulk FinFETs realized by adopting selective Si$_3$N$_4$ recess
- Good device characteristics were achieved and SNM of 280 mV was obtained from SRAM cell at $V_{CC}$ of 1.2 V
3-D Device Structure for Simulation

L_G=25 nm  \quad T_{OX}=1.5 \text{ nm}
Key Process Steps for Thinning of the Fin Body

Active Photo, SiN Etch

Sidewall Oxidation

PR

ARL

SiN

Trench Etch

SiN, SiO₂ Strip