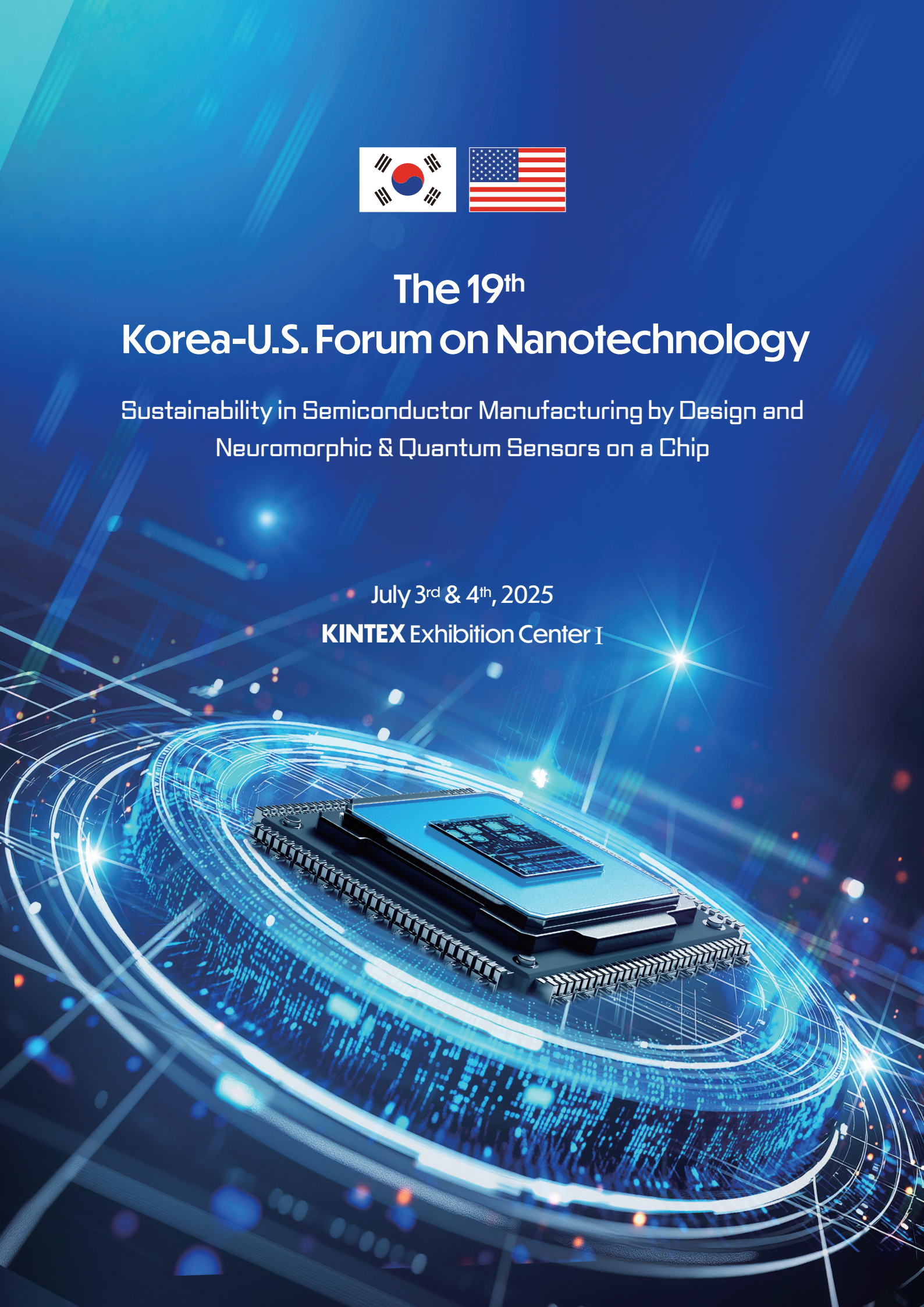
The 19th Korea-U.S. Forum on Nanotechnology

Sustainability in Semiconductor Manufacturing by Design and Neuromorphic & Quantum Sensors on a Chip

July 3rd & 4th, 2025

KINTEX Exhibition Center I



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The 19th U.S.-Korea Forum on Nanotechnology:

Sustainability in Semiconductor Manufacturing by Design and Neuromorphic & Quantum Sensors on a Chip

The Forum will take place on Thursday and Friday, July 3rd & 4th, 2025.

| Program & Presentations

On the first day, the keynote speakers and session participants will give oral presentations (25 minutes and 15 minutes), and the young scientists will participate in a poster session, which will include a 5-minute presentation. All presenters should participate in the group discussion workshop on the second day.

| Meeting Location

Special session of NanoKorea 2025, Kintex, Gyeonggi-do, Korea
(https://nanokorea.or.kr/eng/introduce/summary.php)

| Dates & Time

July 3rd & 4th, 2025 @8:30 a.m.
Lunch (July 3rd) will be provided for all participants.
Dinner (July 3rd) and lunch (July 4th) will be provided for invited participants.

| Conference Hotel

THE PLAZA Seoul, Autograph Collection, 119, Sogong-ro, Jung-gu, Seoul
We will arrange transportation between the hotel and Kintex.

The 19th U.S.-Korea Forum on Nanotechnology:

Sustainability in Semiconductor Manufacturing by Design and Neuromorphic & Quantum Sensors on a Chip

| Supporting Organizations

- National Science Foundation (USA)
- Ministry of Science and ICT (Korea)
- National Nanotechnology Policy Center (Korea)
- Korea-U.S. Science Cooperation Center (USA)

| Organizers

- Korea Nanotechnology Research Society (Korea)
- Carnegie Mellon University (USA)
- Northeastern University (USA)
- University of Pittsburgh (USA)

USA	Korea
Myung S. Jhon (Chair) Ahmed Busnaina Elias Towe In Hee Lee	Jinho Ahn (Chair) Jo-won Lee Sang Joon Cho Tae Gon Kim Seyoung Kim

Chair

Jinho Ahn

President | Korea Nanotechnology Research Society, Korea
Executive Vice President of Research, Hanyang University, Korea

| Biography

Jinho Ahn received his B.S. and M.S. degrees from Seoul National University, and Ph.D. degree from the University of Texas at Austin all in Materials Science and Engineering. He worked for Microelectronics Research Laboratory at NEC, Tsukuba, Japan, and joined Hanyang University in 1995 as a professor of Materials Science and Engineering. He worked as a Director of Nano and Convergence Technology at National Research Foundation of Korea, and the Vice President of Academic Research, the President of Industry University Cooperation Foundation at Hanyang University. He is now the President of Korea Nanotechnology Research Society, and Executive Vice President for Research of Hanyang University. He received the Semiconductor Technology Lifetime Achievement Award in 2015 from the President of Korea.

Chair

Myung S. Jhon

Professor | Carnegie Mellon University

| Biography

Professor Jhon is a Professor Emeritus of Chemical Engineering and a member of the Data Storage Systems Center (DSSC) and the Institute for Complex Engineered Systems (ICES) at Carnegie Mellon University in Pittsburgh, PA. Professor Jhon received his B.S. in Physics from Seoul National University, Korea, and his Ph.D. in Physics from the University of Chicago. He has served as visiting professor in several institutions, including the U.S. Department of Energy (National Energy Technology Laboratory and Sandia National Laboratories); the Department of Chemical Engineering, University of California, Berkeley; IBM Almaden Research Center, San Jose; and the Naval Research Laboratory, Washington, D.C. He served as a consultant to the United Nations Industrial Development Organization, and also served as a Corporate Science and Technology Advisor for Mitsubishi Chemical Corporation (Japan) for several years. He served as the President & CEO of Doosan DND Co., Ltd (Korea) and also served as a World Class University Professor at Sungkyunkwan University in Korea and as a Distinguished Advisor for Exa Corporation.

Professor Jhon is internationally known for his work in the fields of information storage systems, computational science, nanotechnology, engineering policy, semiconductors, graphene, organic light-emitting devices (OLED), and chemical mechanical polishing (CMP). He is a Fellow of the Korean Academy of Science and Technology. He served as an advisory committee member for a Korean national program for Tera-level nanodevices and is serving as the chair of the advisory board and a lead organizer for the U.S.-Korea Nanotechnology Forums (https://www.cmu.edu/nanotechnology-forum/). He has contributed publications in the areas of information storage systems, nanotechnology, computational methods (lattice-Boltzmann method, finite-element method, smoothed particle hydrodynamics, atomistic, Monte Carlo, molecular dynamics & multiscale simulation, and parallel computing), fuel cell, equilibrium and non-equilibrium statistical mechanics, nucleation, fluid and solid mechanics, interfacial dynamics, polymer engineering, rheology, multiphase flow, tribology, chemical kinetics, and OLED & CMP equipment. He is also dedicated to the educational process, as is evident from his numerous teaching awards and his role as an ABET evaluator (Akron, Worcester Polytechnic Institute, Rochester, Tufts, Stanford, Connecticut, Tennessee Tech, Stevens Institute of Technology, Maryland, and Florida), and was the Carnegie Institute of Technology Faculty Chair & Undergraduate Chair in his department.

Chair

Myung S. Jhon

Professor | Carnegie Mellon University

| Biography

Currently, he is completing an undergraduate textbook entitled Principles of Fluid Mechanics, part of which is published on the Carnegie Mellon website. He has won a number of teaching and research recognition awards, including the Ladd, Teare, Ryan, Dowd, and Li Awards.

The 19th U.S.-Korea Forum on Nanotechnology:

Sustainability in Semiconductor Manufacturing by Design and Neuromorphic & Quantum Sensors on a Chip

The purpose of the Forum on Nanotechnology is to provide a common platform for researchers from the U.S. and Korea to engage in discussions on emerging technologies that contribute to the development of state-of-the-art nanotechnology. This year's Forum will provide opportunities for discussion on neuromorphic & quantum sensors on a chip and sustainability in semiconductor manufacturing by design where nanotechnology convergence provides critical solutions to our most pressing technological challenges.

These Forums continue to thrive on the recommendation of the Korea-U.S. Joint Committee on Scientific and Technological Cooperation. The first Forum was initiated two decades ago, and since then, the locations of the Forum have alternated between Korea and the United States. Because of the wide array of technical challenges to which nanotechnology can be successfully applied, each previous Forum had a different emerging technology focus. This 19th Forum will include five keynote speakers, 18 senior presenters, 16 early-career presenters from the U.S. and Korea. This year, the 19th U.S.-Korea nanotechnology Forum is a special session of the NanoKorea 2025 Conference (https://nanokorea.or.kr/eng/introduce/summary.php) to attract a broader audience and maximize impact.

The outcomes of this Forum will lead to milestones and vigorous research collaboration for both countries where sustainability in semiconductor manufacturing and sensor technology will generate great economic and social impact. We hope the discussion during this Forum will enable the U.S. to pivot towards transformative approaches for novel semiconductor design and fabrication as well as advanced sensor technology.

We are looking forward to seeing you in Korea during the July 4th weekend!

Sincerely,

The Organizing Committee

Day 1 | July 3, 2025 (Thursday)

Room 210, KINTEX Exhibition Center I

08:30~09:00		**Registration**
Opening Session Co-chairs Jo-won Lee Myung S. Jhon	09:00~09:03 3 min/talk	**Opening Remarks**
		• Jinho Ahn, *Korea Nanotechnology Research Society*
	09:03~09:15 5 min/talk	**Welcoming Remarks**
		• Taek-ryeol Jeong, *Ministry of Science and ICT* • Seongsin Margaret Kim, *National Science Foundation*
	09:15~10:10 25 min/talk 2 min/Q&A	**Keynote Speeches**
		• John Rogers, *Northwestern University* Semiconductor Nanomaterials in 3D and Transient Electronics • Seongsin Margaret Kim, *National Science Foundation* Research Progress and Perspective of Quantum Networking and Sensing
	10:10~10:35	Coffee Break & Group Photo
	10:35~12:00 25 min/talk 2 min/Q&A	**Keynote Speeches**
		• Heung Soo Park, *National Nanofab Center* The Role of National NanoFab Center for Advancing Nanotechnology Research, Education, and Commercialization in Korea • Kwabena Boahen, *Stanford University* Scaling Knowledge Processing from 2D Chips to 3D Brains • Victor Zhirnov, *Semiconductor Research Corporation* New Chips R&D Initiative – Semiconductor Manufacturing and Advanced Research with Twins
12:00~13:00		Lunch & Poster Set-Up
Session I Sustainability in Semiconductor Manufacturing by Design Co-chairs Tae Gon Kim Ahmed Busnaina	13:00~15:35 15 min/talk 2 min/Q&A	• Ahmed Busnaina, *Northeastern University* Sustainable Additive Manufacturing of Electronics and 3D Heterogenous Integration for Advanced Packaging
		• Hak-Sung Kim, *Hanyang University* Milli-seconds Multi Flip-chip Bonding Process via Intense Pulsed Light Irradiation for Sustainability of Semiconductor Packaging Manufacturing
		• Paul Westerhoff, *Arizona State University* Barriers Associated with Trace Organics and Discoveries on How to Reuse Semiconductor Fab Wastewater for Ultrapure Make-up Water
		• Jin-Seong Park, *Hanyang University* Designing Sustainable Area-Selective ALD: A Data-Driven Framework for Inhibitor Engineering
		• Fazleena Badurdeen, *University of Kentucky* Closing the Loop: Advancing Circularity in Semiconductor Chips and Chip-integrated Components
		• Jungwan Cho, *Sungkyunkwan University* Electro-Thermal Co-Design of High-Power Semiconductor Devices

Day 1 | July 3, 2025 (Thursday)

Room 210, KINTEX Exhibition Center I

		• Sung Kyu Lim, *Georgia Institute of Technology* AI-Driven Co-Optimization of Design and Manufacturing for Heterogeneous AI Chips
		• Jiyoung Kim, *The University of Texas at Dallas* Machine Learning for Accelerating Atomic Layer Deposition Process Optimization
		• Pascal Oberndorff, *NXP Semiconductors* Electronic Packaging Enabling the Future of Semiconductors
15:35~15:55		Coffee Break
Session II Neuromorphic & Quantum Sensors on a Chip Co-chairs Seyoung Kim Elias Towe	15:55~18:30 15 min/talk 2 min/Q&A	• Elias Towe, *Carnegie Mellon University* Solid-state Quantum Magnetometers
		• Gyoujin Cho, *Sungkyunkwan University* Perspective: Way of Sustainable Manufacturing for Disposable Quantum Spin Biosensors and Sticker-Like 2-Qubit Quantum Computers
		• Darmindra Arumugam, *Jet Propulsion Laboratory / California Institute of Technology* Remote Sensing with Rydberg Atoms
		• Douglas Weber, *Carnegie Mellon University* Sensing and Stimulating the Brain to Restore Neurological Function
		• Yang-Kyu Choi, *Korea Advanced Institute of Science and Technology* Rethinking Transistor Operation for Oscillating and Spiking Behavior
		• Euisik Yoon, *University of Michigan* Brain Interface: Electrophysiology and Optimal Neuromodulation at Cellular Resolution
		• Dmitri Strukov, *University of California, Santa Barbara* KLIMA: K-Local In-Memory Accelerator for Combinatorial Optimization
		• Seong Jun Kang, *Kyung Hee University* Band Structure of Oxide Semiconductors for Optical Neuromorphic Devices to Realize Highly Efficient and Accurate Machine Vision
		• Bruce Gnade, *The University of Texas at Dallas* Neuromorphic Sensors for Anomaly Detection
18:30~20:00		**Banquet**

Day 2 | July 4, 2025 (Friday)

Room 210 & 211A, KINTEX Exhibition Center I

Poster Session Co-chairs Jo-won Lee Myung S. Jhon	08:30~09:50 5 min/talk, including Q&A	• Hongseok Oh, *Soongsil University* Te Photonic Synapses for Physical Reservoir Computing
		• Mikael P. Backlund, *University of Illinois at Urbana-Champaign* Quantum and Quantum-Inspired Microscopy of Molecules and Materials
		• Guesuk Lee, *Korea Electronics Technology Institute* Thermoreflectance-Based Submicron Temperature Profiling and Structure Function Analysis for Multilayer Nanostructures
		• Robert Nawrocki, *Purdue University* Organic Spiking Neuromorphic Circuits: Flexible Embodied AI
		• Hyunjeong Kwak, *Pohang University of Science and Technology* Monolithic 4K Electrochemical RAM-Based Analog AI Chip for Energy-Efficient On-Chip Training
		• Youjin Reo, *Pohang University of Science and Technology* Vapour-Deposited High-performance Tin Halide Perovskite Transistors
		• Matthew T. Flavin, *Georgia Institute of Technology* Wearable Mechatronics for Receiving and Transmitting Information Through the Skin
		• Jaeduk Han, *Hanyang University* Design and Generation of High-Performance Transceivers
		• Jung-Hoon Lee, *Korea Research Institute of Chemical Technology* Synthesis of a Tin Compound Bearing N-alkoxy Carboxamide and Methyl Ligands as a Precursor for SnO2 Fabrication via Atomic Layer Deposition
		• Inhee Lee, *University of Pittsburgh* Millimeter-Scale Neuromorphic Vision System
		• Sung Beom Cho, *Ajou University* Multiscale Simulation and AI-Driven Approaches for Comprehensive Understanding of Advanced Materials and Semiconductor Processing
		• Dong-Woo Jee, *Ajou University* In-sensor Processing Techniques for Biomedical Applications
		• Jihoon Seo, *Clarkson University* Integrating Sustainability into Semiconductor Manufacturing: A Comprehensive Approach to CMP Consumables
		• Hyejin Park, *Sungkyunkwan University* Locust Vision-Inspired Silver Nanowire-Based Printed Near-Infrared Image Sensor Label for Collision Avoidance
		• Joonhee Choi, *Stanford University* Advancing Nanoscale Quantum Sensing in Quantum-Photonic Hybrid Solid-State Devices
		• Younsu Jung, *Sungkyunkwan University* Towards Green and Scalable Flexible Electronics: R2R Printed 4-Bit Microprocessor with SWCNT-Based Logic
09:50~11:00		Poster Exhibition & Coffee Break

Day 2 | July 4, 2025 (Friday)

Room 210 & 211A, KINTEX Exhibition Center I

Discussion / Working Group	11:00~12:00	**Group Discussion Workshop**
		• Group I : Sustainability in Semiconductor Manufacturing by Design Co-chairs: Tae Gon Kim, Ahmed Busnaina
		• Group II : Neuromorphic & Quantum Sensors on a Chip Co-chairs: Seyoung Kim, Elias Towe
12:00~13:00		Lunch
Discussion / Working Group	13:00~14:00	**Group Discussion Workshop**
		• Group I : Sustainability in Semiconductor Manufacturing by Design Co-chairs: Tae Gon Kim, Ahmed Busnaina
		• Group II : Neuromorphic & Quantum Sensors on a Chip Co-chairs: Seyoung Kim, Elias Towe
Closing Session	14: 00~15:00	**Poster Award**
		Wrap-up Discussion
		Generate Recommendation to the Governments
		Signature of Overall Summary and Recommendation
		Closing Remarks

Opening Session

Co-chairs

Jo-won Lee / Myung S. Jhon

Co-Chairs

Jo-won Lee

Chairman, 3D Printing Research Organization

Web: http://www.3dpro.or.kr

E-mail address:jowon@3dpro.or.kr

| Biography

*** Education**

1971-1978 : B.S. in Metallurgical Eng. from Hanyang Univ.
1980-1983 : M.S. in Metals Science from Penn State Univ.
1982-1986 : Ph.D. in Metals Science from Penn State Univ.

*** Professional Positions**

1978-1980 : Researcher at ADD
1985-1990 : Research Associate at Carnegie Mellon Univ.
1990-1992 : Visiting Scientist at IBM T. J. Watson Research Center
1992-2000 : General Manager and Project Manager at SAIT
2000-2010 : Director at The National Program for Tera-level Nanodevices
2010-2019 : Professor at Hanyang University
2019-2023 : President at National Nanofab. Center
2023-Present: Chairman at 3D Printing Research Organization

*** Research Field and Interests**

His field of research is primarily neuromorphic devices with a variety of experiences such as magnetic media/head, high Tc superconducting devices, diamond devices and nanoelectronics/memory.

*** Professional Activities**

In 2001, he was a general secretary of the governmental planning committee for the 10 years Korea Nanotechnology Initiative. This plan has been revised in 2005 under the guidance of Dr. Lee as a principle investigator. He was serving as a first vice president of Korean nanotechnology research society in charge of international affairs and a chairman of advisory committee for nanotechnology information. He was also working as a Korean-side chairman of advisory committee for Korea-US nanotechnology forum and was an NT focal point of Korea-UK focal point programs. He has been also serving as Chair, NANO KOREA 2006, 2007, 2008 and 2009 Symposium Steering Committee. He completed national nanotechnology roadmap (Feb. 2008) and national nanotechnology standardization development roadmap (Oct. 2007) as a principle investigator. He was served as a general chair of IEEE-Nanotechnology Conference 2010. He was a chair of study group on neuromorphic devices in Korea.
He also served as a chairman of Korea Infrastructure Organization for Nanotechnology from 2020-2023.

Opening Remarks

- **Jinho Ahn,** *Korea Nanotechnology Research Society*

Welcoming Remarks

- **Taek-ryeol Jeong,** *Ministry of Science and ICT*
- **Seongsin Margaret Kim,** *National Science Foundation*

Keynote Speeches

John A. Rogers

Professor | Northwestern University

| Biography

Professor John A. Rogers obtained BA and BS degrees in chemistry and in physics from the University of Texas, Austin, in 1989. From MIT, he received SM degrees in physics and in chemistry in 1992 and a PhD degree in physical chemistry in 1995. From 1995 to 1997, Rogers was a Junior Fellow in the Harvard University Society of Fellows. He joined Bell Laboratories as a Member of Technical Staff in 1997 and then served as Director of the Condensed Matter Physics Research Department from the end of 2000 to 2002. He then spent thirteen years on the faculty at the University of Illinois, most recently as the Swanlund Chair Professor and Director of the Seitz Materials Research Laboratory. In the Fall of 2016, he moved to Northwestern University where he is Director of the Querrey-Simpson Institute for Bioelectronics. He has co-authored nearly 1000 papers and he is co-inventor on more than 100 patents, more than 70 or which are licensed to large companies or to startups that have emerged from his labs. More than 150 former members of his group are currently in faculty positions at top institutions around the world, including MIT, Princeton, Stanford (3x), Dartmouth (2x), Duke, Cornell, Vanderbilt, Northwestern, University of Southern California, University of Illinois at Urbana/Champaign (4x), University of North Carolina at Chapel Hill, Purdue University, University of California at San Diego, University of California at Santa Barbara, University of Texas at Austin, Texas A&M University (3x) and many others in the US, along with a large collection of universities in Europe and Asia, including TU Delft, ETH, Tsinghua (3x), Fudan (2x), Peking, SNU (3x), KAIST (3x), Univ. of Toronto and many others.

His research has been recognized by many awards, including a MacArthur Fellowship (2009), the Lemelson-MIT Prize (2011), the Smithsonian Award for American Ingenuity in the Physical Sciences (2013), the MRS Medal (2018), the Benjamin Franklin Medal from the Franklin Institute (2019), a Guggenheim Fellowship (2021), the James Prize for Science and Technology Integration from the NAS (2022) and the IEEE Biomedical Engineering Award (2024). He is a member of the National Academy of Engineering, the National Academy of Sciences, the National Academy of Medicine, the National Academy of Inventors and the American Academy of Arts and Sciences. He is also an elected Fellow of the Royal Society.

Semiconductor Nanomaterials in 3D and Transient Electronics

John A. Rogers

Professor | Northwestern University

| Abstract

A remarkable feature of modern integrated circuit technology is its ability to operate in a stable fashion, with almost perfect reliability, without physical or chemical change. Recently developed classes of electronic materials create an opportunity to engineer the opposite outcome, in the form of ‘transient’ devices that dissolve, disintegrate or otherwise disappear at triggered times or with controlled rates[1]. Water-soluble transient electronics serve as the foundations for applications in zero-impact environmental monitors, 'green' consumer electronic gadgetry and bio-resorbable biomedical implants. This presentation describes the essential concepts in chemistry, materials science and assembly processes for bioresorbable electronics in 1D, 2D and 3D architectures, the latter enabled by approaches that draw inspiration from the ancient arts of kirigami and origami. A focus will include our latest work in this area, ranging from 3D microflier structures for environmental monitoring[2,3] to the world’s smallest pacemakers for temporary use after a cardiac surgery[4].

Reference

[1] Y. Zhang, G. Lee, S. Li, Z. Hu, K. Zhao and J.A. Rogers, Chemical Reviews 123, 11722 (2023).
[2] H.-J. Yoon et al, Science Advances 8, eade3201 (2022).
[3] B.H. Kim et al, Nature 597, 503 (2021).
[4] Y. Zhang et al, Nature 640, 77 (2025).

Seongsin Margaret Kim

Program Director | National Science Foundation

| Biography

Dr. Margaret Kim currently serves as a Program Director for the Electronics, Photonics, and Magnetic Devices (EPMD) program within the Electrical, Communication, and Cyber Systems (ECCS) Division of the Directorate for Engineering (ENG) at the National Science Foundation (NSF). She is also a Professor of Electrical and Computer Engineering at the University of Alabama.

Dr. Kim earned her Ph.D. in Electrical and Computer Engineering and M.S. in Physics from Northwestern University, following a B.S. in Physics from Yonsei University in South Korea. Prior to joining the University of Alabama, she held research and academic positions at Stanford University as a Research Associate and Consulting Assistant/ Associate Professor. She also worked in industry at Agilent Technologies and Samsung.

Her research spans photonics, metamaterials, and terahertz (THz) technologies, with applications in next-generation biomedical diagnostics, quantum sensing, quantum networks, 6G/7G communications, AI-assisted bio-imaging, space and underwater exploration, and neurophotonics.

At NSF, Dr. Kim manages a broad portfolio of high-impact programs, including the Future of Semiconductors, the NSF-NIH joint initiative on quantum sensors for biomedical applications, the NSF-AFRL collaboration on Floquet-engineered quantum systems, Addressing Systems Challenges through Engineering Teams (ASCENT), Major Research Instrumentation Program (MRI) in addition to the core programs and among others. She is an active member of the Quantum Information Science and Engineering (QISE) working group. She is also deeply committed to advancing human-centered technologies across her programs.

Dr. Kim has authored over 180 publications, holds three patents, and is the recipient of the NSF CAREER Award. She is a Fellow of OPTICA, recognized for her pioneering contributions to photonics and THz science.

Research Progress and Perspective of Quantum Networking and Sensing

Seongsin Margaret Kim

1. National Science Foundation, USA
2. University of Alabama, USA

E-mail address:sekim@nsf.gov / seongsin@eng.ua.edu

| Abstract

The National Quantum Initiative (NQI) Act calls for coordinated efforts to accelerate quantum information science (QIS) and technology research in the United States. The National Science and Technology Council Subcommittee on Quantum Information Science identified a need for deliberate collaborations to combine fundamental and applied research on quantum sensors toward bringing quantum sensors to fruition.
Quantum sensing is broadly defined as fundamental sensing and imaging science based on quantum phenomena. Due to the unique and peculiar properties of various quantum states, quantum sensors have the potential to exhibit sensing and imaging capabilities beyond current classical limitations. Such highly sensitive quantum sensors are greatly needed in various applications, including but not limited to national security, communication, and defense. This talk will provide an overview of recent progress in quantum sensing, highlight current challenges, and outline future research directions—particularly at the intersection of quantum sensing and quantum networking—aimed at realizing practical and deployable quantum sensor technologies.

Heung Soo Park

President | National NanoFab Center, Daejeon, Korea

| Biography

Heung Soo Park is the President of National NanoFab Center (NNFC), located in the campus of Korea Advanced Institute of Sceince and Technology (KAIST), Daejeon, Republic of Korea. NNFC is the nation's largest semiconductor public R&D facility (including 5,000m2 cleanroom) offering technology platform services to the industry, academia and R&D institutes in the areas of silicon-based semiconductor, MEMS-based sensors, Nano-Bio and Display while nurturing new technologies in house. It also provides semiconductor education courses for college students and graduates with in-house training programs, e.g. process and equipment training, as well as continuing education programs for semiconductor professionals in the industry.

Heng Soo Park has spent more than 30 years in the semiconductor field, mostly in the industry including Samsung Electronics (Korea), Texas Instruments (Dallas, Tx, USA) and DB Hitek (Korea). He was a research professor at Yonsei University, Seoul before joining NNFC as president. He graduated from Seoul National University with a BS and a MS degree in metallurgical engineering in 1983 and 1985, and obtained a Ph.D. degree in materials science and engineering from Stanford university in 1994.

The Role of National NanoFab Center for Advancing Nanotechnology Research, Education, and Commercialization in Korea

Heung Soo Park

President | National NanoFab Center, Daejeon, Korea

| Abstract

Public semiconductor fabrication facilities play a crucial role in advancing nanotechnology research, education, and commercialization. One of their core functions is to democratize access to expensive nanofabrication equipment for universities and small companies while enabling research that would otherwise be cost-prohibitive.

Established in 2004 as an affiliated organization of Korea Advanced Science and Technology (KAIST) in Daejeon, Korea, NNFC has focused on supporting domestic industries, academic institutions and other R&D institutes with a world-class infrastructure in the cleanroom environment. Its main service domains include semiconductor fabrication platforms for testbed service (8 inch and 12 inch) and logic CMOS (8 inch/0.18um), semiconductor and display convergence technology platforms, nano-biosensor/chip fabrication platforms, MEMS sensor fabrication platform and analysis and measurement service. For education and training, its Semiconductor Academy offers education courses with hands-on experience for high school, college students and graduates in the semiconductor cleanroom. The Academy also offers continuing education programs for semiconductor professionals in industry.

As technology advancement in the semiconductor industry faces complex challenges, collaboration among academia and research institutes including public semiconductor facilities is becoming more important than ever. NNFC has been collaborating with the New York Center for Research, Economic Advancement, Technology, Engineering and Science (NY CREATES) since May, 2024; professors from both countries are working on the same topics using either NNFC or NY CREATES facilities and some Korean companies are in discussion with NY CREATES for testbed services. Starting this year, NNFC will send more than 10 graduate students every year to IMEC where they are working as research assistants in semiconductor related research projects. All funding for the collaboration with NY CREATES and IMEC is provided by the Ministry of Science and ICT. For testbed services, NNFC is open to foreign entities including academia and industry and currently we have several customers from USA, Sweden and Germany for processing wafers and devices.

The Role of National NanoFab Center for Advancing Nanotechnology Research, Education, and Commercialization in Korea

Heung Soo Park

President | National NanoFab Center, Daejeon, Korea

Reference

NNFC will focus mainly on three initiatives;

[1] Enhancing collaboration and cooperation between domestic and international public semiconductor facilities and the private sectors

[2] Upgrading in-house capabilities to keep up with future technologies such as advanced packing technology, quantum sensor technology and AI

[3] Maintaining sustainability with 'safety first' principle and improving energy efficiency while following green chemistry principles.

Scaling Knowledge Processing from 2D Chips to 3D Brains

Kwabena Boahen

Professor | Stanford University, USA

| Biography

Kwabena Boahen is a Professor of Bioengineering, Electrical Engineering, and by courtesy Computer Science at Stanford University; an investigator in Stanford's Bio-X Institute, System X Alliance, and Wu Tsai Neurosciences Institute; and the founding director of Stanford's Brains in Silicon Lab. His group models the nervous system computationally to elucidate principles of neural design at the cellular, circuit, and systems levels; and synthesizes neuromorphic electronic systems whose energy-use scales with their size as efficiently as the brain does. He earned a doctorate in Computation and Neural Systems at the California Institute of Technology in 1997. From 1997 to 2005 he was on the faculty of University of Pennsylvania, Philadelphia PA, where he was the inaugural holder of the Skirkanich Term Junior Chair. His research has resulted in over a hundred publications, including a cover story in Scientific American featuring his lab's work on a silicon retina and a silicon tectum that "wire together" automatically (May 2005). He has been invited to give over a hundred seminar, plenary, and keynote talks, including a 2007 TED talk, "A computer that works like the brain", with over seven hundred thousand views. He has received several distinguished honors, including a Packard Fellowship for Science and Egineering (1999) and a National Institutes of Health Director's Pioneer Award (2006). He was elected a fellow of the American Institute for Medical and Biological Engineering (2016) and of the Institute of Electrical and Electronic Engineers (2016) in recognition of his lab's work on Neurogrid, an iPad-size platform that emulates a million neurons in the cerebral cortex in in real time, which hitherto required a supercomputer. He has trained over twenty graduate students and mentored four postdoctoral researchers, including the designers of IBM's TrueNorth chip and NeuraLink's implantable chip, and the founders of Femtosense and Dexterity.

Scaling Knowledge Processing from 2D Chips to 3D Brains

Kwabena Boahen

Professor | Stanford University, USA

E-mail address: boahen@stanford.edu

| Abstract

Artificial intelligence (AI) realizes a synaptocentric conception of the learning brain with dot-products and advances by performing twice as many multiplications every two months. But the semiconductor industry tiles twice as many multipliers on a chip only every two years. Moreover, the returns from tiling these multipliers ever more densely now diminish, because signals must travel relatively farther and farther, expending energy and exhausting heat that scales quadratically. As a result, communication is now much more expensive than computation. Much more so than in biological brains, where energy-use scales linearly rather than quadratically with neuron count. That allows an 86-billion-neuron human brain to use as little power as a single lightbulb (25W) rather than as much as the entire US (3TW). Hence, rescaling a chip's energy-use from quadratic to linear is critical to scale AI sustainably from 10^{12} parameters (mouse scale) today to 10^{15} parameters (human scale) in the next five years. But this would require communication cost to be reduced radically. Towards that end, I will present a recent re-conception of the brain's fundamental unit of computation that sparsifies signals by moving away from synaptocentric learning with dot-products to dendrocentric learning with sequence detectors.

Reference

[1] K. Boahen, Nature 612, 43-5056 (2022).
[2] H. Chen et al., IEDM 2023, 1-4 (2023).

New Chips R&D Initiative – Semiconductor Manufacturing and Advanced Reserch with Twins

Victor Zhirnov

Chief Scientist | Semiconductor Research Corporation, USA

| Biography

Victor Zhirnov is Chief Scientist at the Semiconductor Research Corporation. He is responsible for envisioning new long-term research directions in semiconductor information and communication technologies for industry and academia. His semiconductor experience spans over 30 years in the areas of materials, processes, device physics and fundamental limits. Victor served as the Chair for the Emerging Research Device Working Group for the International Technology Roadmap for Semiconductors (ITRS) and for the 2030 Decadal Plan for Semiconductors. Currently, he is Chair of the Microelectronics and Advanced Packaging Technologies Roadmap. Victor received the M.S. in applied physics from the Ural Polytechnic Institute, Yekaterinburg, Russia, and the Ph.D. in solid state electronics and microelectronics from the Institute of Physics and Technology, Moscow, in 1989 and 1992, respectively. He has authored and co-authored over 150 technical papers and contributions to books.

New Chips R&D Initiative –
Semiconductor Manufacturing and Advanced Reserch with Twins

Victor Zhirnov

Chief Scientist | Semiconductor Research Corporation, USA

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| Abstract

Demand for semiconductors continues to surge across sectors with the rise of artificial intelligence, cloud computing, and growing connectivity demands in other critical industries. The CHIPS and Science Act represents a historic $280 billion investment to rebuild American semiconductor manufacturing, yet success requires more than just new fabs—it demands revolutionary approaches to accelerate development cycles, reduce costs, and enhance manufacturing efficiency to compete globally.

Digital twins represent the most promising technological pathway to address these manufacturing challenges. The transformative potential of digital twins in semiconductor manufacturing extends beyond operational efficiency, encompassing broader applications such as workforce development and supply chain resilience. However, realizing this potential requires addressing fundamental challenges, including data standardization, interoperability across diverse systems, and the development of secure, scalable infrastructure that enables seamless integration from unit processes to complex system-of-systems representations—precisely the mission of the SMART USA Manufacturing Institute.

SMART USA aims to address critical gaps in semiconductor manufacturing through the development of scalable digital twin technologies. This initiative seeks to create innovative projects that advance digital twin capabilities to optimize semiconductor design, manufacturing, packaging, assembly, and testing processes. Through collaborative research, SMART USA strives to enhance U.S. semiconductor manufacturing competitiveness, reduce costs, improve yields, and develop a skilled workforce that can leverage these transformative technologies

Session I

Sustainability in Semiconductor Manufacturing by Design

Co-chairs

Tae Gon Kim / Ahmed Busnaina

Ahmed Busnaina

Ph.D | Northeastern University

| Biography

Ahmed A. Busnaina, Ph.D., is the founding Director of the National Science Foundation's Nanoscale Science and Engineering Center for High-rate Nanomanufacturing since 2004 and the NSF Center for Microcontamination Control at Northeastern University, Boston, MA, since 2002. He is also the founder and CTO of Nano OPS, Inc. since 2017. Prior to joining Northeastern University, he was a professor and a director of the Particulate Control Lab at Clarkson University from 1984-2000. Dr. Busnaina is internationally recognized for his work on semiconductor fabrication with an emphasis on yield. He also developed nano and microscale additive manufacturing for making interconnects, passive and active electronic components, LEDs, and sensors. He authored more than 600 papers in journals, proceedings, and conferences. He also has 25 granted and 45 pending patents. He was awarded the 2020 American Society of Mechanical Engineers (ASME) William T. Ennor Manufacturing Technology Award and Medal. He is a fellow of the National Academy of Inventors, a fellow of the American Society of Mechanical Engineers, and a Fulbright Senior Scholar. He is an editor of the Journal of Microelectronic Engineering. He also serves on many advisory boards, including Samsung Electronics, the Journal of Electronic Materials Letters, the Journal of Nanomaterials, and the Journal of Nanomanufacturing.

Sustainable Additive Manufacturing of Electronics and 3D Heterogenous Integration for Advanced Packaging

Ahmed Busnaina

Ph.D | Northeastern University

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| Abstract

What if there were an electronics manufacturing technology that could reduce costs by 10-100 times compared to conventional semiconductor manufacturing and the carbon footprint by more than one order of magnitude? Imagine if this technology does not use any corrosive or toxic chemicals. Such a technology exists, and it is the topic of this presentation. It is enabled by the directed assembly of suspended nanoparticles [2] at room temperature and pressure and manufactures devices 1000 faster and 1000 smaller structures than inkjet-based or 3D printing. The process is scalable, environmentally sustainable, and enables precise and repeatable manufacturing of various nanomaterials at a very high rate. This allows the printing of passive and active components monolithically on an interposer platform along with a trace such that the total footprint can be within a few mm of the original IC footprint. The technology has been sown to reduce the carbon footprint by 10-20 times depending on the type of directed assembly method used. The presentation will show the electrical properties of capacitors, resistors, and transistors that are made using a fully additive process down to the submicron scale without using etching, vacuum, or chemical reactions. The presented technology enables the printing of single-crystal conductors and semiconductors [3]. The process demonstrates the manufacturing of transistors with an on/off ratio greater than 106.

An immediate application for this technology is 3D heterogeneous integration for advanced packaging applications, where there is a need to shrink the size of traces and interconnects to integrate different passive and active components, including memory, microcontrollers, and power electronics. The new ultrafine resolution requirements for 3D heterogeneous integration have prompted many advanced packaging processes to be transferred to foundries, rather than relying on traditional packaging processes. This led to a much higher cost that made the most advanced packaging applications out of reach for many small companies. This additive high-throughput manufacturing solution can enable low-cost trace, interconnect, passive, and active components manufacturing.

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Hak-Sung Kim
Professor | Hanyang University

| Biography

Professor Hak-Sung Kim received his Ph.D. in Mechanical Engineering from KAIST in 2006. From 2006 to 2008, he worked at Samsung Electronics' Semiconductor Packaging Center as a senior researcher. He then continued his academic career as a postdoctoral researcher and lecturer at the University of California, Los Angeles (UCLA) from 2008 to 2010. Since 2010, he has been a faculty member in the Department of Mechanical Engineering at Hanyang University.

For over 20 years, Professor Kim has been actively engaged in advanced semiconductor packaging research. Since 2022, he has served as the Director of the Hanyang Advanced Semiconductor Packaging Center, where he leads multidisciplinary research efforts focused on next-generation semiconductor packaging technologies.
His main research themes include:

- Development of innovative processes for semiconductor packaging
- Characterization and reliability analysis of packaging materials
- AI-driven prediction and modeling of packaging warpage and deformation

Professor Kim is recognized for bridging mechanical engineering fundamentals with advanced electronic packaging applications, contributing to both academic advancements and industrial innovations in semiconductor packaging.

Milli-Seconds Multi Flip-Chip Bonding Process via Intense Pulsed Light Irradiation for Sustainability of Semiconductor Packaging Manufacturing

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| Abstract

This presentation introduces a novel approach to achieving sustainability in semiconductor manufacturing through process innovation and design, with a focus on packaging technologies. In particular, it highlights a breakthrough in interconnection technology by replacing the conventional energy-intensive reflow soldering process with an ultra-fast, white-light solder bonding method [1]. The proposed white-light soldering process utilizes intense broadband light pulses lasting only tens of milliseconds to achieve solder joint formation. In this work, a numerical thermal transient simulation model was developed and validated by comparing with in situ monitoring results. The temperature profiles according to IPL parameters (pulse on-time, frequency, and pulse number) were investigated to effectively reduce bonding process time and maximum temperature of flip-chip bonding process.

The thickness of intermetallic compounds (IMC) was effectively reduced from 6 μm in the conventional reflow process to approximately 800 nm in the IPL flip-chip bonding process, as the process time was significantly shortened from 90 seconds to 56.4 milliseconds and the maximum temperature was lowered from 250 °C to 221.7 °C. Die shear tests demonstrated that the IPL flip-chip bonding process improved die shear force by 30% compared to conventional reflow processes. This study demonstrates that the IPL flip-chip bonding process could produce 3D multi-chip packages with excellent mechanical reliability. Compared to conventional reflow soldering, this method offers approximately 40% reduction in energy consumption and significantly shortens the process time from several minutes to mere milliseconds.
This talk will explore how such innovative bonding design and process improvements contribute to sustainable semiconductor packaging and provide insights into the future of eco-efficient advanced packaging technologies.

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Paul Westerhoff

Professor | Arizona State University

| Biography

Dr. Paul Westerhoff is a Regents Professor in the School of Sustainable Engineering and the Built Environment at Arizona State University and the Fulton Chair of Environmental Engineering. He joined ASU in 1995 and after serving as the Civil and Environmental Engineering Department Chair he was the Founding Director for the School of Sustainable Engineering and the Built Environment, plus additional administrative roles as Associate & Vice Dean of Research in Engineering and ASU Vice Provost for Academic Programming. He is the Director of the Global Center of Water Technology, Deputy Director of a NSF ERC (newtcenter.org) co-Deputy Director of the NSF Science and Technologies for Phosphorus Sustainability Center (steps-center.org). He has over 425 journal publications (H-index>110) and multiple patents on his research related to fate of nanomaterials in water, developing novel technologies for water and reuse treatment, and understanding reactions related to the fate of pollutants during treatment or in natural systems with a focus on oxo-anions, natural organic matter and micropollutants. He is the recipient of several awards including the recipient of the 2020 A.P. Black award from the American Water Works Association, 2019 NWRI Clarke Prize for excellence in the fields of water science and technology, 2017 Sustainable Nanotechnology Organization Annual Achievement Award, ASU Outstanding Doctoral Mentor for 2015, 2013 ARCADIS/AEESP Frontier in Research Award, and 2006 Paul L. Busch Award. He was elected to the National Academy of Engineering in 2023.

Barriers Associated with Trace Organics and Discoveries on How to Reuse Semiconductor Fab Wastewater for Ultrapure Make-up Water

Paul Westerhoff, Junli Wang, and Hyunki "Arnold" Jung

Professor | Arizona State University

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| Abstract

Semiconductor fabrication is water-intensive, consuming tens of billions of gallons annually for fabrication and packaging, plus supply chain chemicals. As Arizona faces long-term water constraints, ensuring the industry's sustainability will depend on transformative advances in water reuse. Fabs in Arizona can reuse up to ~30% of their industrial wastewater for cooling towers, gas scrubbers and other facilities. The remaining 70% of the wastewater could be reused to make chips again, but there is concern about industrial chemicals in the wastewater impacting chip production. We hypothesize, and have started demonstrating, that treatment of industrial wastewater by reverse osmosis will be unsatisfactory for reuse, even in passed through a conventional ultrapure water (UPW) system, because of the presence of low molecular weight organics (LWOs). The most concerning LWOs include urea, TMAH, acetone and a few others, which are not removed by conventional UPW systems. While hydroxyl radicals are ineffective at treatment these LWOs in RO permeate, we have successfully demonstrated in the lab that other radical species (e.g., sulfate radical, bromide radical) generated during novel advanced oxidation processes (AOPs) effectively mineralize these compounds to carbon dioxide. Residual salts from our AOPs would be effectively removed by conventional UPW systems, thus providing a path to ultra-low level total organic carbon and other standards needed for ultrapure water suitable for us in making the most advanced computer chips.

Jin-Seong Park
Professor | Hanyang University

| Biography

Professor Jin-Seong Park holds positions as a professor in the Division of Material Science and Engineering, as well as in the Division of Nano-scale Semiconductor Engineering at Hanyang University. His research group is primarily dedicated to Semiconductor Materials & Devices utilizing Atomic Layer Process (ALP), with a focus on Oxide Semiconductor channel layers (both n and p type), Gate Insulators (including SiO2, SiNx, and high-k dielectrics), Area-Selective Atomic Layer Deposition, and Atomic Layer Etching, among other areas of study. During the period spanning 2005 to 2009, he was engaged in pioneering work at Samsung SDI, concentrating on the development of innovative active-matrix devices employing IGZO semiconductor technology for AMOLED applications. His contributions were instrumental in the realization of mass-produced AMOLED televisions and flexible AMOLED displays utilizing IGZO transistors. From 2003 to 2005, Professor Park served as a post-doctoral researcher in the chemistry department of Harvard University. During this time, his focus was on the development of novel precursors and the advancement of oxide & metal Atomic Layer Deposition (ALD) processes. Professor Park earned his Ph.D. degree from KAIST in 2002, with a dissertation titled "TiN, TiSiN, and TaN for Cu Diffusion Barriers using Plasma Enhanced ALD." His academic achievements include the publication of over 300 SCI(E) papers and the acquisition of more than 100 issued patents related to active-matrix devices and ALD materials. In addition to his research and academic pursuits, Professor Park contributes to the scholarly community as an Associate Editor for the IEEE Transactions on Electronic Devices and holds the position of executive director within the Thin Film Division of the American Vacuum Society.

Designing Sustainable Area-Selective ALD:
A Data-Driven Framework for Inhibitor Engineering

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| Abstract

In the pursuit of environmentally sustainable and efficient semiconductor manufacturing, area-selective atomic layer deposition (AS-ALD) has emerged as a promising bottom-up patterning method that eliminates the need for conventional etch and resist processes. This presentation introduces a design-driven approach for enhancing AS-ALD selectivity by integrating density functional theory (DFT) calculations, random sequential adsorption (RSA) simulations, and surface-sensitive experimental validations.[1-3]

We present a systematic investigation into the role of small molecular inhibitors (SMIs) with phenyl-based silane structures, including TCPS, MDCPS, CDMPS, and DCDPS, focusing on their chemical and physical passivation capabilities. DFT results reveal that these inhibitors selectively adsorb on SiO_2 surfaces through exothermic interactions, while avoiding adsorption on TiN surfaces, establishing the chemical foundation for selective inhibition. RSA simulations further demonstrate how molecular size and steric configuration affect surface packing density, interparticle spacing, and shielding efficiency, which are critical for preventing undesired precursor infiltration.

To quantitatively assess the selectivity performance, we introduce a holistic metric termed the S-factor, which integrates chemical deactivation (based on surface energy and hydroxyl consumption) and physical shielding (from molecular structure and spatial coverage). Experimental evaluations, including water contact angle, X-ray photoelectron spectroscopy (XPS), and Auger electron spectroscopy (AES), validate the computational predictions. AS-ALD of MoO_2 and VO_2 on TiN/SiO_2 patterned substrates confirms the strong correlation between the S-factor and actual deposition selectivity over multiple cycles.

This framework not only identifies MDCPS as an optimal inhibitor with high S-factor due to its balance of adsorption strength and spatial coverage, but also offers a generalized design principle for inhibitor selection based on precursor and substrate combinations. By correlating theoretical predictions with practical outcomes, our approach advances the precision and sustainability of AS-ALD processes.
Ultimately, this research demonstrates how inhibitor molecule design—guided by theoretical modeling and quantitative metrics—can reduce material waste, eliminate etch residues, and enable more sustainable semiconductor fabrication. This design-centric strategy serves as a blueprint for future atomic-scale manufacturing platforms, where simulation-led process optimization can contribute to greener, more resource-efficient production paradigms.

Designing Sustainable Area-Selective ALD:
A Data-Driven Framework for Inhibitor Engineering

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Professor | Hanyang University

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Fazleena Badurdeen

Professor | University of Kentucky

| Biography

Fazleena Badurdeen is the Earl Parker Robinson Chair Professor in the Department of Mechanical and Aerospace Engineering at the University of Kentucky. She also serves as the Director for the Manufacturing Systems Engineering master's program and is a core faculty member at the University of Kentucky's Institute for Sustainable Manufacturing, an internationally recognized center of excellence focused on cutting-edge research and technology development for sustainable products, processes and systems. Prof. Badurdeen is recognized for her expertise in sustainable and circular product design, measurement systems for circularity and sustainability evaluation, and modeling and analysis of manufacturing systems and supply chains. She has been involved in externally funded research exceeding $20 million and has published over 150 peer-reviewed papers. Prof. Badurdeen is the founding Chair of the International Forum on Sustainable Manufacturing and has served as a Technical Vice President for the Institute of Industrial and Systems Engineers (IISE). She is also an Editor for the Resources, Conservation, and Recycling journal and serves on the editorial boards of a number of other journals. Prof. Badurdeen received her PhD in Integrated (Industrial and Mechanical) Engineering and MS in Industrial Engineering, both from Ohio University, USA. She also holds an MBA from the Postgraduate Institute of Management, Sri Lanka and BS in Engineering from the University of Peradeniya, Sri Lanka. Prof. Badurdeen is a Fellow of IISE.

Closing the Loop:
Advancing Circularity in Semiconductor Chips and Chip-integrated Components

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| Abstract

Growing concern over the environmental impacts of semiconductor manufacturing and the increasing disposal rates of chip-integrated products have brought renewed focus to improving sustainability across the microelectronics sector. The Circular Economy presents a compelling framework to shift from traditional linear production models toward restorative and regenerative systems. Applying circular principles to the semiconductor industry holds significant promise for advancing sustainability throughout the lifecycle of chips—from manufacturing to use and end-of-life (EoL) management.

This presentation will explore ongoing efforts to identify the requirements for enabling circular resource flows in semiconductor chips and chip-integrated microelectronic components and subassemblies (MCS). It will examine the challenges posed by the industry's highly specialized and fragmented supply chains, which complicate the closure of material loops. The presentation will also highlight emerging initiatives focused on the collection, recovery, and repurposing of EoL MCS for multiple lifecycle applications, along with research assessing the feasibility of chip and component reuse. Finally, it will identify critical intervention points across design, manufacturing, and EoL phases that are essential to supporting a transition toward a more circular and sustainable microelectronics ecosystem.

Jungwan Cho
Professor | Sungkyunkwan University

| Biography

Dr. Cho is an Associate Professor in the School of Mechanical Engineering at Sungkyunkwan University (SKKU), Korea. At SKKU, he leads the Multi-Scale Heat Transfer (MHeat) Laboratory, which conducts both experimental and theoretical research in electronics cooling, semiconductor materials, and advanced packaging. His research particularly focuses on nano- and microscale heat transfer in advanced semiconductor thin films and at interfaces, utilizing state-of-the-art thermal characterization techniques such as pump-probe thermoreflectance. More recently, his group has also been developing innovative thermal metrology methods for Metrology & Inspection (MI) applications in advanced packaging.

Dr. Cho received his B.S. degree (2008) in Mechanical Engineering from Seoul National University (SNU), and his M.S. (2010) and Ph.D. (2014) degrees in Mechanical Engineering from Stanford University, where he was supported by the Samsung Scholarship. He subsequently conducted postdoctoral research in the Stanford NanoHeat group and joined the SKKU faculty in 2020 after a productive period as a faculty member at Kyung Hee University, Korea. At SKKU, he was awarded the 성공(成工) Young Fellowship (2024) from the College of Engineering. He is also the recipient of the Young Thermal Scientist Award (2025) from the Thermal Engineering Division of the Korean Society of Mechanical Engineers (KSME) and the Young Engineer Award (2018) from the Korean Society for Precision Engineering (KSPE).

Electro-Thermal Co-Design of High-Power Semiconductor Devices

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| Abstract

Phonon conduction governs heat removal and cooling in a wide range of modern semiconductor devices. Electrons in the active device junction emit phonons, which subsequently carry heat away from the heated electronic region. In many transistors, defects and interfaces near the active junction impede phonon conduction and thus significantly reduce the thermal conductivity of the near-junction materials (by up to orders of magnitude compared to their bulk values), leading to substantial junction temperature rises that degrade device performance and reliability [1]. The problem is arguably most severe in high-power wide bandgap (e.g., GaN) and ultrawide bandgap (e.g., Ga2O3) transistors, where local power densities can approach several MW/cm2 [2,3].

This talk will summarize our efforts to implement electro-thermal co-design for WBG GaN and UWBG Ga2O3 electronics. We will discuss (i) the use of laser-based pump-probe thermoreflectance techniques, such as frequency-domain thermoreflectance, to measure the thermophysical properties of device material stacks [4], (ii) an electro-thermal device modeling scheme capable of predicting the temperature-dependent electrical output characteristics as well as the device self-heating behavior [5], and (iii) the use of the electro-thermal model to design novel thermally-aware device structures [6,7].

Acknowledgments

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Sung Kyu Lim
Professor | Georgia Institute of Technology

| Biography

Prof. Sung Kyu Lim earned his Ph.D. in Computer Science from UCLA in 2000. Since 2001, he has been a faculty member at the School of Electrical and Computer Engineering at the Georgia Institute of Technology. His research explores the architecture, design, and electronic design automation (EDA) of 2.5D and 3D integrated circuits, contributing to over 400 published papers. He received the Best Paper Awards from the IEEE Transactions on CAD in 2022 and the ACM Design Automation Conference in 2023. He is an IEEE Fellow and served as a program manager at DARPA's Microsystems Technology Office from 2022 to 2024.

AI-Driven Co-Optimization of Design and Manufacturing for Heterogeneous AI Chips

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| Abstract

The efficiency of data movement between dies, whether mounted or stacked on silicon or glass substrates, is heavily influenced by the electro-thermo-mechanical properties of the interconnects and the bonding techniques used. Conventional evaluations of these materials and technologies often rely on metrics such as resistivity, coefficient of thermal expansion, Young's modulus, pitch, and interconnect width. However, these parameters do not directly correlate with critical system-level metrics such as performance, power consumption, and area efficiency.

In this presentation, we introduce AI/ML-based approaches to accurately and efficiently model the relationship between manufacturing properties and system performance. We demonstrate how these models enable co-optimization of manufacturing and system design, with a focus on heterogeneous chip architectures for AI accelerators. By leveraging predictive analytics, we aim to bridge the gap between materials science, advanced packaging, and system architecture—driving the next wave of semiconductor innovation for AI applications.

Jiyoung Kim
Professor | The University of Texas at Dallas

| Biography

Dr. Jiyoung Kim received his B.S. and M.S. in Metallurgical Engineering from Seoul National University and his Ph.D. in Materials Science and Engineering from the University of Texas at Austin. He was awarded the prestigious Korean Government Scholarship for Study Overseas. After working as an Integration Engineer at Texas Instruments, Dr. Kim worked as a faculty member at Kookmin University (Seoul, Korea) (1996-2005). In 2005, Dr. Kim joined UT-Dallas as an associate professor and was promoted to a full professor. Since 2000, Dr. Kim has led groundbreaking research on atomic-scale semiconductor processing, materials, devices, and characterization, with a focus on atomic layer deposition (ALD). He introduced innovative in-situ characterization techniques, including XPS, FT-IR, and electrical probing, to better understand reaction mechanisms and interface formation during ALD processes. Dr. Kim has pioneered the development of advanced ALD processes using a variety of new precursors, including organometallic compounds, high-purity ozone, hydrogen peroxide, hydrazine, and nitrogen radicals. These innovations have enabled low-temperature processes, improved dielectric quality, and enhanced conformality, particularly in complex 3D structures. His research encompasses the development of novel organic-inorganic materials for EUV photoresists and semiconductor applications. His research has received substantial support from both government agencies and the semiconductor industry, including NSF, DoD, DoE, Texas State, and the Korean Government, as well as from semiconductor consortia like SRC (USA) and COSAR (Korea). His research has been directly supported by 20 companies worldwide, including TI, Qorvo, Samsung, SK-hynix, Intel, Dow, TMEIC, Air Liquide, Lam, Rasirc, and others. Dr. Kim has published over 350 peer-reviewed journal articles and conference papers, with an H-index of 58 and more than 15,000 citations (Google Scholar). He has also given more than 100 invited talks and colloquia at professional society meetings, academic conferences, and industry events. Dr. Kim is actively involved in the professional community, serving as the co-chair of the 2013 ALD Conference in San Diego (with over 700 attendees), as well as a program committee member since 2011. He was also the vice-chair of the 2009 IEEE ISAGST in San Francisco and has contributed to various international society committees, including IEEE-EDS, TMS, AVS, UKC, and MNC etc.

Machine Learning for Accelerating Atomic Layer Deposition Process Optimization

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| Abstract

Artificial intelligence (AI) is driving the development of more convenient and efficient technological systems. Industry 4.0 integrates 'intelligent' information technology into manufacturing and industrial processes, with machine learning (ML) promising to increase flexibility and efficiency while minimizing process errors [1]. This transformative technology is expected to enhance virtually every sector of modern society, revolutionizing systems and protocols across diverse fields. The integration of ML is particularly valuable in semiconductor fabrication, where current processes have become increasingly complex, often requiring over 30 steps to deposit a single high-quality film layer. Consequently, process optimization has become crucial for achieving high-quality films and simplifying process steps. To meet these demands, proof-of-concept of ML-driven processes is essential to validate their potential in advancing semiconductor manufacturing.

Among semiconductor fabrication techniques, ALD processes have been highlighted due to their precise control of atomic-scale film engineering and their compatibility with advanced 3D semiconductor architectures. However, ALD involves numerous critical parameters that influence film quality. The comprehensive exploration of all possible ALD process conditions is economically unfeasible, as each experimental run costs over $1,000 per wafer, plus additional labor and analysis costs [2]. This constraint forces us to narrow the inspection ranges of ALD conditions out of potentially trillion combinations. Such limited sampling hinders the creation of highly accurate, atomic-scale process models. In this context, the incorporation of AI technologies shows promise in improving the cost-efficiency of process development by potentially decreasing the volume of data necessary for developing new process technologies.

In this presentation, we discuss the applications of a deep neural network (DNN) framework as an ML-driven atomic layer deposition (ALD) process, with a focus on hafnium oxide (HfOx) film analysis. ML applications in ALD processes have shown promise; however, they have primarily focused on monitoring film thickness and performing the prediction tasks [3]. Although film thickness serves as a valuable indicator of chemical reactions based on the ALD window, analyzing film quality, particularly film density, is crucial for achieving superior film performance. We demonstrate the properties of film density using the wet etch rate (WER) test, which leverages the principle that higher-density films have more tightly packed atoms, increasing resistance to etchant penetration and reaction

Machine Learning for Accelerating Atomic Layer Deposition Process Optimization

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| Abstract

with HfOx films. Furthermore, a comprehensive ML framework is expanded to include a DNN system, generating prediction maps for further process optimization, as well as dependencies on ALD parameters. This proof-of-concept of DNN integration into the ALD process marks a simplification of experimental design, demonstrating how these innovations are reshaping creative methods for process optimization.

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Pascal Oberndorff
Dr. | NXP Semiconductors

| Biography

Pascal Oberndorff holds a Master and Ph.D. degree from the department of Chemical Engineering of the Eindhoven University of Technology, the Netherlands. He joined Philips Development Laboratories in 2001 as a materials scientist. In 2005 he switched to Package Innovation at Philips Semiconductors/NXP, where his initial responsibility was the introduction of Pb-free technology and eventually team-lead for the packaging materials team. In 2010 he returned to Philips, working on LED development and packaging for LED lighting at the Lighting division. In 2014 he rejoined NXP Package Innovation, where he was responsible for new product introduction in packaging for automotive industry until 2023. Since 2023 he is responsible for the Packaging Core Technology department within Package Innovation. This world-wide department encompasses materials, (thermo-mechanical/thermal) modeling, platform management and technology scouting of Electronic Packaging. He has (co-) authored around 30 publications and conference contribution about Pb-free introductio, materials technology, package development in automotive technology.

Electronic Packaging Enabling the Future of Semiconductors

Pascal Oberndorff
Dr. | NXP Semiconductors

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| Abstract

In the recent decades semiconductors have become increasingly important in daily life, going from analog (such as computers and mobiles) to an on-demand world (data centers, smartphones and tablets).

In the upcoming era the influence of semiconductors will expand to the robotics era (AI from cloud to edge, smart connected devices).For these technologies miniaturization, which traditionally was dictated by the front end technology nd wafer nodes, will play a vital role.

Recent years have shown that now electronic packaging is becoming increasingly important not only to achieve the miniaturization, but also cost effectiveness, . It can even be stated that packaging will enable and further accelerate this upcoming robotic era through heterogenous integration and thus becoming essential for further innovation. With heterogenous integration the packaging aspect has to be closely matched with front end technology, creating system level solutions. In order to operate efficiently at the edge these systems should be able to sense, think connect and act.
In order to ensure proper functionality of these systems, a profound understanding of the behavior of the system, both during manufacturing as well as during the lifespan, is of the utmost importance. In order to achieve this material selection based on material characteristics and modeling of the thermo-mechanical and thermal behavior ensures optimal functionality.

In this presentation the above mentioned concepts will be demonstrated by examples in the field of radar and communications.

Session II

Neuromorphic & Quantum Sensors on a Chip

Co-chairs

Seyoung Kim / Elias Towe

Elias Towe
Professor | Carnegie Mellon University

| Biography

Elias Towe is the Albert and Ethel Grobstein Professor, and University Professor in the Department of Electrical and Computer Engineering at Carnegie Mellon. Towe's group pursues research in optical and quantum phenomena in semiconducting materials for applications in novel photonic devices and systems that enable a new generation of information processing systems for communication, computing, and sensing. Current device- and subsystem-level research includes work on quantum sensors, single-photon light sources, and quantum entropy generators for secure communication. Prof. Towe is currently Director of the National Science Foundation Industry-University Center on Quantum Computing and Information Technologies (QCiT) at Carnegie Mellon. The research at the Center is in the broad areas of quantum computing and quantum networks. In computing, the team is focusing on the computing stack: from the bottom qubit layer, through the gate control to the compiler/transpiler layer, to the top algorithmic layer, including software for use-case applications in select areas. In networks, the team works on secure quantum networks for distributed computing and communication, including networked sensors.

Towe received the S.B., S.M., and Ph.D. degrees from the Department of Electrical Engineering and Computer Science at the Massachusetts Institute of Technology in Cambridge, MA, where he was a Vinton Hayes Fellow. He is a Fellow of the IEEE, Optica (formerly OSA), American Physical Society, and the American Association for Advancement of Science. He is a recipient of several academic and professional awards that include the John Bardeen Award. Prof. Towe is a Member of the US National Academy of Engineering.

Solid-state Quantum Magnetometers

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| Abstract

Although ordinary magnetometers are generally bulky, they can measure and resolve magnetic flux densities larger than the earth's magnetic field of 25 to 65 micro-Tesla. A quantum magnetometer, based on the spin of sub-atomic particles such as unpaired valence electrons or nuclei of atoms, should, in principle, be capable of measuring and resolving magnetic flux densities on the order of a pico- to femto-Tesla, which makes it attractive for biomedical applications. This talk will discuss magnetometers based on quantum defects in solid-state materials. Diamond has been the prototypical solid-state material with quantum defects suitable for fabricating quantum magnetometers. We are particularly interested in the feasibility of making magnetometers based on quantum defects in other large bandgap materials that are readily available and could be used for manufacture of magnetometers at scale. Silicon carbide is one such material; it is low-cost and currently serves as platform for a number of important electronic devices that are manufactured at scale.

Quantum magnetometers made from diamond are currently the state of the art in devices based on solid-state media. Although diamond has a number of desirable electronic properties, such as a wide bandgap, which permits room-temperature operation of the magnetometers, it requires specialized tools and processes to fabricate into quantum devices. This presentation will review the essential requirements for solid-state materials suitable for quantum magnetometers. One of the critical requirements for a material for a quantum magnetometer is an ability to host paramagnetic defect states that are long-lived. Depending on the usage mode of the magnetometer, either the magneto-optical or magneto-electrical properties of the solid-state material may play a critical role.

Gyoujin Cho
Professor | Sungkyunkwan University

| Biography

Prof. Cho has been a professor at the Department of Biophysics in the Institute of Quantum Biophysics, Sungkyunkwan University, since September of 2019 and served as the director of the Engineering Research Center for Developing Flexible Computers from 2020 and as a vice director of the Institute of Quantum Biophysics from 2021. He attained his Ph D. from the University of Oklahoma in 1995 and started his academic career at Sunchon National University, Korea, in 1996 as an assistant professor and began the World Class University in Printed Electronics in 2008. He was a visiting project engineer at EECS, UC Berkeley, from 2013 to 2016 and a visiting professor of the Materials and Construction Lab, Tokyo Institute of Technology, in 2013. His research has been focused on roll-to-roll (R2R) printing foundry to fabricate flexible electronic devices and biochips without emitting hazardous byproducts and using industrial water during the last 20 years. He has served as an executive editorial board member of Flexible and Printed Electronics, IOP, since 2013, and served as the president of Korea Flexible and Printed Electronics Association in 2024. His research was introduced in Nature 2010, MIT Technology Review on March 24th, 2010, BBC News Technology on Aug. 13th, 2012, NHK on January 1st, 2013, YTN Science Today on June 24th, 2021. Recently, he reported the world's first R2R printed plasmonic mini-rectors to run rapid photonic PCR (Advanced Science, 10 (28) 2023) and R2R printed 4-bit ALU (npj Flexible Electronics, 78 (8), 2024). His R2R printing foundry is exploring the fabrication of disposable quantum spin biosensors and 2-qubit sticker computers.

Perspective: Way of Sustainable Manufacturing for Disposable Quantum Spin Biosensors and Sticker-Like 2-Qubit Quantum Computers

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| Abstract

After the invention of Intel's 4-bit processor, the Intel 4004, there has been an unprecedented rise in silicon chips that has contributed to global warming, overwhelming heavy industries. Therefore, when innovative technologies are developed, it is crucial to consider environmentally friendly manufacturing methods to sustain the Earth. In this presentation, a sustainable manufacturing method will be introduced for fabricating a disposable quantum spin-based biosensor (QS-Bs) and a sticker-like quantum computer with 2 qubits (2-Qt SQC). To produce both QS-Bs and 2-Qt SQC without emitting hazardous byproducts, a typical additive manufacturing method using printing technology will be optimal, provided that a spin probe material with a long coherence time under ambient conditions can be formulated into an ink. Accordingly, a 1-D spin probe material (single-walled carbon nanotube: SWCNT)-based ink will be introduced and characterized by EPR spectroscopy, and a method for printing QS-Bs and 2-Qt SQC will be presented to demonstrate how the printed QS-Bs can monitor a single molecule in biofluid in real time and how the printed 2-Qt SQC operates.

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Darmindra Arumugam

Ph.D. | Jet Propulsion Laboratory, California Institute of Technology

| Biography

Dr. Darmindra Arumugam is a senior research technologist at NASA's Jet Propulsion Laboratory (JPL), California Institute of Technology, where he leads efforts in atomic sensors for remote sensing, applied physics, and novel sensor systems. He serves as the technical group supervisor for the Radar Concepts and Formulation Group at JPL, overseeing development of advanced sensing architectures across radar and electromagnetic domains. Dr. Arumugam received his Ph.D. from Carnegie Mellon University.

His research focuses on quantum and atomic sensor technologies, particularly using Rydberg atoms for electric field sensing across a broad frequency spectrum—from DC to THz. He has led the development of compact, tunable Rydberg-based sensors for airborne platforms and bistatic radar systems using signals of opportunity. Dr. Arumugam is also pioneering the use of dissipative time crystal (DTC) dynamics in Rydberg vapors to realize ultra-sensitive detection of low-frequency electromagnetic fields, targeting the ELF, VLF, and SLF regimes for future applications in subsurface, and geophysical sensing. His work is opening new directions in reconfigurable quantum sensors with applications spanning Earth and Planetary science.

Remote Sensing with Rydberg Atoms

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| Abstract

Rydberg atoms—atoms in highly excited quantum states—are uniquely sensitive to electric fields across a broad frequency spectrum, from kHz to THz. When excited using precisely tuned lasers, these atoms can serve as compact, low-power sensors capable of detecting and analyzing weak electromagnetic signals with high fidelity. Their exceptional sensitivity and spectral tunability arise from controllable interactions between atomic energy levels and the excitation laser fields. These attributes make Rydberg sensors a promising platform for reconfigurable, multi-band electromagnetic detection.

At NASA's Jet Propulsion Laboratory, Dr. Arumugam's team is advancing Rydberg-based remote sensing techniques for Earth science, including bistatic radar using existing satellite transmissions as illumination sources. Applications include soil moisture retrieval through passive reflectometry, using GNSS and communications signals of opportunity to probe land surface properties at high spatiotemporal resolution. In parallel, the team is developing a new class of low-frequency Rydberg sensors based on dissipative time crystal (DTC) dynamics, enabling ultra-sensitive field detection in the ELF, VLF, and SLF bands. These emerging techniques could open new pathways for subsurface sensing, earthquake precursor detection, and space-based monitoring of ultra-weak signals.

This talk will cover the enabling atomic physics, system-level architectures, and recent experimental progress toward deploying Rydberg-enabled remote sensing platforms for both airborne and future spaceborne missions.

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Douglas J. Weber
Professor | Carnegie Mellon University

| Biography

Doug Weber is the Akhtar and Bhutta Professor of Mechanical Engineering and Neuroscience at Carnegie Mellon University. Dr. Weber received a Ph.D. in Bioengineering from Arizona State University and completed post-doctoral training in the Centre for Neuroscience at the University of Alberta. His primary research area is Neural Engineering, combining fundamental neuroscience and medical device engineering to understand the neural basis of sensory perception, motor control, and neuroplasticity and drive the development of neurotechnologies for restoring sensorimotor functions in patients. A founding member of DARPA's Biological Technologies Office, Weber created and managed a portfolio of neurotechnology research programs to support the White House BRAIN initiative, launched by President Obama in 2013. At CMU, he is co-director of the NeuroMechatronics Laboratory, which is a highly multidisciplinary group of students, post-docs and faculty working on projects spanning fundamental and applied studies in animals and translational research in humans. He is also a founder and Chief Technology Officer of Reach Neuro, Inc., a medical device startup developing a novel therapy for restoring arm and hand function for people with chronic hemiplegia post-stroke.

Sensing and Stimulating the Brain to Restore Neurological Function

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| Abstract

Significant advancements in materials and microelectronics over the last decade have enabled clinically relevant technologies that measure and regulate neural signaling in the brain, spinal cord, and peripheral nerves. These technologies provide new capabilities for studying basic mechanisms of information processing and control in the nervous system, while also creating new opportunities for restoring function lost to injury or disease. Neural sensors can also measure the activity of motor neurons to enable direct neural control over prosthetic limbs and assistive technologies. Conversely, these neural interface technologies can stimulate activity in sensory and motor neurons to reanimate paralyzed muscles. Although many of these applications rely currently on devices that must be implanted into the body for precise targeting, ultra-miniaturized devices can be injected through the skin or vascular system to access deep structures without open surgery. This talk will focus on efforts to develop wearable and injectable neural interfaces for restoring or improving motor function in people with paralysis due to stroke, spinal cord injury, ALS, and other neurological disorders.

Yang-Kyu Choi
Distinguished Professor | KAIST, South Korea

| Biography

Yang-Kyu Choi received his B.S. and M.S. degrees from Seoul National University, South Korea, in 1989 and 1991, respectively. He earned his Ph.D. in Electrical Engineering from the University of California, Berkeley, in 2001. He is currently a Distinguished Professor in the School of Electrical Engineering at the Korea Advanced Institute of Science and Technology (KAIST). From January 1991 to July 1997, he worked at SK hynix Co., Ltd., in Gyeonggi-do, Korea, as a process integration engineer, where he was involved in the development of 4M, 16M, 64M, and 256M DRAM technologies. His current research interests include artificial neurons, synapses, and dendrites for neuromorphic computing; multiple-gate MOSFETs; exploratory devices; and unified memory technologies. He has also conducted extensive research on reliability physics and quantum phenomena in nanoscale CMOS devices. Professor Choi received the Sakrison Memorial Award in 2002 for the best dissertation in the Department of Electrical Engineering and Computer Sciences at UC Berkeley. In 2006, he was recognized as Scientist of the Month by the Ministry of Science and Technology of Korea. He has authored or co-authored over 430 journal articles and 132 conference papers, including presentations at the IEEE International Electron Devices Meeting (IEDM) and the VLSI Symposia, and holds more than 30 U.S. patents. He is a full member of the Korean Academy of Science and Technology (KAST) and the National Academy of Engineering of Korea (NAEK), reflecting his distinguished contributions to the fields.

Rethinking Transistor Operation for Oscillating and Spiking Behavior

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| Abstract

A metal-oxide-semiconductor field-effect transistor (MOSFET) typically operates by receiving an input voltage (Iin) and delivering an output current (Vout). However, when a floating body is present within the MOSFET, applying Iin to the drain terminal initiates a series of internal processes: (i) electron-hole pairs are generated through impact ionization, (ii) the generated holes temporarily accumulate in the floating body, reducing the built-in potential barrier (Vbi,S_FB) between the source and the floating body, (iii) this reduction allows more electrons to be injected into the floating body, and (iv) the resulting increase in carrier injection further enhances impact ionization, leading to additional hole accumulation. This sequence forms a positive feedback loop, referred to as the charging process. The positive feedback results in a phenomenon known as the single transistor latch (STL). Once the floating body becomes fully charged and Vbi,S_FB is flattened, the output voltage (VD = Vout) is rapidly generated at the drain terminal, while a spike shaped output current (IS = Iout) is abruptly discharged through the source terminal. This discharging event completes the cycle. The interplay of gradual charging and abrupt discharging produces a sawtooth shaped oscillation in Vout, which persists as long as Iin is applied.

Owing to its inherent leakage current, charge accumulation capability, and sudden discharge behavior, the MOSFET exhibits leaky, integrate, and fire characteristics, respectively. These attributes enable the device to operate in a leaky-integrate-fire (LIF) mode, making it suitable for implementation as an artificial neuron. The LIF behavior has been experimentally demonstrated in MOSFETs fabricated not only on silicon on insulator (SOI) substrates featuring a floating body, but also on bulk silicon substrates, where both spiking and oscillatory behaviors have been observed.

Furthermore, when a charge trapping nitride layer, such as an ONO stack, is employed as the gate dielectric, the MOSFET functions not only as an artificial neuron but also as an artificial synapse. This is due to its multi-level memory characteristics, which enable the modulation and retention of synaptic weights. Since artificial neurons and synapses share an identical physical structure and differ only in their mode of operation, they have been co-integrated on a single plane. This unified platform has been utilized to implement character and pattern recognition tasks using a spiking neural network (SNN).

Rethinking Transistor Operation for Oscillating and Spiking Behavior

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| Abstract

These MOSFET devices, capable of mimicking brain-inspired signal processing, are not only effective as artificial neurons and synapses but also responsive to external stimuli, making them suitable for use as sensory neurons in in-sensor computing applications. This paper presents experimental results that demonstrate the multifunctionality of this homotypic MOSFET structure through a reexamination of its operating principles.

Euisik Yoon
Professor | University of Michigan

| Biography

Euisik Yoon is a professor in the Department of Electrical Engineering and Computer Science at the University of Michigan, Ann Arbor, Michigan. After receiving Ph.D. degree in Electrical Engineering from the University of Michigan, Ann Arbor, he worked for industry including the National Semiconductor Corp. in Santa Clara, CA and Silicon Graphics Inc. in Mountain View, CA before returning to academia (1990-1996). He took faculty positions at Korea Advanced Institute of Science and Technology (KAIST) in Daejon, Korea and the University of Minnesota, Minneapolis, MN, respectively. In 2008, he joined the University of Michigan, Ann Arbor, MI, where he is a Professor. He served as the Director of Solid-State Electronics Laboratory (2011-2015) and the Director of Lurie Nanofabrication Facility (2011-2016) at the University of Michigan. He led the NSF NeuroNex Hub: Multimodal Integrated Neural Technologies (MINT), disseminating neurotechnologies to the research community (2017-2024).

Dr. Yoon is a Fellow of the IEEE and has served on various Technical Program Committees including the IEEE International Electron Device Meeting (IEDM) (2006-2008) and the IEEE International Conference on Micro Electro Mechanical Systems (MEMS) (2006, 2008-2010, 2021). He also served on the IEEE International Solid-State Circuit Conference (ISSCC) program committee (2003-2007) and organized and co-chaired the International Conference for Advanced Neurotechnology (ICAN) (2016-2020). He served as an associate editor for IEEE Solid-State Circuit Letters (2018-2021).

Brain Interface:
Electrophysiology and Optimal Neuromodulation at Cellular Resolution

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| Abstract

The evolution of Michigan neural probe technologies will be reviewed toward scaling up the number of recording sites and adding selective neural modulation capability to enable optogenetic control of neurons at cellular resolution. Multiple neuro-size micro-LEDs (~10 μm) were monolithically integrated on a probe shank to achieve high spatial temporal modulation of neural circuits. Initial prototype optoelectrodes (MiniSTAR) demonstrated independent control of distinct neuron cells ~50 μm apart in the CA1 pyramidal layer of freely-moving mice at 60 nW light power. The number of optical stimulation sites has scaled up to integrate 128 micro-LEDs along with 256 recording sites (HectoSTAR). Recently, 3D origami architecture has been introduced to deploy the optoelectrodes on non-planar surfaces and enable multi-modalities by incorporating the additional sensors to monitor neurotransmitters and temperature of the local brain region and their effects on electrophysiology.

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Dmitri Strukov

Professor, ECE Department | University of California, Santa Barbara

| Biography

Dmitri Strukov is a Professor of Electrical and Computer Engineering at the University of California, Santa Barbara. Prior to joining UCSB, he was a postdoctoral associate at Hewlett-Packard Laboratories, where he worked on various aspects of nanoelectronic devices and systems. He earned an M.S. in Applied Physics and Mathematics from the Moscow Institute of Physics and Technology in 1999, and a Ph.D. in Electrical Engineering from Stony Brook University, New York, in 2006. He is a Fellow of the IEEE.

Professor Strukov's research broadly focuses on various aspects of computation, particularly on how to perform computation efficiently across different levels of abstraction. His work spans multiple disciplines, including materials science, device physics, circuit design, high-level computer architecture, and algorithms, with an emphasis on emerging device technologies. Over the past decade, his primary research has centered on neuromorphic computing. More recently, he has focused on implementing hardware security circuits and accelerators for solving optimization problems using in-memory computing architectures. These architectures leverage both conventional and emerging memory technologies, such as resistive switching devices ("memristors") and embedded floating-gate memory devices.

KLIMA:
K–Local In-Memory Accelerator for Combinatorial Optimization

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| Abstract

Ising machines, along with related models such as Hopfield neural networks and Boltzmann machines, are promising computational paradigms for solving complex optimization problems. Many real-world problems are naturally described by higher-degree polynomial objective functions [1], necessitating the development of efficient high-order Ising machines. However, the hardware implementations of such machines remain limited, largely due to the difficulty of efficiently computing partial derivatives of high-degree functions in a scalable and reconfigurable manner. A common workaround is to convert high-order problems into equivalent quadratic formulations and solve them using conventional second-order Ising machines. However, this transformation incurs significant complexity and latency overheads, including an increased number of variables and slower convergence due to spurious local minima [1,2].

This talk focuses on KLIMA (K–Local In-Memory Accelerator), a comprehensive framework developed by my research group with our DARPA QuICC program collaborators [1-9] to address the above challenges. A central innovation is an approach for the massively parallel gradient computation for high-degree polynomials, which is well-suited to efficient mixed-signal in-memory computing [3,9]. This method enables circuit implementations whose area complexity scales linearly with the number of variables and polynomial terms, independent of the polynomial's degree. We have built experimental KLIMA prototypes using ReRAM [3,8] and SRAM-based [6,7] in-memory computing circuits, and evaluated them on standard satisfiability problem (SAT) benchmarks. These prototypes, along with simulations on larger-scale problems, demonstrate orders-of-magnitude improvements in speed and energy efficiency over state-of-the-art solutions. Finally, I will discuss a higher-level KLIMA architectures [4,5] inspired by island-style field-programmable gate arrays. Such an architecture leverages the high sparsity of coupling matrices found in many practical (hard) problems, enabling solving efficiently SATs with tens of thousands of variables on a single chip.

KLIMA:
K–Local In-Memory Accelerator for Combinatorial Optimization

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Reference

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Seong Jun Kang
Professor | Kyung Hee University

| Biography

Seong Jun Kang received his B.S., M.S. and Ph.D. degrees in Physics from Yonsei University. In 2005, He joined in University of Illinois at Urbana Champaign as a postdoctoral research associate, where he was involved in research of flexible and stretchable electronic devices based on carbon nanomaterials. In 2007, he joined Korea Research Institute of Standards and Science as a research scientist. From 2010, he joined to the Department of Materials Science and Engineering at Kyung Hee University. He also worked at Columbia University (New York) in 2016. His research interests focused on emerging optoelectronics based on oxide semiconductors and nanomaterials. Also, he focused on the study of interfacial electronic structures between nanomaterials for the high-performance optoelectronics. Additional information of Prof. Kang can be found at his webpage of http://lant.khu.ac.kr.

Band structure of oxide semiconductors for optical neuromorphic devices to realize highly efficient and accurate machine vision

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| Abstract

IThis talk will focus to introduce a new type of optoelectronics based on oxide semiconductors for advancing machine vision technology. In-sensor computing systems based on optical neuromorphic devices have attracted increasing attention to improve the efficiency and accuracy of machine vision systems. However, most materials used in optical neuromorphic devices exhibit spike-timing-dependent plasticity (STDP) behavior in response to input light signals, leading to complex in-sensor computing and reduced machine vision accuracy. To address this issue, we introduce a novel band structure of oxide semiconductor designed to enhance spike-number-dependent plasticity (SNDP) in response to input light signals while eliminating STDP behavior. As a result, in-sensor computing with the SNDP-enhanced device reduces multi-layer perceptron (MLP) training time by 87.7 % while achieving high classification accuracy. This study demonstrates that in-sensor computing systems with SNDP characteristics in optical neuromorphic devices have significant potential to accelerate machine learning for highly efficient machine vision systems.

Reference

[1] Min Ho Park, Yeojin Kim, Min Jung Choi, Yu Bin Kim, Jung Min Yun, Jun Hyung Jeong, Seunghwan Kim, Soohyung Park, Seong Jun Kang, ACS Nano, 19, 13107 (2025).

Bruce Gnade
Emeritus Professor | The University of Texas at Dallas

| Biography

Bruce Gnade received his BA in Chemistry from St. Louis University in 1976 and his Ph.D. in Nuclear Chemistry from the Georgia Institute of Technology in 1982. He is Professor Emeritus at UT Dallas and Chief Scientist at Mustang Optics. He was the Executive Director of the Hart Center for Engineering Leadership in the Lyle School of Engineering at SMU from 2017-2022, the Vice President for Research and the Distinguished Chair in Microelectronics at UT Dallas from 2006-2016, and a program manager in the Microsystems Technology Office at the Defense Advanced Research Projects Agency (DARPA) from 1996-1999. At Texas Instruments he led several research and technology groups from 1982-1996. His current research interests focus on electronics for harsh environments and using optical techniques to solve problems. He is a Fellow of APS, IEEE, and National Academy of Inventors, and was Chair of the Board of Directors of Oak Ridge Associated Universities from 2021-2023. He was awarded the IEEE J.J. Ebers award in 2021. He has authored or co-authored > 200 refereed journal papers, 79 U.S. and 55 foreign patents.

Neuromorphic Sensors for Anomaly Detection

Bruce Gnade[1], Danyal Ahsanullah[2], Prasanna Rangarajan[3]

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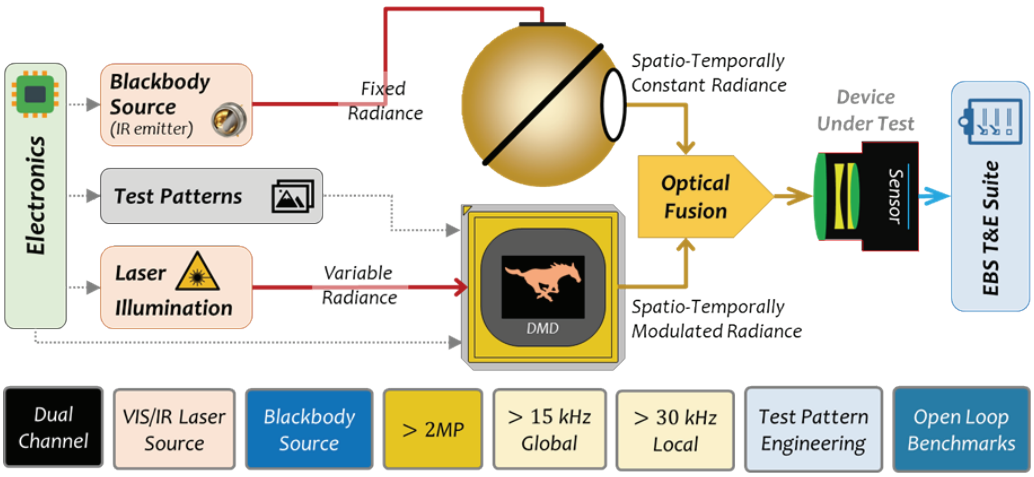
| Abstract

Neuromorphic sensors, commonly referred to as event based cameras, respond only to changes in stimuli as they occur. They have the potential benefits of higher dynamic range and higher effective frame rates, relative to traditional framing sensors. This is possible because in an event based camera a pixel only outputs data when a stimulus occurs at that pixel. The output is the x and y position of the pixel, the time stamp for when the event occurred, and whether or not the intensity increased or decreased, essentially a time stamped spike train. The stimulus can be either an increase or a decrease in intensity. Neuromorphic sensors have found uses for applications ranging from temporal anomaly detection to autonomous driving. In order to characterize the performance characteristics of event cameras, we have developed a task specific hardware-in-the-loop testing system shown schematically in the figure below. In this presentation we will discuss the test system, as well as the measurement of the temporal and spatial response of a neuromorphic sensor.



Poster Session

Co-chairs

Jo-won Lee / Myung S. Jhon

Hongseok Oh

Professor | Soongsil University

| Biography

Dr. Hongseok Oh is an Assistant Professor in the Department of Physics at Soongsil University, specializing in semiconductor device physics, nanomaterials, and neuromorphic devices. He received his Ph.D. from Seoul National University, focusing on hybrid nanomaterials for flexible electronic and optoelectronic devices. He subsequently conducted postdoctoral research at UC San Diego, where he contributed to the development of high-resolution tactile sensor arrays for robotic applications.

His group at Soongsil explores energy-efficient computing and sensing devices based on novel findings in device physics. The group aims to uncover new physical principles at the intersection of semiconductor materials, light–matter interaction, and information processing. To date, he has published over 40 peer-reviewed papers in journals including Science Advances, ACS Nano, and Small. He has served as an Editorial Board Member of Scientific Reports since 2024 and actively contributes as a committee member to major international conferences, including Nano Korea.

Te Photonic Synapses for Physical Reservoir Computing

Hongseok Oh

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| Abstract

Physical reservoir computing (PRC) is a new computing framework for energy-efficient machine learning, especially for processing time-series data. Usually, such data is processed using a recurrent neural network (RNN)-based approach, which is powerful but computationally intensive. An alternative approach is reservoir computing (RC). In RC, a reservoir—a set of fixed, randomly connected perceptrons—is driven by the input signal, and only the connections between its readout nodes and output nodes are trained. This approach can significantly reduce computational costs while maintaining comparable or superior performance in learning dynamical systems.[1]

PRC is similar to RC but replaces the digital reservoir with a physical system. Here, the reservoir requires no computational cost during operation, ultimately enabling energy-efficient AI. Any nonlinear physical system with fading memory can serve as a PRC reservoir, including electronic circuits, mechanical systems, and even water surfaces. [2] Recently, PRC systems based on one or a few (opto)electronic devices exhibiting a fading memory effect—where the latest signal contributes most to the device state—have emerged as practical solutions due to their simplicity and compatibility with existing electronics.[3]

In this presentation, we introduce our research progress on PRC utilizing artificial synaptic devices, including tellurium thin-film-based photonic synapses.[4] Our system demonstrated strong performance in tasks such as classification of grayscale handwritten digits and prediction of nonlinear dynamical equations. We also investigate the device physics underlying nonlinear and fading memory characteristics. Our research can enable energy-efficient AI for learning and processing dynamic systems, such as speech, motion, and biological signals.

Reference

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Mikael P. Backlund

Professor | University of Illinois at Urbana-Champaign

| Biography

Mikael Backlund earned his B.S. from the University of California, Berkeley in 2010 and his Ph.D. from Stanford University in 2016, where he worked in the lab of W. E. Moerner as a Robert and Marvel Kirby Stanford Graduate Fellow. From 2016 to 2020 he was a postdoctoral fellow at the Harvard-Smithsonian Center for Astrophysics under the advisement of Ron Walsworth. In 2020 he started as an assistant professor in the Department of Chemistry at the University of Illinois at Urbana-Champaign, where he is also a member of the Illinois Quantum Information Science and Technology Center (IQUIST), the Center for Biophysics and Quantitative Biology, and the NSF Science and Technology Center for Quantitative Cell Biology. Recent awards and honors include the Spectroscopy Society of Pittsburgh Starter Grant Award, a National Academy of Sciences Kavli Fellowship, the Arnold and Mabel Beckman Young Investigator Award, and the National Science Foundation CAREER Award

Quantum and Quantum-Inspired Microscopy of Molecules and Materials

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| Abstract

Quantum resources like superposition and entanglement can be leveraged to realize sensing capabilities beyond what is possible with wholly classical sensors [1, 2]. One promising application space for quantum sensing is the imaging and spectroscopy of molecules and materials at the nanoscale. In this talk I will present my group's recent work on the development of methods to this end.

First, I will discuss our recent progress on magnetic resonance microscopy using nitrogen-vacancy (NV) centers in diamond. Shallow-implanted NVs are in principle capable of sensing magnetic signals emanating from single nuclear spins embedded in target molecules brought to the surface of the diamond. Direct single-molecule NMR would require NVs placed within a few nanometers of the target. However, when the NV is too shallow it's coherence properties and charge stability break down. To bridge the gap others have suggested the use of reporter electronic spins located external to the diamond that can couple directly to nuclei of interest and in turn relay information to NVs embedded somewhat deeper in the diamond [3]. In our work we repurpose a commonly used class of fluorescent dyes which form stable radical ions under the right buffer conditions. These photoswitchable reporter spins will enable new approaches to correlative fluorescence and magnetic resonance imaging.

Next I will describe our work aimed at placing optical nanoscopy of molecules in the context of quantum metrology. This facilitates comparison of experimental performance to the fundamental, measurement-independent precision bounds set by quantum mechanics. When these bounds are saturated, no amount of microscope engineering can improve the performance. When these bounds are not saturated, the development of new microscopy methods is warranted. Specifically I will discuss the age-old problem of optical resolution in this context, and show that our recently constructed vortex-polarized image inversion interferometer can greatly surpass direct imaging for the task of resolving a pair of fluorescent point emitters [4].

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Guesuk Lee
Senior Research Engineer | Korea Electronics Technology Institute

| Biography

Dr. Guesuk Lee received his Ph.D. in Mechanical and Aerospace Engineering from Seoul National University, Republic of Korea, where his doctoral research focused on optimization-based statistical model calibration.

He began his professional career at the Semiconductor R&D Center of Samsung Electronics, where he worked as a staff engineer. At Samsung, he specialized in diagnosing and resolving process and equipment failures in semiconductor manufacturing. This role provided him with in-depth experience in high-volume production environments and strengthened his understanding of reliability engineering and failure mechanisms in advanced semiconductor processes.

Building upon this industrial foundation, Dr. Lee is currently a senior research engineer at the Korea Electronics Technology Institute (KETI), where he leads research at the Reliability Research Center. His work encompasses advanced semiconductor packaging, automotive and power semiconductors, and battery reliability. He focuses on hybrid bonding reliability evaluation, multi-temperature warpage measurement, and structure-function-based thermal diagnostics. His recent work integrates AI-driven modeling for degradation prediction and condition monitoring of next-generation electronic components.

Dr. Lee is actively involved in international joint research with institutions in the United States and Germany, targeting measurement-based mechanical, thermal, and electrical evaluation methods for 3D multichip structures. These collaborations aim to establish robust reliability assessment frameworks for highly integrated semiconductor systems. In addition to his research and project leadership, Dr. Lee contributes to global standardization through IEC and JEDEC working groups on hybrid bonding and packaging reliability. Domestically, he serves as a board member of the Korean Society of Prognostics and Health Management (KSPHM) and the Korean Microelectronics and Packaging Society (KMEPS), where he promotes technical advancement and interdisciplinary collaboration in the fields of semiconductor reliability and packaging.

Thermoreflectance-Based Submicron Temperature Profiling and Structure Function Analysis for Multilayer Nanostructures

Guesuk Lee

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| Abstract

Recent advances in nanoscale semiconductor packaging and interconnect technology have led to increasing demands for high-resolution thermal metrology and internal structure analysis techniques. This study proposes an integrated methodology combining thermoreflectance (TR) imaging-based submicron temperature measurement with structure function analysis to extract internal thermal properties of multilayer structures.

Thermoreflectance techniques enable non-contact, optical temperature measurements with spatial resolutions below 1 μm by monitoring changes in the reflectivity of the material surface as a function of temperature. This allows for the capture of localized hotspots and thermal gradients across advanced interposer and redistribution layer (RDL) configurations. However, to fully understand heat conduction paths and material interfaces, temperature profiles alone are insufficient.

To address this, the transient thermal responses acquired from TR imaging were further analyzed using the structure function method. This approach deconvolutes thermal impedance into cumulative thermal resistance and capacitance, enabling the identification of thermal interface layers, defects, and material boundaries in complex 2.5D/3D IC packaging. Experimental results on silicon-based multilayer samples demonstrate that the combined methodology can not only visualize surface temperature profiles but also reconstruct internal thermal architecture with high fidelity.

This hybrid technique is expected to contribute significantly to the thermal design and reliability evaluation of next-generation power and AI semiconductor packages, especially where conventional measurement techniques are limited in resolution or invasiveness.

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Robert Nawrocki
Assistant Professor. | Purdue University, USA

| Biography

Dr. Robert A Nawrocki is an Assistant Professor in the School of Engineering Technology (SOET) at Purdue University. He is a recipient of the 2021 Office of Naval Research, Young Investigator Award and the 2021 Ralph W. and Grace M. Showalter Research Trust Award. His current research interests include physically flexible organic electronics with the application in biopotential monitoring and soft robotics, as well as neuromorphic systems, chemical sensors, smart (meta) materials and neuroscience. He completed his BS at New Jersey Institute of Technology (2004), PhD at University of Denver (2014), his internship at Eidgenössische Technische Hochschule Zürich, Switzerland (ETH) (2011), and his postdoctoral research at University of Colorado Boulder (2014), University of Nova Gorica, Slovenia (2015), and The University of Tokyo, Japan (2017).

Organic Spiking Neuromorphic Circuits:
Flexible Embodied AI

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2. Chemical Engineering, Stanford University, Stanford, CA, USA
3. Department of Mechanical and Automation Engineering, The Chinese University of Hong Kong, China
4. Event-Driven Perception for Robotics, Italian Institute of Technology, Genoa, Italy
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| Abstract

Artificial neurons are key components of neuromorphic computing systems, which aim to emulate the structure and functions of biological neural networks for efficient, brain-like computation. However, most artificial neurons rely on rigid, silicon-based technologies that are poorly suited for integration with soft structures, such as soft robots or biological systems, due to limitations in mechanical flexibility. Our aim is to develop networks of artificial spiking neurons, implemented using physically flexible organic electronics, to perform pattern recognition, processing of input/output data, and control of mechanical actuators. We have fabricated an electrical circuit that approximates the behavior of an Integrate-and-Fire (I&F) spiking neuron based on the Axon-Hillock model.1 Utilizing complimentary p- and n-type organic transistor, the circuit integrates synaptic input current and produces output voltage spikes of a proportional frequency. We showed it encoding an analog concentration of an analyte of a chemical sensor into the frequency of output voltage spikes.2 We verified that a somatic circuit is capable of generating tonic spikes enabling deep brain stimulation for altering the effects of neurological conditions, such as Parkinson's Disease.3 We demonstrated physically flexible organic Log-Domain Integrator and Differential-Pair Integrator synaptic circuits.4-5 Synapses, which convert input voltage spikes into output current traces, were characterized to demonstrate the effects of various synaptic parameters, including gain and weighting voltage, synaptic capacitance, and circuit response to inputs of various voltage spike frequencies. Time constants comparable to biological synapses, critical in processing real-world sensory signals were also shown. Furthermore, we reported the first organic spiking neuron fit with excitatory and inhibitory synapses and I&F soma. The circuit emulates key neural functions including pre-synaptic signal integration, frequency modulation, adjustable synaptic weighting, and coincidence detection. The neuron can interact with the real world in a light-control feedback loop that adjusts luminance based on ambient light intensity.

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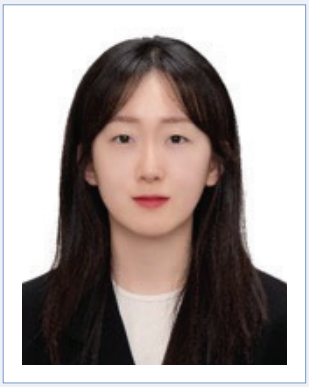

Hyunjeong Kwak
Dr. | POSTECH, South Korea

| Biography

Hyunjeong Kwak is a postdoctoral researcher in the Department of Materials Science and Engineering at Pohang University of Science and Technology (POSTECH), South Korea. She received her Ph.D. from POSTECH under the supervision of Professor Seyoung Kim, where her research focused on analog artificial intelligence (AI) hardware based on electrochemical random-access memory (ECRAM).

Her academic work bridges material-level innovation and system-level implementation. During her doctoral and postdoctoral research, she developed novel ECRAM devices and demonstrated their application in analog AI accelerators. Notably, she led the development of the first monolithically integrated 4K ECRAM-based analog AI chip with in-situ training capability, demonstrating energy efficiency of up to 6.17 TOPS/W. Her work contributes to closing the gap between memory device physics and full-stack neuromorphic computing.

Hyunjeong has authored over ten publications and patents spanning from materials characterization to chip-level AI acceleration. She also completed a research internship at IBM T.J. Watson Research Center, where she worked on resistive memory-based computing for AI training and conducted Hall measurements to analyze device-level transport phenomena.

Her research interests include neuromorphic hardware, in-memory computing, materials for energy-efficient AI, and sensor-integrated learning systems. She is particularly interested in bridging physical computing with real-world AI applications at the edge.

Monolithic 4K Electrochemical RAM-Based Analog AI Chip for Energy-Efficient On-Chip Training

Hyunjeong Kwak
Dr. | POSTECH, South Korea

| Abstract

The rapid advancement of artificial intelligence (AI) has led to an exponential increase in computational demand. However, Moore's Law, which has guided performance improvements in conventional computing for decades, is no longer sufficient to sustain this growth. There is a pressing need for high-performance, energy-efficient AI hardware to overcome the limitations of traditional systems.

Analog AI hardware based on resistive memory arrays has emerged as a promising candidate, offering in-memory vector-matrix multiplication (VMM) with enhanced parallelism and power efficiency. Yet, real-world implementations have faced gaps between theoretical expectations and experimental results due to device nonidealities, variability, and noise.

Electrochemical random-access memory (ECRAM) devices are well suited for analog AI hardware due to their ion-driven, stable conductance modulation and inherently low cycle-to-cycle and device-to-device variation. In this talk, we present a monolithically integrated analog AI chip comprising 4,096 ECRAM devices fabricated atop CMOS peripheral circuits using a back-end-of-line (BEOL)-compatible low-temperature process (< 200°C). This architecture enables scalable and energy-efficient in-memory computing.

The fabricated chip achieves a low total power consumption of 11.08 mW and a peak system-level energy efficiency of 6.17 TOPS/W. Our ECRAM devices demonstrate symmetric and linear conductance updates, robust endurance over 80,000 cycles, and stable selector-free operation across the entire 4K array.

Most notably, we experimentally demonstrate the world's largest in-situ neural network training using a selector-free resistive memory cross-point array. A total of 441 functional devices are used to perform VMM operations and stochastic outer-product updates without the need for external computation. This result demonstrates meaningful progress toward realizing practical neuromorphic computing hardware.

By integrating material engineering, circuit design, and algorithm co-optimization, this work establishes a scalable and energy-efficient hardware platform for analog AI and neuromorphic computing. Furthermore, the monolithic integration scheme is readily extendable to sensor-interfaced systems, paving the way for future on-chip intelligence in neuromorphic sensing applications.

Youjin Reo
Dr. | Pohang University of Science and Technology

| Biography

Dr. Youjin Reo received her Ph.D. in Chemical Engineering in Pohang University of Science and Technology (POSTECH), Korea in 2024 for her research on tin-based hybrid and inorganic perovskite electronic materials and devices using thermal evaporation and solution processing. She has published over 32 SCI(E) papers with approximately 820 citations and an h-index of 14. A key achievement was developing the world's highest-performing p-type tin-based perovskite transistor via thermal evaporation, along with identifying a novel thermally induced reaction mechanism. This work was published in Nature Electronics (Nat. Electron. 8, 403-410 (2025)) and earned her major honors, including awards from the Gordon Research Conference (GRC), the International Meeting in Information Display (IMID), and the International Conference in Molecular Electronics & Devices (ICME&D).

In addition to her primary research, Dr. Reo made significant contributions as a co-author on projects applying semiconductors such as perovskites, metal halides, chalcogenides, and oxides to devices like transistors, phototransistors, and integrated circuits. These efforts led to high-impact publications in Nature and Nature Electronics. Her research was also recognized in the Ministry of Science and ICT's "Top 100 Outstanding National R&D Achievements" for two consecutive years (2023, 2024).

During her doctoral studies, Dr. Reo was selected for a Ministry of Education fellowship supporting independent research on new perovskite synthesis and high-performance thin-film transistors. She is currently a postdoctoral researcher at POSTECH, where she was awarded the PIURI Postdoctoral Fellowship. Her work lays the foundation for next-generation electronics, with strong potential impact on display circuits, wearable devices, and vertically integrated systems.

Vapour-Deposited High-Performance Tin Halide Perovskite Transistors

Youjin Reo[1], Taoyu Zou[1], Taesu Choi[1], Soonhyo Kim[1], Ji-Young Go[1], Taewan Roh[1], Hyoungha Ryu[1], Yong-Sung Kim[2], Huihui Zhu[3], Ao Liu[4] and Yong-Young Noh[1]*

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| Abstract

Solution-processed tin (Sn2+)-halide perovskites can be used to create p-channel thin-film transistors (TFTs) with performance levels comparable with commercial low-temperature polysilicon technology.[1-3] However, high-quality perovskite film deposition using industry-compatible production techniques remains challenging. Here we report the fabrication of p-channel Sn2+-halide perovskite TFTs using a thermal evaporation approach with inorganic caesium tin iodide (CsSnI3).[4] We use lead chloride (PbCl2) as a reaction initiator that triggers solid-state reactions of the as-evaporated perovskite compounds. This promotes the conversion of dense and uniform perovskite films, and also modulates the intrinsically high hole density of the CsSnI3 perovskite channels. Our optimized TFTs exhibit average hole field-effect mobilities of around 33.8 cm2 V−1 s−1, on/off current ratios of around 108, and large-area fabrication uniformity. The devices also exhibit improved stability compared with solution-deposited devices.

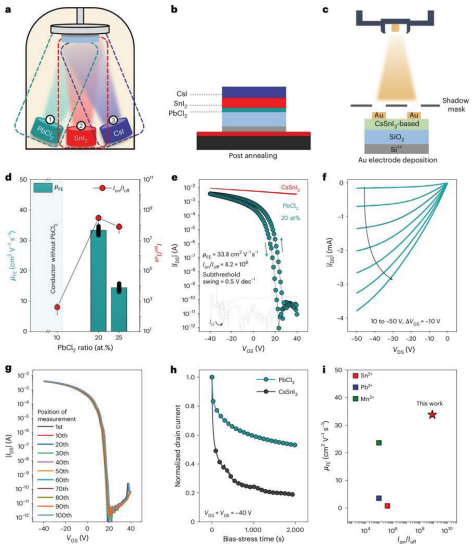

Fig. 1. Electrical characterisations of vapour-deposited CsSnI3-based TFTs.

Vapour-Deposited High-Performance Tin Halide Perovskite Transistors

Youjin Reo[1], Taoyu Zou[1], Taesu Choi[1], Soonhyo Kim[1], Ji-Young Go[1], Taewan Roh[1], Hyoungha Ryu[1], Yong-Sung Kim[2], Huihui Zhu[3], Ao Liu[4] and Yong-Young Noh[1]*

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Acknowledgement

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Matthew T. Flavin
Assistant Professor | Georgia Institute of Technology

| Biography

Prof. Matthew Flavin is an assistant professor in the School of Electrical and Computer Engineering at the Georgia Institute of Technology where he leads the Flavin Neuromachines Lab. Before joining the faculty at Georgia Tech, he was a postdoctoral researcher at Northwestern University. He received his M.S. and Ph.D. degrees in Electrical Engineering in 2017 and 2021 from the Massachusetts Institute of Technology (MIT), and he received his B.S. in Electrical Engineering in 2015 from the University of Illinois at Urbana-Champaign (UIUC). He received the NIH Ruth L. Kirschstein Institutional National Research Service Award (T32) and the Draper Laboratory Fellowship. The vision for his independent research program is to develop powerful peripheral neural interfaces and mechatronic wearables that leverage advanced sensors and intelligent systems to address important and unresolved challenges in patient care.

Wearable Mechatronics for Receiving and Transmitting Information Through the Skin

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| Abstract

The rich set of mechanoreceptors found in human skin offers a versatile engineering interface for transmitting information and eliciting perceptions, potentially serving a broad range of applications in patient care. Targeted multisensory engagement of these afferent units, however, faces persistent challenges, especially for wearable, programmable systems that need to operate adaptively across the body. We present a miniaturized electromechanical structure that, when combined with skin as an elastic, energy storing element, supports bistable, self-sensing modes of deformation. Targeting specific classes of mechanoreceptors as the basis for distinct, programmed sensory responses, this haptic unit can deliver both dynamic and static stimuli, directed as either normal or shear forces. A wireless, skin-conformable haptic interface, integrating an array of these bistable transducers, serves as a high-density channel capable of rendering input from smartphone-based 3D scanning and inertial sensors. Demonstrations of this system include clinical trials for patients with stroke and spinal cord injury [1,2].

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Jaeduk Han
Prof. | Hanyang University

| Biography

Jaeduk Han is an Assistant Professor of Electronic Engineering at Hanyang University. He received his B.S. and M.S. degrees in Electrical Engineering from Seoul National University, Seoul, Korea, in 2007, and 2009, respectively, and his Ph.D. degree in Electrical Engineering and Computer Sciences from the University of California at Berkeley, CA, USA, in 2017. He has held various full-time, part-time, and advisory positions at TLI, Altera, Intel, Xilinx, Apple, LG Innotek, and SK Hynix, where he worked on digital, analog, and mixed-signal integrated circuit designs and design automations. His research interests include high-speed analog and mixed-signal (AMS) circuit design and automation.

Design and Generation of High-Performance Transceivers

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| Abstract

In the AI-driven era, high-performance communication circuits must support extremely high data throughput, demanding over 100 Gb/s per channel. To address these challenges, we present two key research items: high-speed transceiver design and automated custom layout generation.

First, we developed a PAM-8 based transceiver architecture capable of transmitting 3 bits per symbol. A carefully engineered multi-path receiver chain ensures robust signal recovery and high fidelity, enabling the highest mixed-signal PAM-8 data rate reported to date. This design addresses both bandwidth and signal integrity challenges inherent in modern AI SoC environments.

Second, we introduce LAYGO, a layout generation framework that leverages a template-and-grid methodology to significantly reduce manual effort and design complexity. The framework has been successfully applied to advanced semiconductor platforms including sub-7nm FinFETs, DRAM, and CMOS image sensors, achieving over 5x productivity improvement. Its modular design supports rapid adaptation to various circuit topologies and design rules.

We are now actively extending this framework through the integration of artificial intelligence and large language models (LLMs), aiming to further automate layout tasks and improve design quality. This research is being conducted in close collaboration with industry partners, ensuring both academic innovation and practical relevance.

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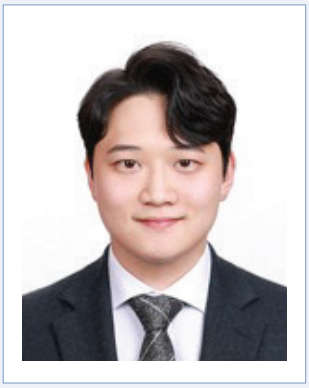

Jung-Hoon Lee
Dr. | Korea Research Institute of Chemical Technology

| Biography

Dr. Jung-Hoon Lee is a materials scientist specializing in thin film deposition technologies, particularly Atomic Layer Deposition (ALD) with strong expertise in the fields of oxide semiconductors, metal thin films, and display/semiconductor device fabrication. He received his B.S. and Ph.D. degrees in Materials Science and Engineering from Hanyang University, Korea, where his doctoral research focused on the development of p-type oxide semiconductors and their integration into Thin-Film Transistors (TFTs) via ALD.

Following his academic training, Dr. Lee gained extensive industrial experience. At Isac Research, he led efforts in ALD/PEALD equipment development, novel precursor engineering, and passivation layers for Micro-LED/OLED applications. During his tenure at Samsung Display, he played a key role in process architecture design for next-generation OLED panels, focusing on oxide semiconductor TFTs and device reliability. Since 2023, he has served as a Senior Researcher at Korea Research Institute of Chemical Technology (KRICT), where he is engaged in novel precursor assessment and development for both ALD and MO-CVD processes, enabling advanced device applications in the semiconductor industry.

With his unique combination of fundamental research expertise and industrial insight, Dr. Lee is actively contributing to the advancement of next-generation electronic materials and devices, particularly at the intersection of semiconductor process innovation and display technology evolution.

Synthesis of a Tin Compound Bearing N-alkoxy Carboxamide and Methyl Ligands as a Precursor for SnO2 Fabrication via Atomic Layer Deposition

Sol-Hee Jo[1a,b], Sunyoung Shin[1a], Minhyeok An[a], Youngkwon Kim[a], Donghwi Cho[a,c], Jeong-O Lee[a], Ji Yeon Ryu[a], Bo Keun Park[a,c], Chang Gyoun Kim[a]*, Jinseong Park[b]*, Jung-Hoon Lee[a]*

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c. Department of Chemical Convergence Materials, University of Science and Technology, 217, Gajeong-Ro, Yuseong-Gu, Daejeon 34113, Republic of Korea

| Abstract

We synthesized a novel tin precursor and deposited SnO2 thin films to demonstrate their excellent applicability in gas-sensor technology. The novel SnMe3(EDPA) (EDPA, N-ethoxy-2,2-dimethylcarboxylicpropanamide) precursor was analyzed using thermogravimetric analysis (TGA), which revealed complete mass loss at 155 °C with negligible residue. The temperature of SnMe3(EDPA) under 1 Torr vapor pressure was 25 °C. We successfully deposited tin oxide via atomic layer deposition (ALD) using SnMe3(EDPA) and O2 plasma as reactants. The film growth behavior of SnO2 thin films deposited via the ALD process exhibited typical surface-limited reaction characteristics and a crystal structure of tetragonal tin dioxide. The films had an optical bandgap of 3.5–3.6 eV and a refractive index of ~1.9, which is a typical optical property of SnO2. Further, we confirmed that there were almost no impurities and that it was an n-type material. Consequently, our experimental results showed that the SnMe3(EDPA) precursor is suitable for the ALD process. The chemical sensing experiments demonstrated the superiority of films deposited using the novel precursor, which significantly exceeded the performances reported in previous studies.

Inhee Lee
Assistant Professor | University of Pittsburgh

| Biography

Inhee Lee is an assistant professor in the Electrical and Computer Engineering department at the University of Pittsburgh. Inhee Lee received his B.S. and M.S. degrees in electrical and electronic engineering from Yonsei University, South Korea, in 2006 and 2008, respectively, and a Ph.D. degree in electrical engineering from the University of Michigan in 2014. He was an assistant research scientist at the University of Michigan from 2015 to 2019. Currently, he is leading PITT Circuit Lab developing adaptive, energy-efficient reference circuits, sensor interfaces, energy harvesters, power management circuits, machine learning accelerators, emerging memory interfaces, and Cryogenic-CMOS circuits. Also, he is developing low-power millimeter-scale or even smaller sensing/computing systems for ecological, biomedical, energy exploration, and internet-of-things applications. Dr. Lee is an IEEE senior member and has been serving as a Technical Program Committee (TPC) Member for IEEE Symposium on VLSI Technology and Circuits (VLSI), IEEE Custom Integrated Circuits Conference (CICC), IEEE Asian Solid-State Circuits Conference (ASSCC), IEEE Circuits & Systems (CAS) Analog Signal Processing Technical Committee (ASPTC) and ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED).

Millimeter-Scale Neuromorphic Vision System

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| Abstract

Millimeter-scale sensing semiconductor devices offer a unique combination of features, including wireless communication, energy harvesting, and ultra-compact form factors. These capabilities enable non-invasive and secure deployment in next-generation Internet-of-Things (IoT) applications across biomedical, ecological, surveillance, and infrastructure domains. Significant progress in miniaturization has advanced the vision of “smart dust” at the millimeter scale [1]. Meanwhile, emerging artificial intelligence (AI) technologies are enhancing the intelligence, accuracy, and reliability of traditional sensing systems. Motivated by these advances, I am investigating how to integrate advanced machine learning (ML) techniques to further expand the capabilities of millimeter-scale sensing platforms.

In this talk, I will highlight the key challenges involved in developing ultra-small sensing systems and introduce a millimeter-scale platform recognized as the world’s smallest computer. I will also present recent research advances in digital circuit design for implementing Dynamic Neural Fields (DNF) [2] and Convolutional Neural Networks (CNN), enabling bio-inspired dynamic vision sensing (DVS) for low-power object classification and motion tracking.

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Sung Beom Cho
Professor | Ajou University

| Biography

Sung Beom Cho is an Assistant Professor at Ajou University, where he is establishing a research program in computational materials science and materials informatics. He earned his Ph.D. from Hanyang University in 2017 and completed postdoctoral research at Washington University in St. Louis from 2017 to 2018. Dr. Cho specializes in multi-scale simulations, incorporating Density Functional Theory (DFT), Molecular Dynamics (MD), and Finite Element Method (FEM), with expertise in thermodynamics. His research focuses on integrating these methodologies with machine learning for advanced materials and process design. Dr. Cho's interests also extend to polymorph control in solid-phase epitaxy, instrument design, and recipe engineering for various materials.

Multiscale Simulation and AI-Driven Approaches for Comprehensive Understanding of Advanced Materials and Semiconductor Processing

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| Abstract

Computational modeling is now indispensable to materials science and semiconductor manufacturing, yet standard techniques—Density Functional Theory (DFT), Molecular Dynamics (MD), the Finite Element Method (FEM), and Technology Computer-Aided Design (TCAD)—operate on isolated time and length scales. Each excels within its niche but inevitably omits critical physics that emerge when atomic reactions, mesoscale microstructures, and device-level fields interact. These blind spots, amplified by numerical instability and physical complexity, restrict our ability to predict real process–structure–property relationships. We demonstrate that coupling multiscale simulations with AI-driven data curation overcomes these limitations and yields a cohesive description of material behavior, processing conditions, and device performance.

The talk focuses on chemical-vapor-deposited Ga_2O_3, a wide-band-gap semiconductor whose five polymorphs and diverse out-of-plane orientations challenge process control. Multiphysics FEM reveals how carrier-gas flow, precursor depletion, and thermal gradients develop inside commercial CVD reactors, but it cannot capture the surface chemistry governing which phase nucleates. By embedding Classical Nucleation Theory informed by DFT-computed surface energies, adsorption barriers, and cluster stabilities into the FEM solution, we predict local nucleation rates and explain why specific polymorphs dominate under given precursor partial pressures and substrate temperatures. MD simulations, accelerated by machine-learning interatomic potentials trained on DFT data, extend the analysis to lateral growth fronts, resolving defect incorporation, strain relaxation, and orientation competition in real time. By orchestrating DFT, MD, nucleation theory, FEM, TCAD, and AI within one framework, this study charts a path toward predictive, adaptive process design for complex semiconductors and other multicomponent materials.

Dong-Woo Jee
Professor | Ajou University

| Biography

Dong-Woo Jee received the B.S., M.S., and Ph.D. degrees in electronic and electrical engineering from Pohang University of Science and Technology (POSTECH), Korea, in 2006, 2009, and 2013, respectively. From 2011 to 2012, he was a Visiting Researcher with the University of Michigan, Ann Arbor, MI, USA. From 2013 to 2015, he worked as an Analog IC Designer at Biomedical Circuit group of IMEC in Leuven, Belgium. From 2021 to 2022, he was a Visiting Scholar with Arizona State University, Tempe, AZ, USA. In 2015, he joined Ajou University, where he is currently a professor. His research interests include circuit techniques for analog/digital frequency synthesizer phase-locked loop, ultra-low-power clock generation for sensor node system, sensor interface circuits, in-sensor computing, and mixed signal circuits for biomedical applications. Dr. Jee was the recipient of the Gold Prize at the 17th HumanTech Paper Award hosted by Samsung Electronics in 2011.

In-sensor Processing Techniques for Biomedical Applications

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Professor | Ajou University

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| Abstract

In-sensor processing has emerged as a key enabler in biomedical applications where energy efficiency, spatial resolution, and form factors are critical. This work demonstrates two representative implementations: a wearable photoplethysmography (PPG) sensor [1] and an implantable retinal prosthesis chip [2]. The wearable device integrates a pixelated monolithic CMOS PPG sensor with spiking-neural-network-inspired architecture to locally extract spatial features and cancel ambient light interference using machine learning techniques. This architecture reduces power and system complexity while enabling robust physiological signal monitoring. On the other hand, the implantable retinal prosthesis utilizes time-domain in-pixel image processing to perform real-time edge extraction within each pixel. Combined with a bipolar stimulation scheme, it minimizes power and spatial blurring, enabling high-acuity artificial vision with ultra-low power. Both approaches demonstrate how in-sensor processing can transform traditional readout and processing pipelines into localized, task-optimized architectures. By directly embedding intelligence into the sensor layer, these systems offer scalable and application-specific solutions for continuous health monitoring and vision restoration. Together, they exemplify the future direction of bio-integrated electronics where sensing and processing are co-designed at the pixel level.

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Jihoon Seo
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| Biography

Dr. Jihoon Seo is an Assistant Professor of Chemical and Biomolecular Engineering at Clarkson University, where he leads research in advanced semiconductor manufacturing processes, particularly chemical mechanical planarization (CMP). His work focuses on developing innovative CMP slurry formulations and post-CMP cleaning solutions. Dr. Seo significantly contributes to Clarkson's globally recognized CMP research program, emphasizing sustainable manufacturing practices and workforce development within the semiconductor industry. He has established robust collaborations with leading semiconductor companies, securing substantial external funding and earning recognition through Clarkson's 2024 Million Dollar Club and consecutive FuzeHub Manufacturing Awards in 2022 and 2023. Additionally, Dr. Seo actively serves on the Center for Advanced Materials Processing (CAMP) Faculty Advisory Board, organizes Clarkson's annual CMP symposium, participates in semiconductor technology roadmap committees, and holds editorial roles in leading CMP-focused scientific journals.

Integrating Sustainability into Semiconductor Manufacturing:
A Comprehensive Approach to CMP Consumables

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| Abstract

As semiconductor technologies enable innovations in autonomous systems, artificial intelligence (AI), 5G communications, the Internet of Things (IoT), and large-scale data processing, the demand for reliable, high-performance semiconductor manufacturing is on the rise. Meeting this demand requires cutting-edge device architectures that depend on two critical fabrication steps: Chemical Mechanical Planarization (CMP) and post-CMP cleaning

This work focuses on the development of advanced CMP slurry formulations and effective post-CMP cleaning solutions, emphasizing their pivotal roles in modern semiconductor processing. We examine how different slurry synthesis methods influence the surface chemistry of ceria abrasives, thereby affecting silicon dioxide (SiO2) removal rates during shallow trench isolation (STI) CMP. Our results demonstrate that the optimized cleaning solutions can remove ceria abrasive particles as small as 10 nm from SiO2 surfaces, ensuring thorough removal of these residual contaminants and improved process efficiency. Furthermore, we explore the incorporation of aliphatic amino acids as environmentally friendly corrosion inhibitors in CMP slurry formulations. These amino acids offer a sustainable alternative to the conventional benzotriazole (BTA) inhibitor, helping to mitigate the environmental and safety concerns associated with CMP chemicals.

In light of the semiconductor industry's rapid expansion, our research also addresses critical sustainability and environmental health and safety (EHS) objectives in CMP. We propose a comprehensive methodology to evaluate the sustainability of CMP consumables, with an emphasis on slurries given their significant market share and short usage lifetimes. This approach lays the groundwork for future CMP sustainability assessments and encourages proactive improvements within the CMP community to minimize environmental impact. Finally, we establish a framework for Life Cycle Assessment (LCA) of CMP consumables, representing a significant step toward integrating sustainable practices into semiconductor manufacturing. In summary, this study not only advances the technical understanding of CMP and post-CMP processes crucial for next-generation semiconductor devices, but also aligns these processes with pressing environmental sustainability objectives.

Hyejin Park
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| Biography

Hyejin Park received her B.S. degree in Department of Printing Information Engineering from Pukyong National University, Busan, South Korea, in 2008. Followed by M.S. and Ph.D. degrees in Printed Electronics Engineering from Sunchon National University, Suncheon, South Korea, in 2012 and 2019, respectively. Currently, she is a Research Professor in Engineering Research Center for Developing R2R (Roll-to-Roll) Printed Flexible Computer at Sungkyunkwan University, Suwon, South Korea. Her research focuses on the development of printed devices on flexible substrates, including the realization of a sustainable high throughput foundry utilizing R2R gravure printing to fabricate printed processors and microcontrollers on flexible substrates. Her past work primarily concentrated on developing rectifiers to harvest wireless DC power from the NFC signals of smartphones for sensors.

Locust Vision-Inspired Silver Nanowire-Based Printed Near-Infrared Image Sensor Label for Collision Avoidance

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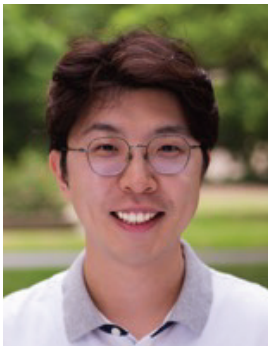
| Abstract

As robot arms are utilized in workplaces to collaborate with humans, collision accidents between the robot arm and humans are often encountered. However, to avoid those accidents, a computer vision system should be integrated into the robot arm, which will exponentially raise the cost. Here, we develop a roll-to-roll gravure (R2Rg) printed silver nanowire (Ag-NW)-based Near-infrared image sensor (NIRIS) label by inspiring the locust vision system, which has compound photoreceptors and a neuron system to efficiently avoid collisions with approaching objects. By utilizing localized surface plasmonic resonance of printed Ag-NWs, NIRIS can be formed like the compound photoreceptors by embossing the array of printed Ag-NW sheets. The detected NIR image will be assessed to determine whether it will collide or not by a simple R2R printed neuromorphic controller, which consists of a single-walled carbon nanotube-based thin film transistor. This NIRIS will serve as a collision-free vision label, allowing the robot arm can cooperate with humans in the workplace without any accidents of collision with extremely low cost.

Reference

[1] Hyejin Park et al., Adv. Electron.2020,6,2000770.



Joonhee Choi
Professor | Stanford University

| Biography

Joonhee Choi is an Assistant Professor of Electrical Engineering at Stanford University. He received his Ph.D. and master's degrees from Harvard University, as well as master's and bachelor's degrees from the Korea Advanced Institute of Science & Technology. Prior to joining Stanford, he was an IQIM Postdoctoral Fellow at the Institute for Quantum Information and Matter (IQIM) at Caltech. Joonhee's research focuses on engineering the dynamics of quantum many-body systems to explore fundamental science and develop practical quantum applications. Throughout his career, he has worked in a wide range of fields, including nonlinear nano-optics, ultrafast phenomena, solid-state and atomic physics, and quantum many-body physics. His expertise extends to practical applications in quantum metrology, quantum simulation, and information processing. Joonhee is the recipient of the Outstanding Young Researcher Award from the Association of Korean Physicists in America (2021), the KSEA Young Investigator Grant (2024), the AFOSR Young Investigator Program (YIP) Award (2025), and the Terman Faculty Fellowship in the School of Engineering at Stanford.

Advancing Nanoscale Quantum Sensing in Quantum-Photonic Hybrid Solid-State Devices

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| Abstract

Quantum sensing with solid-state spins offers a powerful approach for achieving highly sensitive measurements of magnetic and electric fields, temperature, and pressure, as well as for probing quantum many-body interactions at the nanoscale. This approach leverages the unique properties of atomic-scale defects—such as nitrogen- and tin-vacancy centers in diamonds, rare-earth ions in crystals, and optically addressable spins in two-dimensional materials—to surpass the limitations of classical sensing. By employing error-robust control techniques tailored to specific sensing signals and sensor characteristics [1], solid-state quantum sensors can achieve ultrahigh sensitivity and superior spatial resolution [2]. In this talk, I will introduce recent advancements in nanoscale quantum sensing and its applications, including the engineering of high-density rare-earth ion ensembles for probing many-body interactions and preparing time-crystalline states [3], as well as the exploration of spin qubits for precision quantum sensing in two-dimensional van der Waals materials [4].

Reference

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[4] Manuscript in preparation.

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| Biography

Younsu Jung received the M.S degrees in Dept. of Chemistry Education and the Ph. D. degrees in Printed Electronics from Sunchon National University, Korea, in 2009 and 2014, respectively. In 2018, he was an Assistant Professor at the Institute of Innovative Research, Tokyo Institute of Technology, Japan. Currently, he is a Research Professor in Quantum Biophysics at Sungkyunkwan University, Korea. He focused on printed sensors, thin transistors, TFT simulation, and electrochemistry.

Towards green and scalable flexible electronics:
R2R printed 4-bit microprocessor with SWCNT-based logic

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| Abstract

A microprocessor is the central component in nearly all modern electronic systems, such as smartphones, tablets, laptops, routers, servers, automobiles, and Internet of Things (IoT) devices. Although conventional Si-based technologies have enabled the widespread use of microprocessors, they face significant limitations in terms of reducing device weight (flexibility), lowering manufacturing costs, and minimizing environmental impact. Roll-to-roll (R2R) gravure printing has emerged as a promising alternative, offering high throughput, low costs, and large-area fabrication with a minimal carbon footprint and no hazardous byproducts(1, 2). In this study, we present the development and demonstration of the world's first fully R2R gravure-printed flexible 4-bit microprocessor, which consists of over 1,200 thin-film transistors (TFTs) fabricated entirely through a continuous R2R process. To achieve this, we designed R2R-compatible standard cell libraries by optimizing the electrical characteristics of both p-type and n-type single-walled carbon nanotube (SWCNT)-TFTs. These libraries were essential for ensuring reliable logic operation and were validated with a process design kit (PDK), ensuring that the circuit schematics aligned with the physical layouts. Complementary logic operation was achieved by engineering the threshold voltages (Vth) of both transistor types through controlled doping. To minimize Vth variation, we used a rheological tuning method to ensure uniform topography in the printed dielectric patterns, which are particularly sensitive to such variations. To scale down the TFT geometry—including channel length and width—we developed an ensemble linear regression model to analyze registration marker superposition errors over time, allowing us to predict machine-direction (MD) errors within the R2R system. Additionally, we employed Spectre simulations integrated with artificial neural networks to facilitate rapid and variation-aware PDK generation. Following these core strategies, we successfully fabricated a flexible Harvard-architecture 4-bit processor that integrates phase A/B control, a program counter, an accumulator, a FETCH unit, register-out logic, and a 4-bit arithmetic logic unit (ALU). This work establishes a foundation for scalable, eco-friendly, and fully R2R-printed flexible computing systems.

Towards green and scalable flexible electronics:
R2R printed 4-bit microprocessor with SWCNT-based logic

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