Applications of 2D Materials in Future CMOS Nodes

Steven J. Koester

Department of Electrical and Computer Engineering, University of Minnesota-Twin Cities

E-mail: skoester@umn.edu

Two-dimensional (2D) materials offer the promise to continue MOSFET scaling to its ultimate limit due to their controllable monolayer thickness. However, many challenges remain at all levels, from engineering challenges such as layer transfer and process integration, to fundamental questions such as low-temperature growth, carrier mobility and contact resistance. In this talk, I will describe my perspective on the challenges and opportunities facing 2D materials for use in future CMOS nodes. I will first provide a broad overview of my group's research on integrated 2D-material devices including sensors and optoelectronics. Then I will provide a focused discussion on transition-metal dichalcogenides (TMDCs) and discuss the potential applications of these materials for both scaled logic and memory devices. In particular, I will describe our work on phase-engineered contacts to MoTe₂ and show the benefits and limitations of MOSFETs with contacts consisting of the metallic (1T') and semiconducting (2H) phases of this material. Next, I will describe results showing the potential of MoS₂ for use in dynamic memories due to its potential for ultra-low leakage. I will also show recent results on semi-metallic Bi contacts to WS₂ which have greatly reduced contact resistance compared to standard metal contacts, but also have the ongoing challenge of contact gating effects which could still make them susceptible to fluctuations in the local electrostatic environment. Finally, I will provide additional discussion of other challenges to achieving integration and ultimate scalability in 2D MOSFETs.