The Future is Bright for Chips

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Abstract

Designing, manufacturing, and deploying semiconductor chips, either in monolithic single-chip or heterogeneously integrated or monolithic disaggregated form, ushers in a new era of innovation for applications including data center/HPC, mobile/communications/infrastructures, edge/IoT, automotive, bio/health, defense/harsh environment, and others that may not yet be known to us.

In this new era, we believe the absence of a predictable scaling "law" similar to Moore's law will be a once-in-a-lifetime opportunity for the three pillars of the ecosystem (chip/system maker, manufacturer, and EDA) to collaborate and open the aperture of hardware innovation, with the full lifecycle quality and reliability in mind.

In this talk, we will use an example of electronic-photonic co-design to illustrate the possibility of multi-objective architecture exploration, design optimization, and yield enhancement with interpretable AI.