

# Advanced IC Packaging using Silicon Interconnect Fabric

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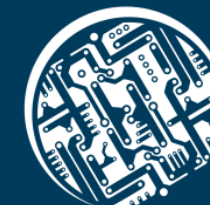
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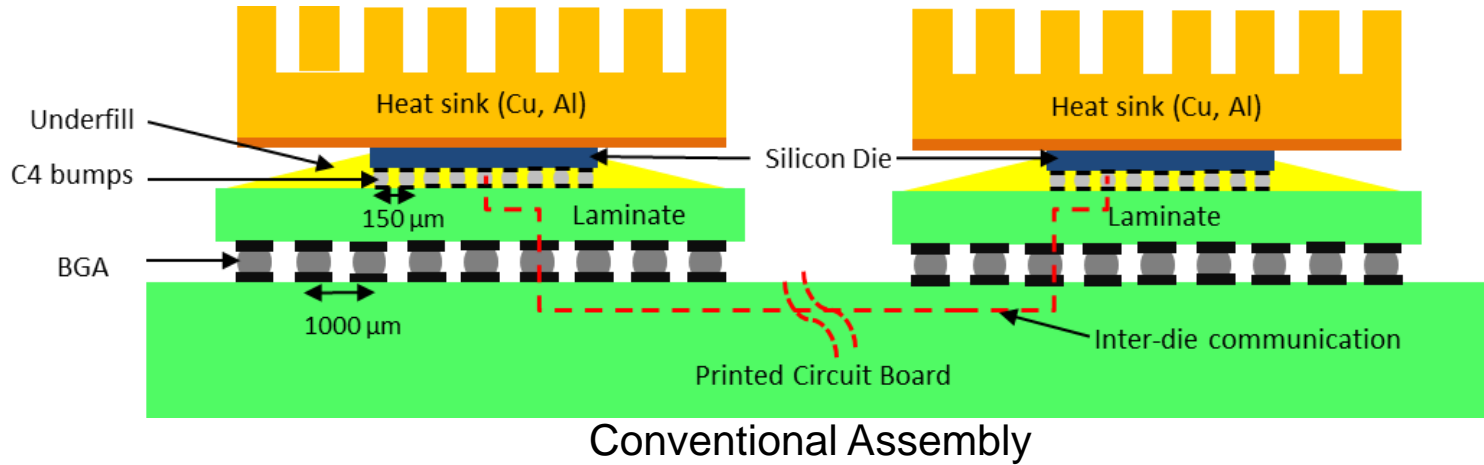
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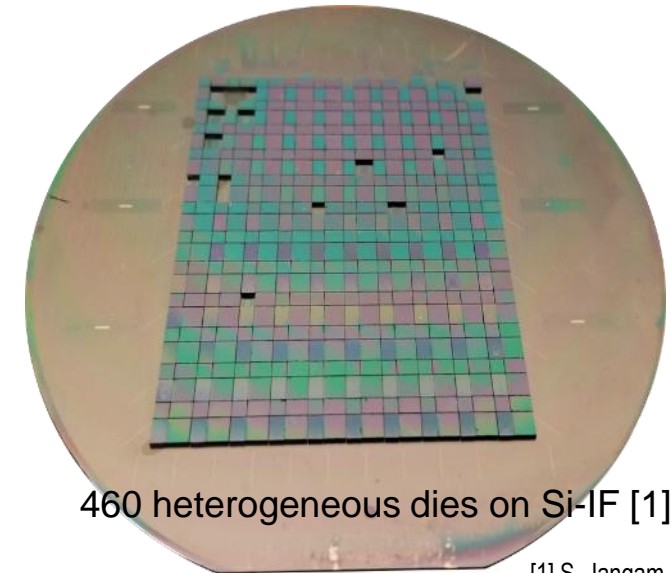
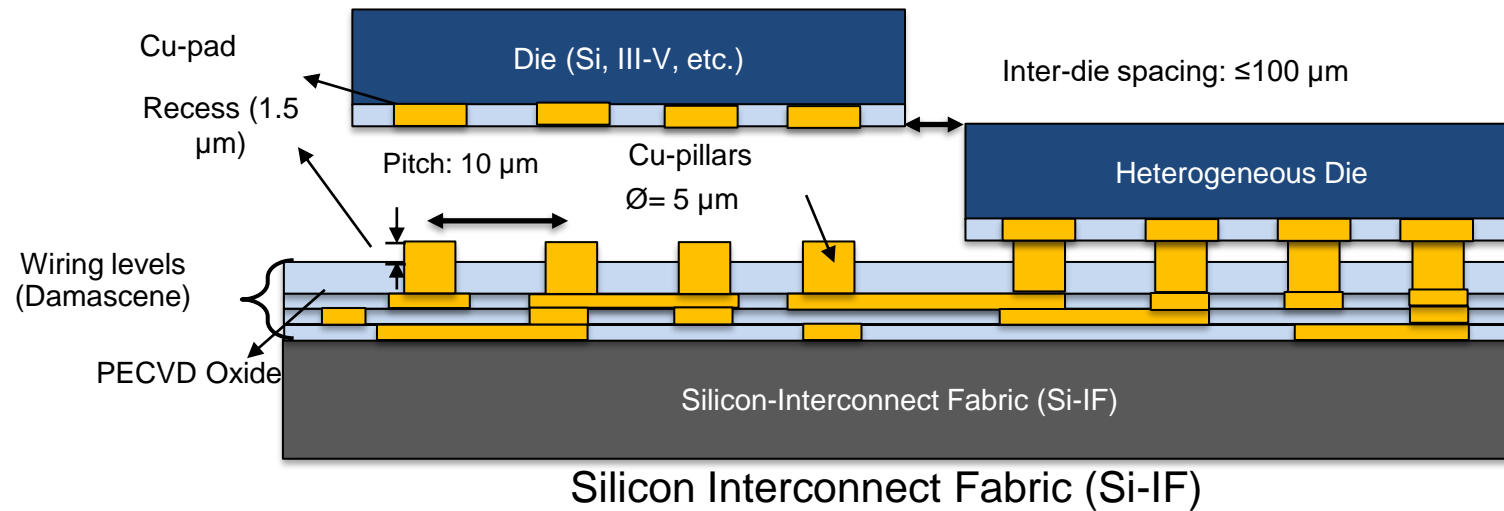


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# Silicon Interconnect Fabric

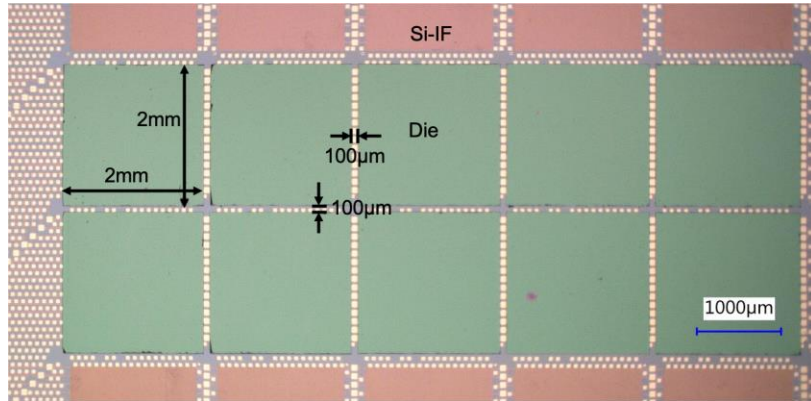


- Conventional Assemblies limited by Si vs package dimensions
  - Large packages, long links, high loss
- Silicon Interconnect Fabric (Si-IF)
  - Fine pitch interconnects:  $<10 \mu\text{m}$
  - Packages-less (die spacing  $<100 \mu\text{m}$ )
  - High bandwidth, low latency & power

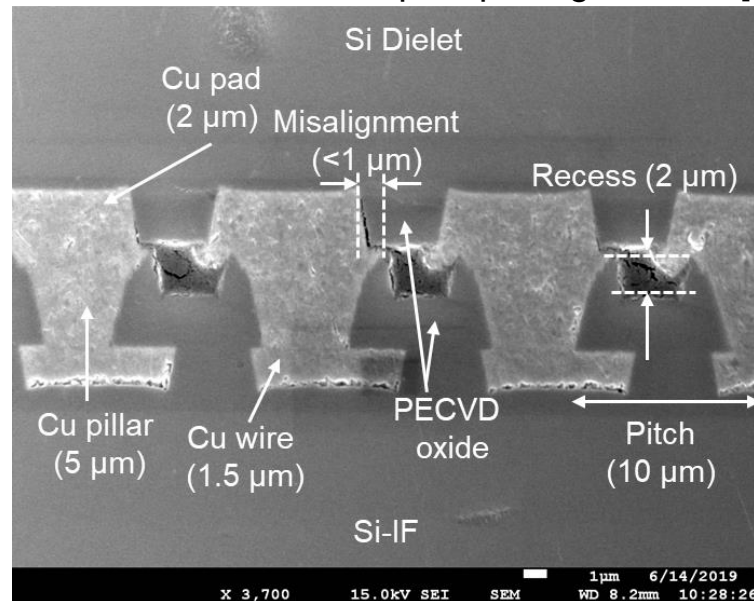


[1] S. Jangam, et al, T-CPMT, 2021

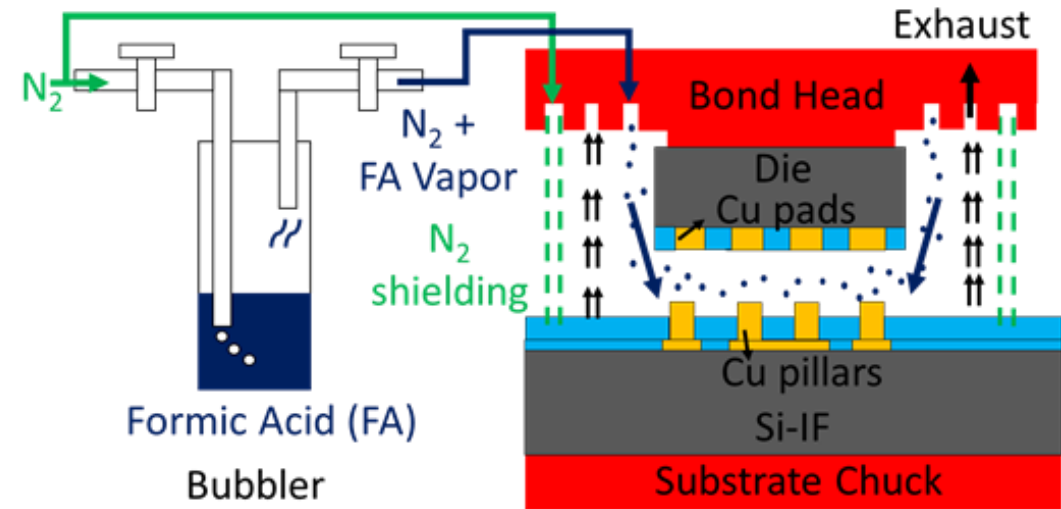
# Fine Pitch Assembly



Dies assembled at 100µm spacing on Si-IF [1]



10µm pitch bonded interconnects [2]

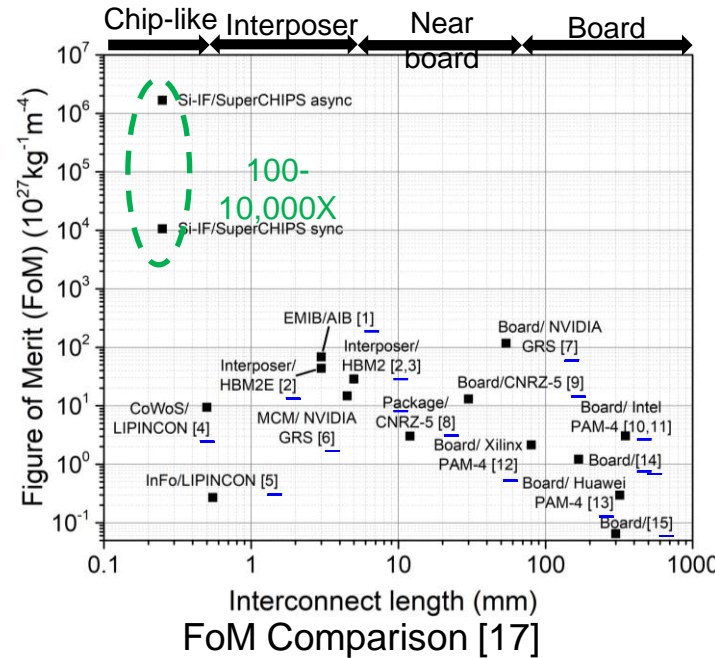
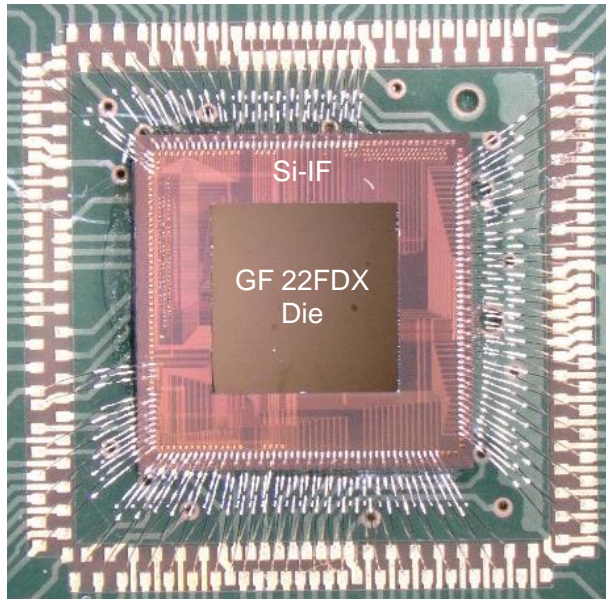
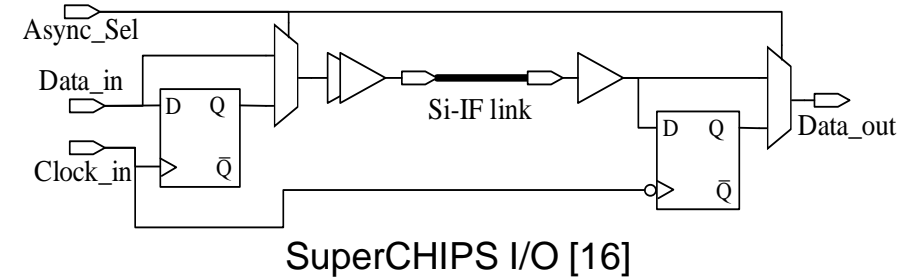
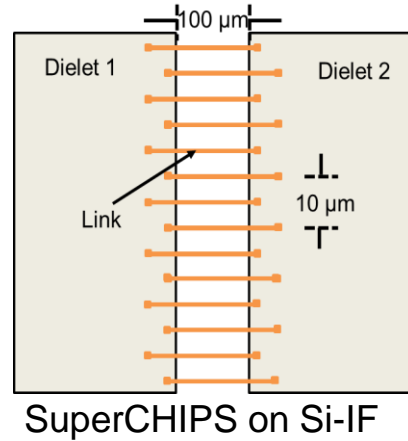
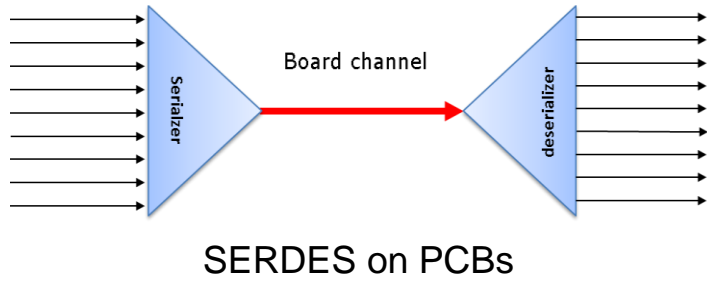


In-situ formic acid treatment setup (In collaboration with K&S) [2]

- Demonstrated sub-10µm fine-pitch interconnects
- Solder-less metal-metal thermal compression bonding (TCB)
  - Temperature & pressure on planar, pristine bonding surfaces
- In-situ formic acid treatment for direct Cu-Cu bonding
  - Local reducing environment under bond-head

[1] S. Jangam, et al, T-CPMT, 2021 [2] S. Jangam, et al, ECTC, 2019

# Simple Universal Parallel intERface for chips (SuperCHIPS)



- High bandwidth & low power using large number of parallel short links
  - Simple inverter based drivers
- Demonstrated SuperCHIPS performance on functional TV
  - Latency: <30 ps (3-65X↓)
  - Energy/bit: <0.03 pJ/b (5-40X↓)
  - Data-Bandwidth: up to 8 Tbps/mm (4-23X↑)

[1] AIB interface [2] HBM JESD235C, 2020. [3] M. O'Connor, MICRO, 2017. [4] M. Lin, JSSC, 2020. [5] M. Lin, et al, HCS, 2016. [6] J. W. Poulton, et al, JSSC, 2013. [7] J. W. Poulton, JSSC, 2019. [8] A. Shokrollahi, ISSCC, 2016. [9] A. Tajalli, JSSC, 2020. [10] Y. Krupnik I, JSSC, 2020. [11] J. Kim et al, JSSC 2019. [12] M. Erett, ISSCC 2018. [13] M. LaCroix et al, ISSC 2019. [14] E. Depaoli, JSSC, 2019. [15] R. Navid, JSSC, 2019. [16] S. Jangam et al, ECTC, 2020. [17] S. Jangam et al, T-CPMT, 2020

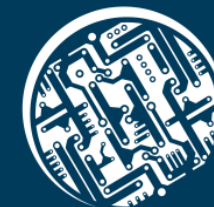
# Thank You!

See you at my poster

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