Semiconductor Research Corporation

DECADAL PLAN FOR SEMICONDUCTORS AND NANOTECHNOLOGY

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Semiconductor Research Corporation

The 17th U.S.-Korea Forum on Nanotechnology:
Next-Generation Semiconductors and the Environmental Implications of Semiconductor Manufacturing

Outline

- My personal journey in the Land of Nanotechnology
- Decadal Plan for Semiconductors
  - Global data storage inventory
  - Compute energy problem
- Microelectronics and Advanced Packaging Roadmap
  - Energy sustainability
  - Environmental sustainability
  - Workforce sustainability
- Summary

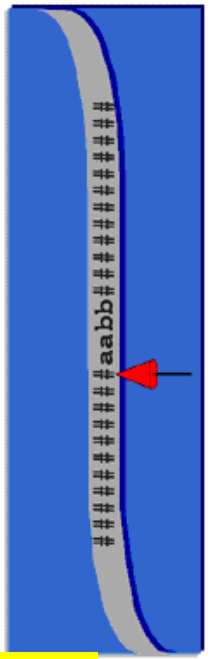
My personal journey in the Land of Nanotechnology: Three decades long

2001 – 2010

ITRS

Binary Transitions

BITS



MIPS
FLOPS

Computing Instructions

Fundamental limits of computing:
What is the upper bound for bit-utilization efficiency in computation?

Fundamental limits of scaling:
How small can a bit be?

Key limitation:
heat removal
(power envelope)

2010 – 2019

2019 – ongoing

Decadal Plan for Semiconductors

Full inventory of bits and bytes

Key limitation:
Energy envelope

2022 – ongoing

Microelectronics and Advanced Packaging Technologies Roadmap

Fundamental and **Practical** limits of ICT sustainability:

- *Energy sustainability*
- *Environmental sustainability*
- *Workforce sustainability*

Limits to Binary Logic Switch Scaling—A Gedanken Model

VICTOR V. ZHIRNOV, RALPH K. CAVIN, III, FELLOW, IEEE,
JAMES A. HUTCHBY, SENIOR MEMBER, IEEE, AND GEORGE I. BOURIANOFF, MEMBER, IEEE

Invited Paper

How Deep Can Multicore Processing Go?

By Mark LaPedus
EE Times

February 15, 2007 09:07 PM

Mark Bohr, an Intel senior fellow and director of process architecture and integration at the microprocessor giant, said that future devices could theoretically scale down to 1.5-nm, with 0.04-ps switching speeds and 0.017 electron volts in terms of power consumption.

Bohr's forecast was based on a paper by V. Zhirnov in the November 2003 issue of "Proceedings of IEEE," where the minimum quantum well dimensions were estimated to be 1.5-nm.

$$P = \frac{0.017eV \cdot 1.6 \cdot 10^{-19}}{0.04\,ps \cdot 1.5nm^2} =$$

$$P = 3,000,000 \frac{W}{cm^2}$$

Sun

Limits of Cooling?

https://www.src.org/about/decadal-plan/

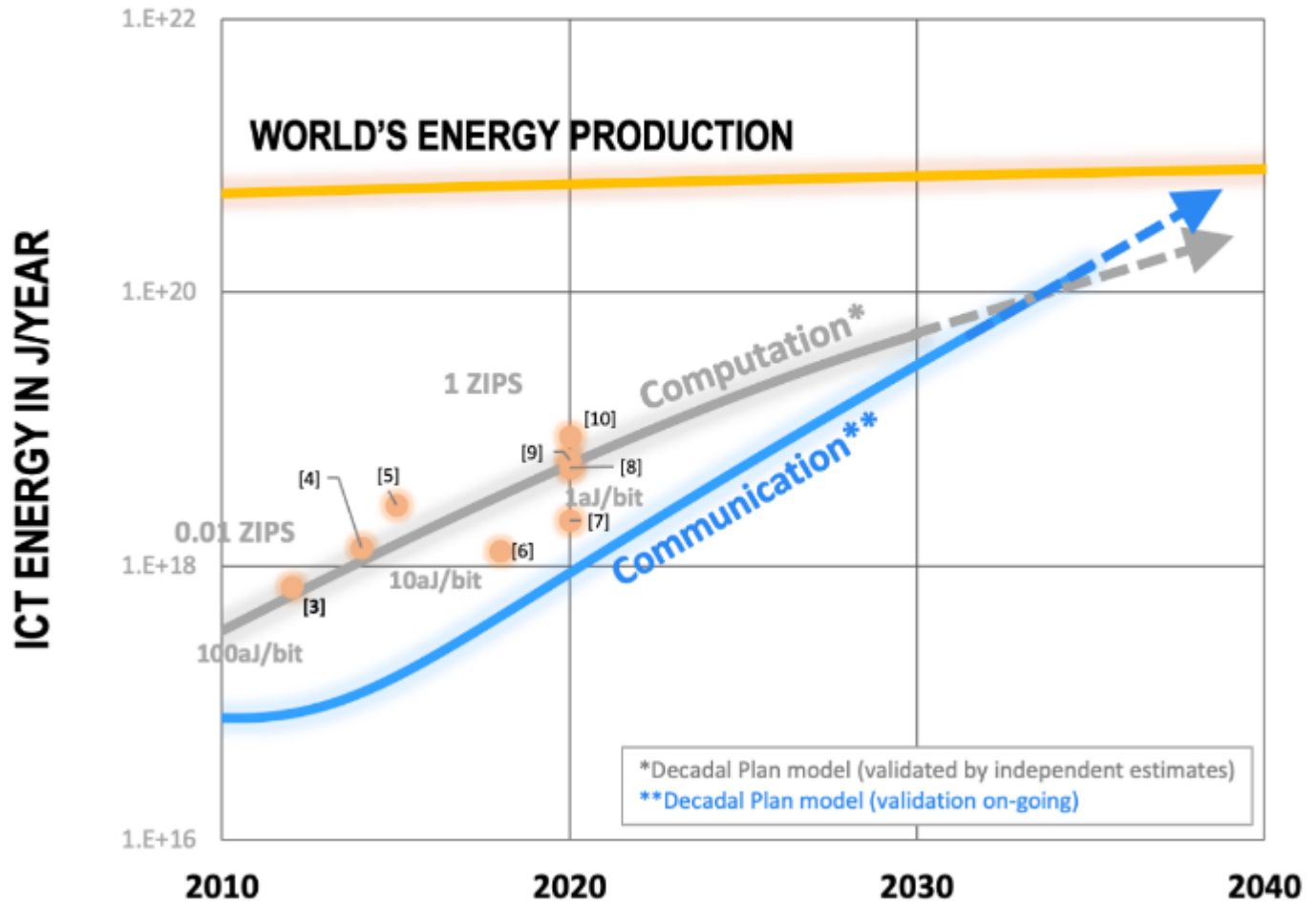
Five "Seismic Shift" Research Priorities

- Smart Sensing — The Analog Data Deluge
- Memory & Storage — The Growth of Memory and Storage Demands
- Communication — Communication Capacity vs. Data Generation
- Security — ICT Security Challenges
- Energy Efficiency — Compute Energy vs. Global Energy Production

SRC

By design, the Decadal Plan focuses on WHAT to accomplish, not HOW to accomplish it.

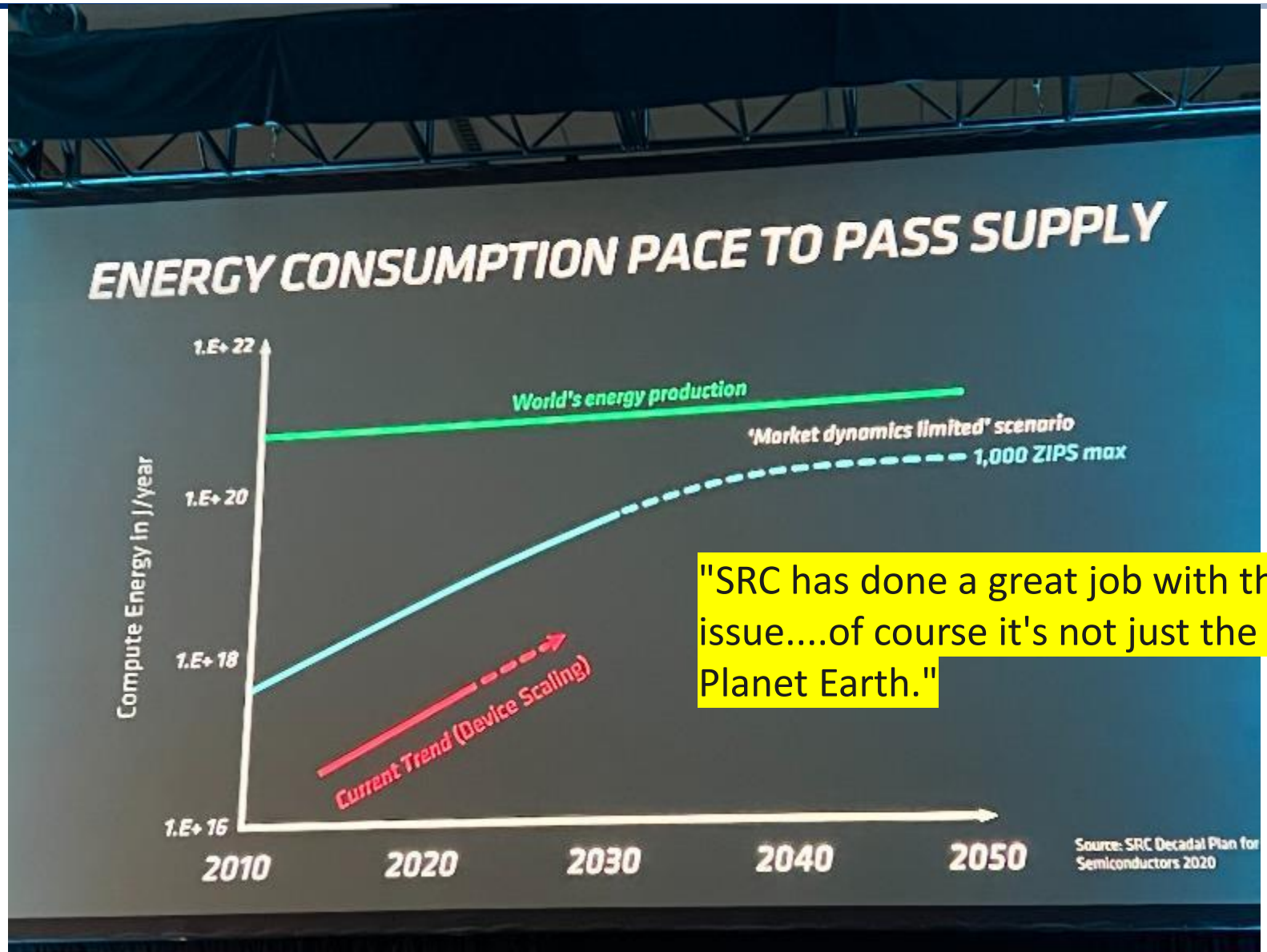
ICT ENERGY
COMPUTATION AND COMMUNICATION



By design, the Decadal Plan focuses on WHAT to accomplish, not HOW to accomplish it.

Opening keynote talk at DAC 2022 (by Mark Papermaster, AMD CTO)

[Semi Engineering - What Future Processors Will Look Like, Mark Papermaster (AMD)]



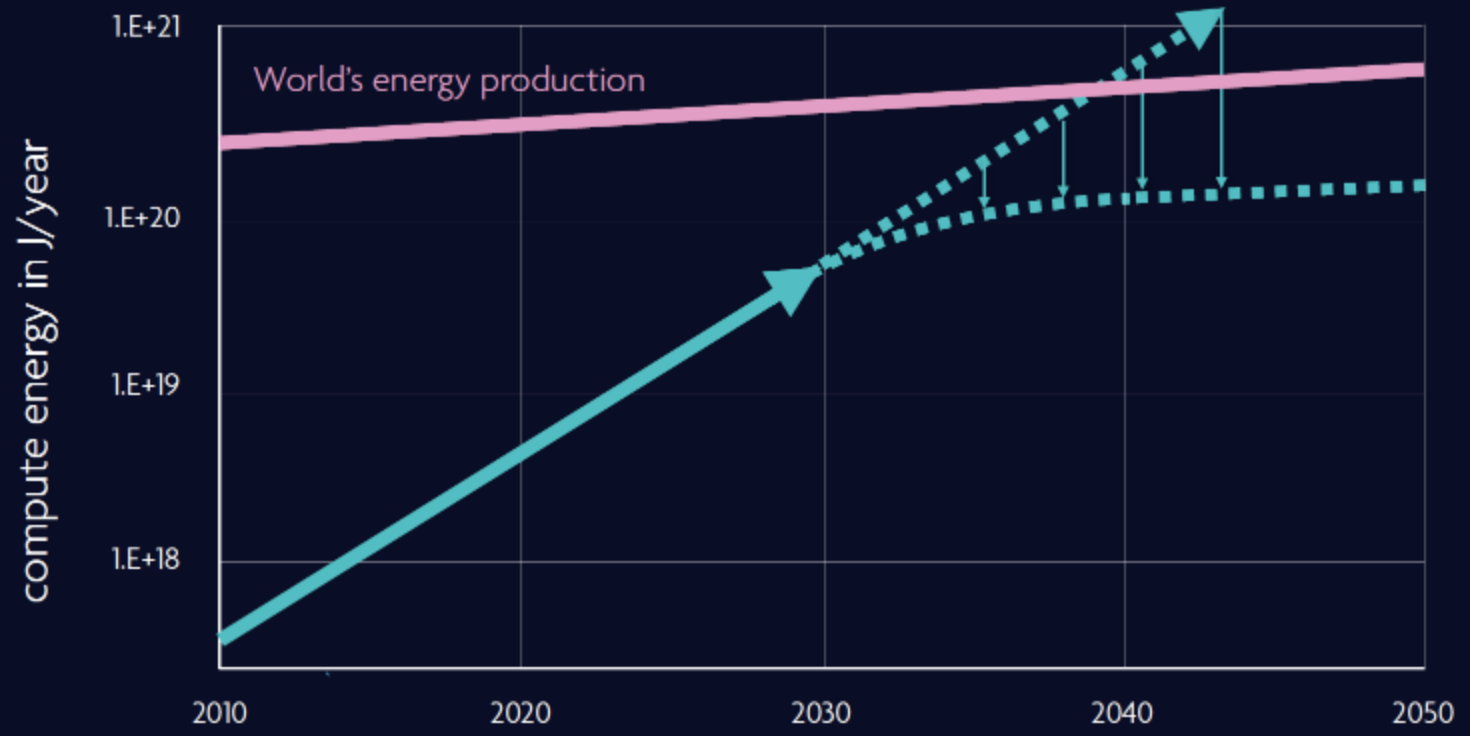
"SRC has done a great job with their Decadal Plan to highlight this issue....of course it's not just the energy used, it's the impact on Planet Earth."

The **Endless Proceed** of **Moore's Law**

+ Luc Van den hove - President & CEO imec

Luc Van den Hove's presentation slides 16-17

New energy-efficient computational concepts become critical



Source: SRC decadal plan 2020

SRC

imec
embracing a better life

A **Future Shaped** by **Energy**

Jan M. Rabaey

SRC

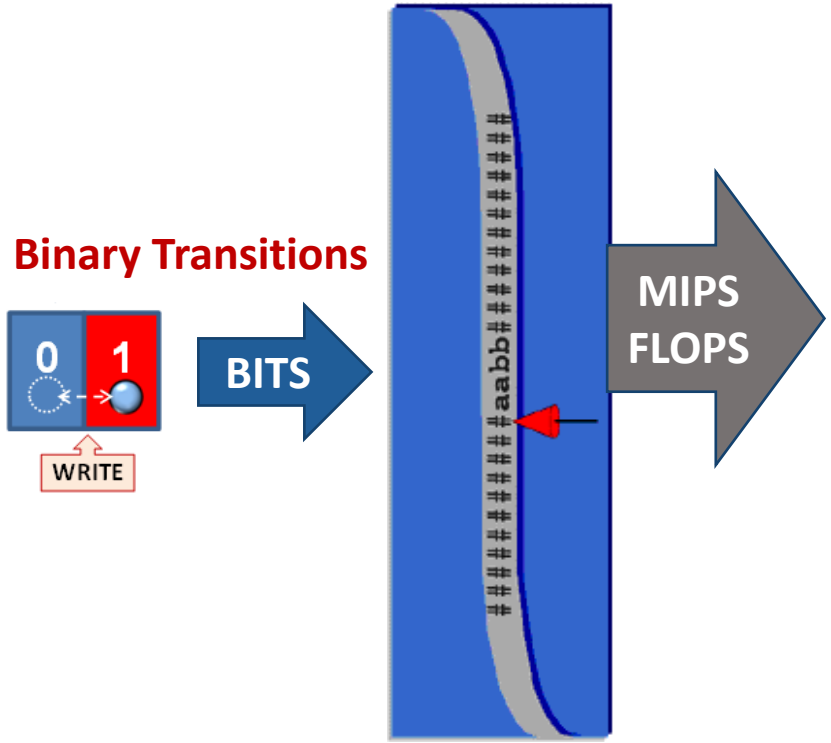
CPU operations vs. binary transitions

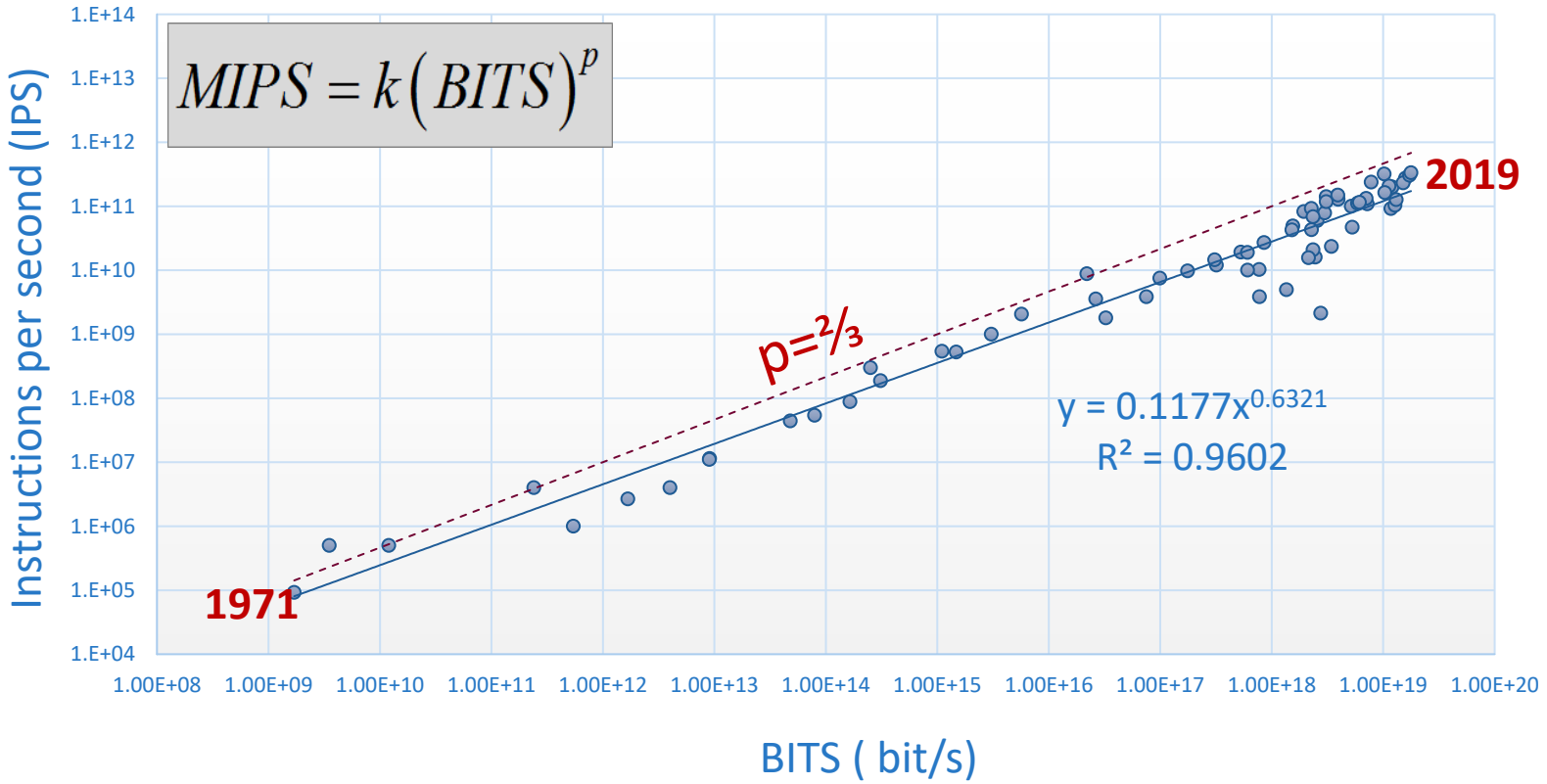
$$\mu = f(\beta) = k\beta^{p}$$

k=0.1, p= 0.64 ≈ ⅔

Computing Instructions

Binary Transitions





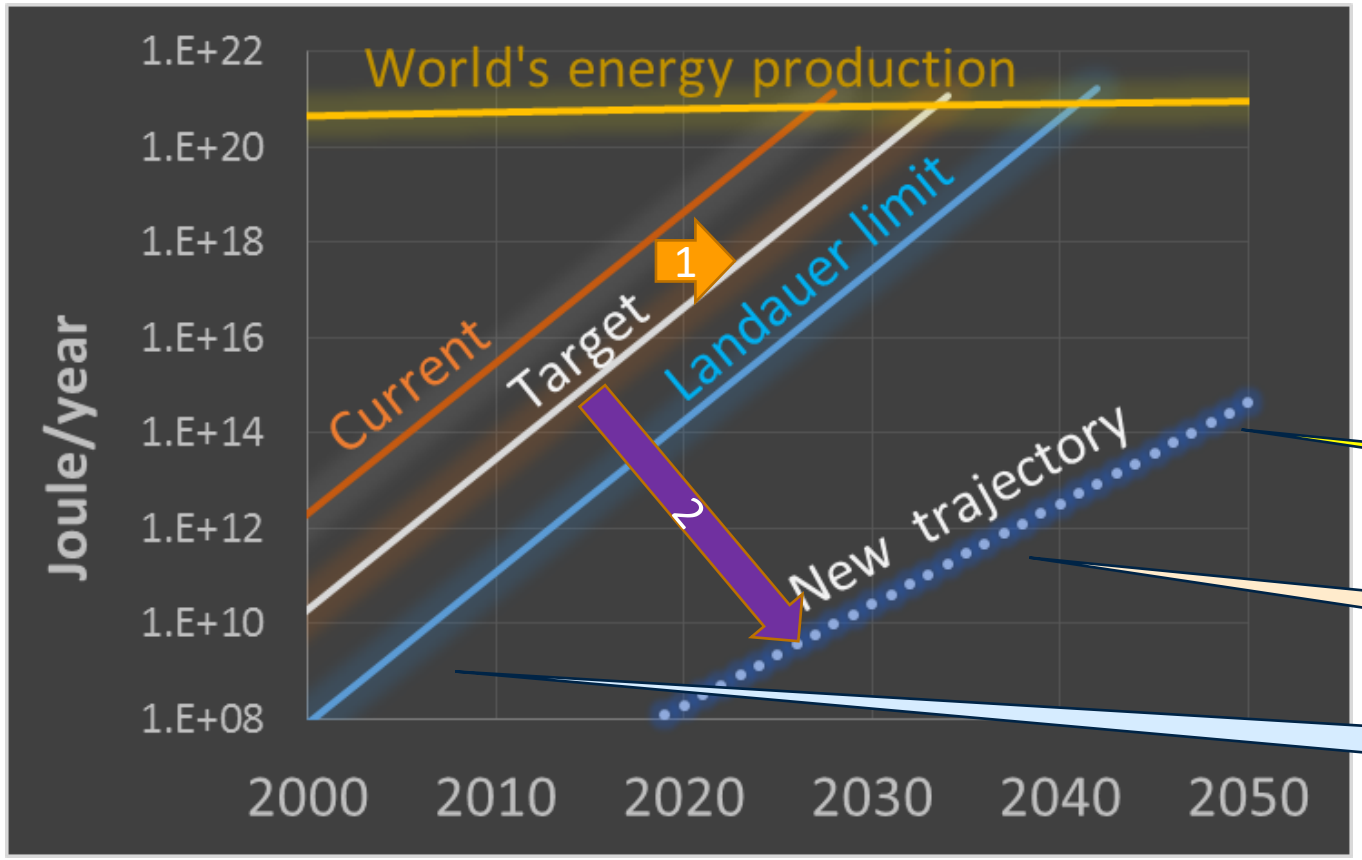
The key question is *bit-utilization efficiency* in computation

$$\beta = \alpha N_{tr} \cdot f \quad \Rightarrow \quad P = \beta E_{bit}$$

Total energy of computing: A need to change 'computational trajectory'

(based on research by Hilbert and Lopez: M. Hilbert and P. Lopez, "The World's Technological Capacity to Store, Communicate, and Compute Information", Science 332 (2011) 60-65

$$MIPS = k\left(BITS\right)^{p}$$



Existing trajectory: $p \approx \frac{2}{3}$

Current: 10^{-16} J/bit

Target: 10^{-18} J/bit

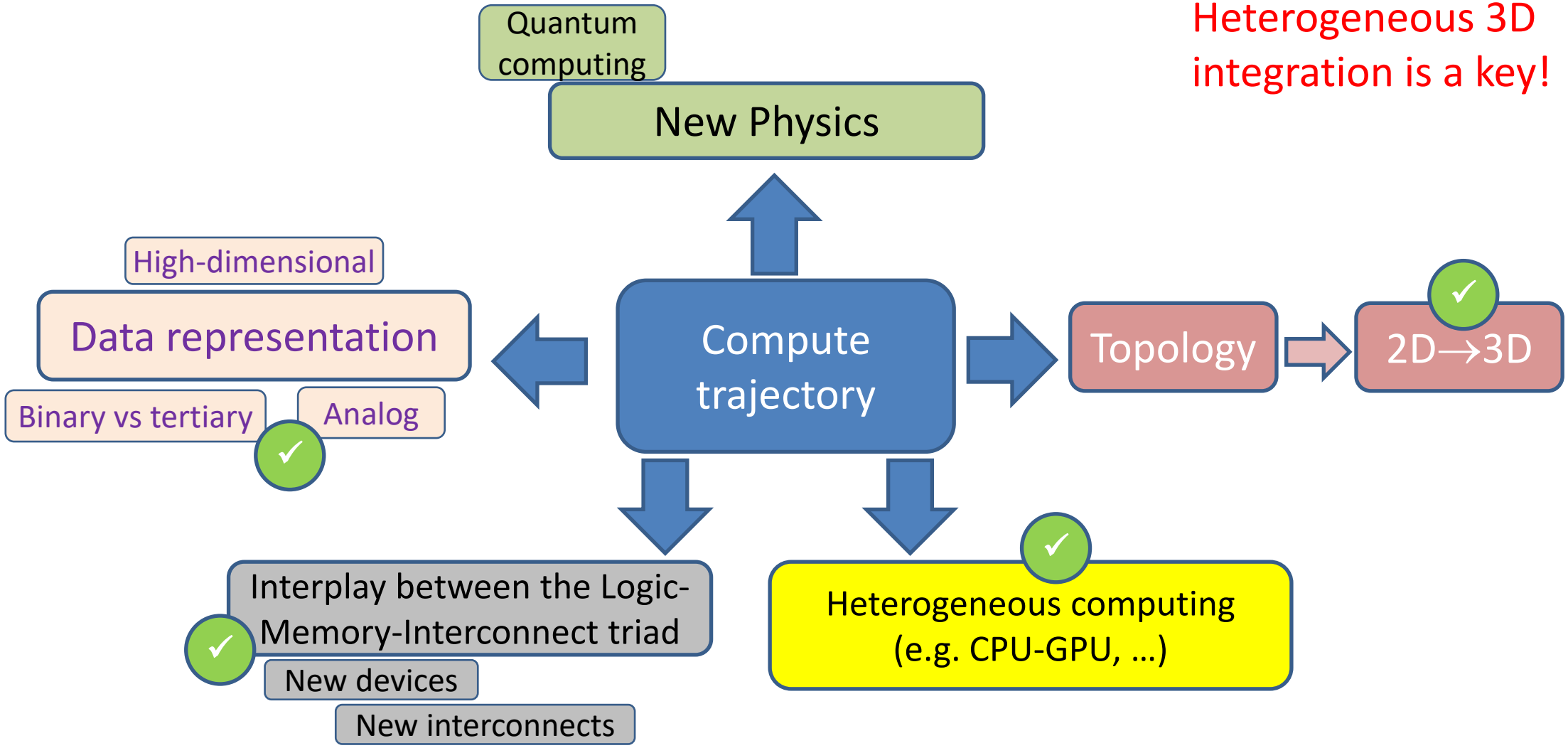
Landauer limit: 10^{-21} J/bit

New trajectory: $p \approx 1$

- Quantum computing
- Neuromorphic
- Efficient AI engines

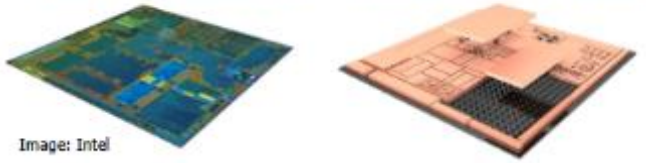
Towards new compute trajectories for energy efficiency

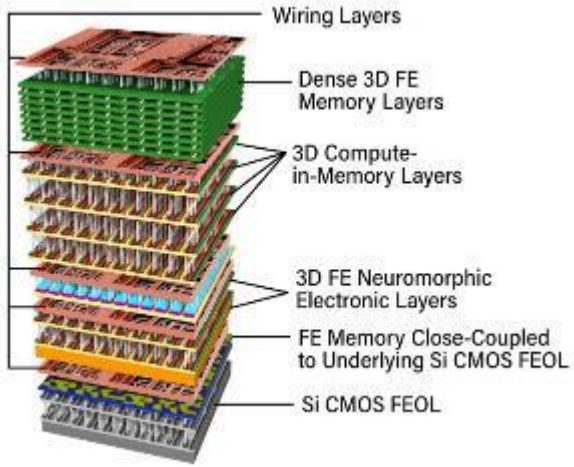
Heterogeneous 3D integration is a key!

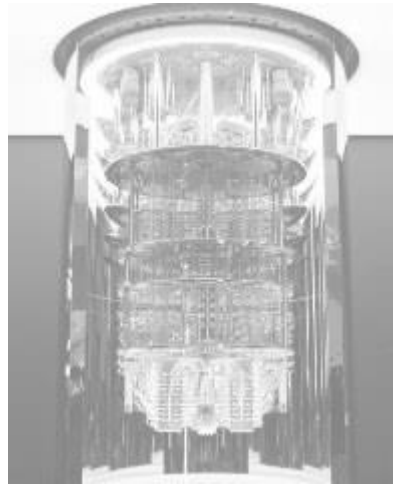


Next microelectronic revolution

We must evaluate market-driven opportunities "side-by-side" to realize lasting innovations







Priority 1

2.5D and 3D Advanced Packaging

Image: DARPA/Intel
https://www.darpa.mil/program/common-heterogeneous-integration-and-ip-reuse-strategies

Priority 2

3D Super Chips

Image: SIRO, Penn State, Prof. Vijay Narayanan
https://news.psu.edu/story/625834/2020/07/15/research/over-10-million-awarded-penn-state-energy-center

Priority 3

Hardware for New Paradigms

Image: IBM Q system displayed at CES 2020
https://www.fierceelectronics.com/electronics/what-quantum-computing

Advanced Packaging, along with 3D monolithic and 2.5D/3D heterogeneous integration, will be the key enabler of the next microelectronic revolution. In fact, advanced packaging+3D is becoming the equivalent of transistor of the Moore's Law and ITRS era.

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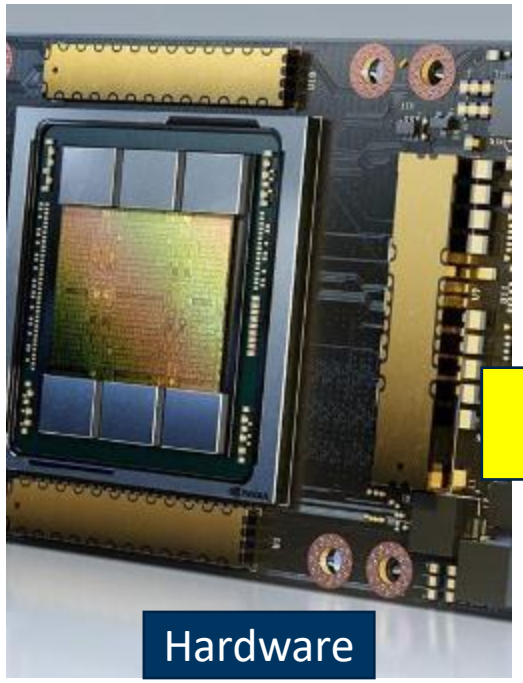
MAPT: From Decadal Plan to actionable all-industry Roadmap

Microelectronics and Advanced Packaging Technologies Roadmap

MAPT: A natural next step for Decadal Plan



Who/When/Where?

Decadal Plan
defines **WHAT** is needed
- Plan for 10 years

MAPT Roadmap
defines **HOW** to accomplish

MAPT team is developing the first industry-wide 3D semiconductor roadmap to guide the forthcoming microelectronic revolution

CHIPS Funding
implementation plan
- Industry, academia, gov. labs
- NSTC, NAPMP
- Manufacturing USA Inst.

Interim Report - https://srcmapt.org/about/

106 participation organizations

~250 individual participants

Final version due 31/10/2023

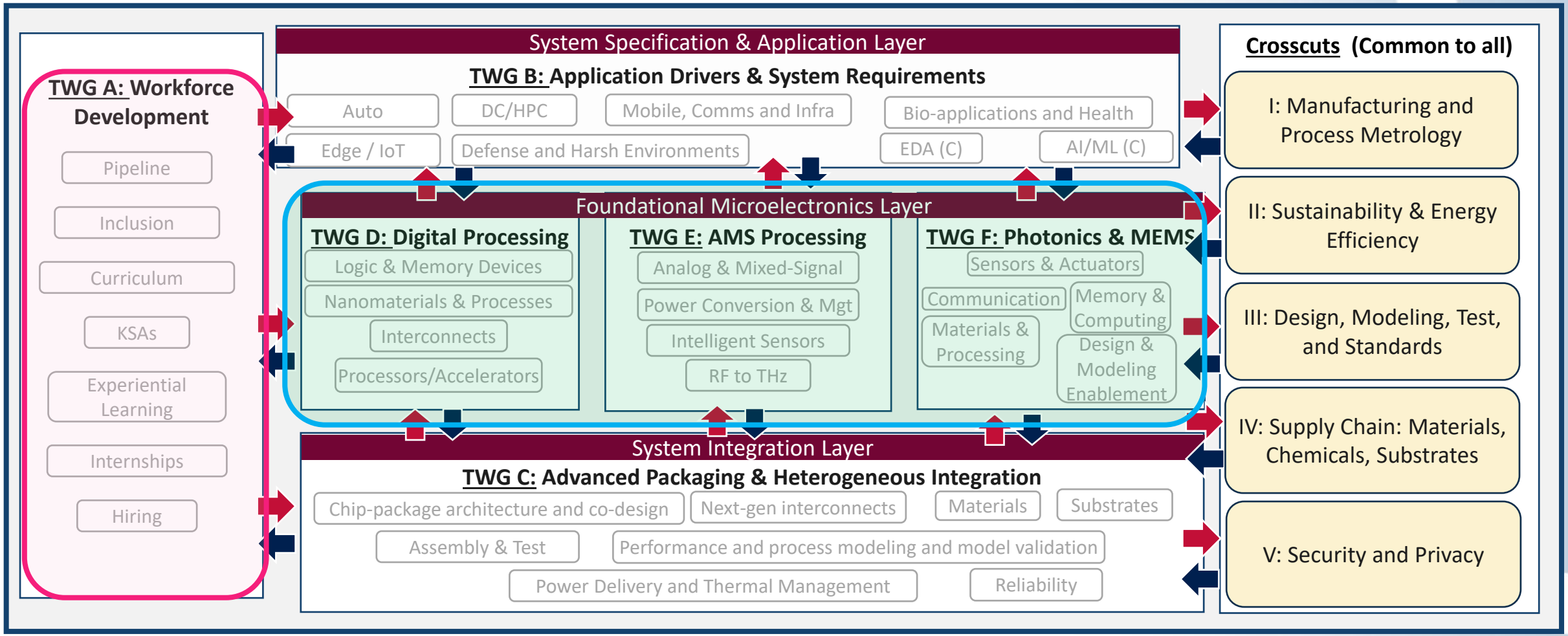
MAPT Roadmap

Organization Structure

Specs

Requirements

Needed: 3D-IC platform for multi-chiplet system design and advanced packaging



SRC

MAPT is the first industry-wide 3D semiconductor roadmap to guide the forthcoming microelectronic revolution - *like the ITRS has served in the past*.

ITRS

2D transistor scaling to < 1nm

nm-scale patterning for 2D chips

MAPT

Transistor scaling provides less value node-to-node

3D chips: Dep+Etch is the new litho

1. **Use ALD, ALE, or other self-limiting reactions to address 300mm equipment-related opportunities in Stacked 2D material transistors**
2. **Use ALD, ALE, or other self-limiting reactions to address 300mm equipment-related opportunities in BEOL Transistors**
3. **Use ALD, ALE, or other self-limiting reactions to address 300mm equipment-related opportunities in Thermal Management Solutions**

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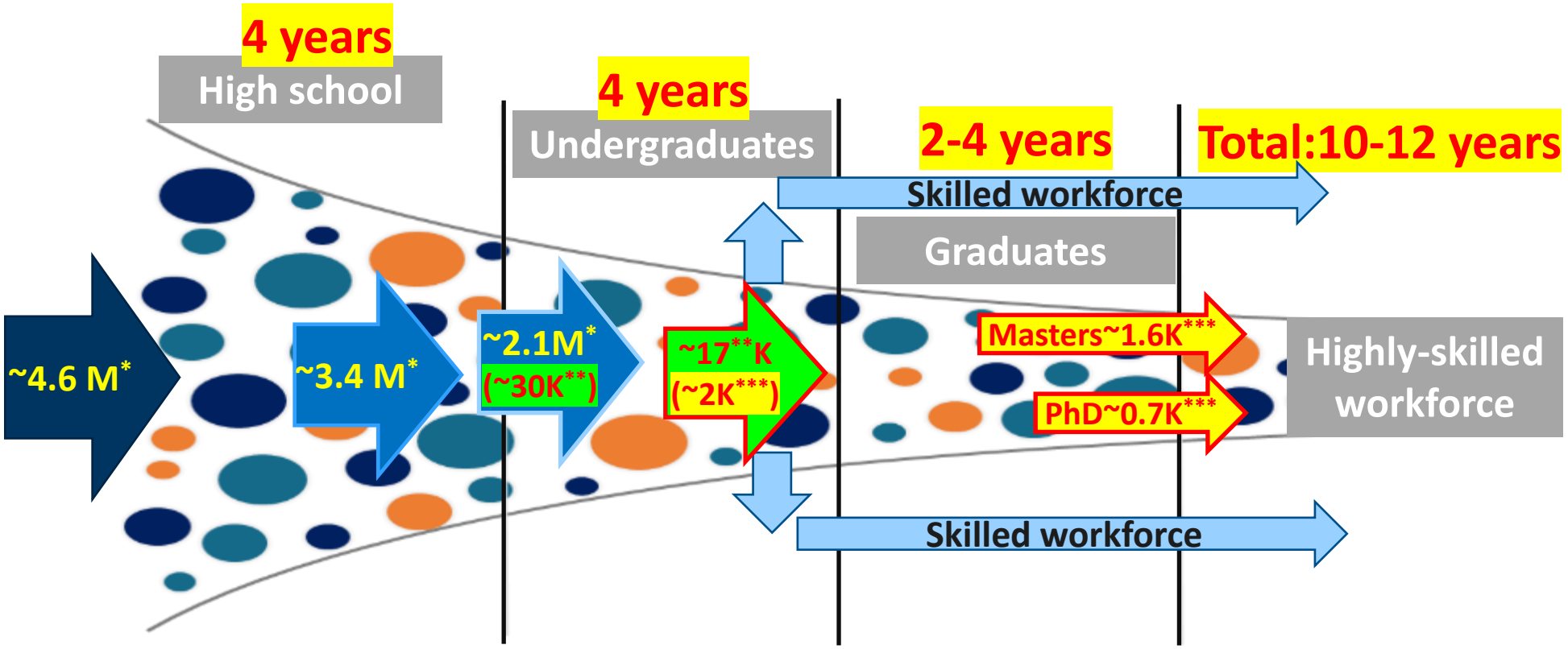
Semiconductor Workforce Development Pipeline



*total number of students in 2021

IES NCES National Center for Education Statistics

**2021 EE & ECE statistics

ASEE 2021 Edition
Engineering & Engineering Technology BY THE NUMBERS

*** EE & ECE semiconductor students

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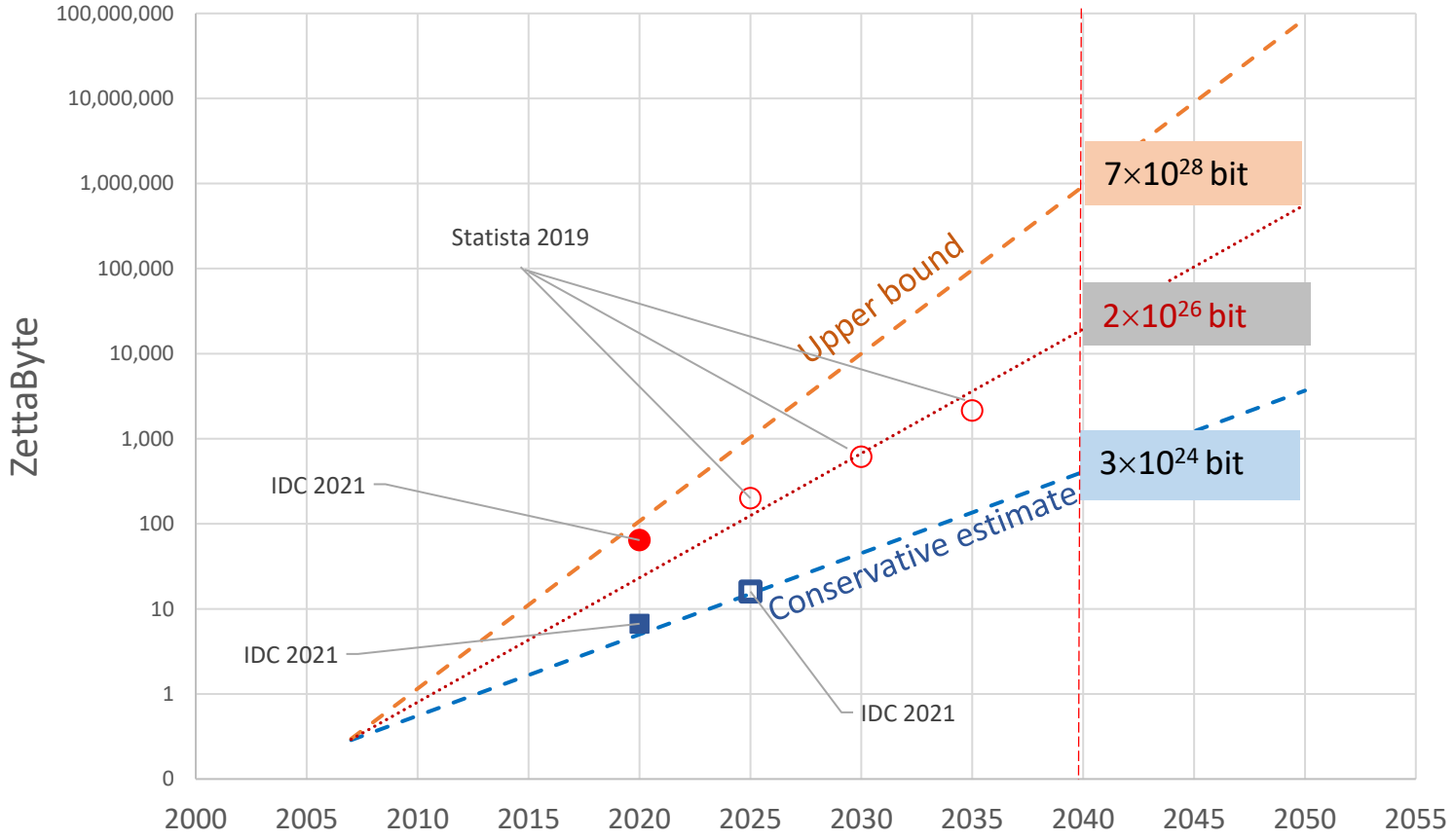
Decadal Plan and MAPT highlights

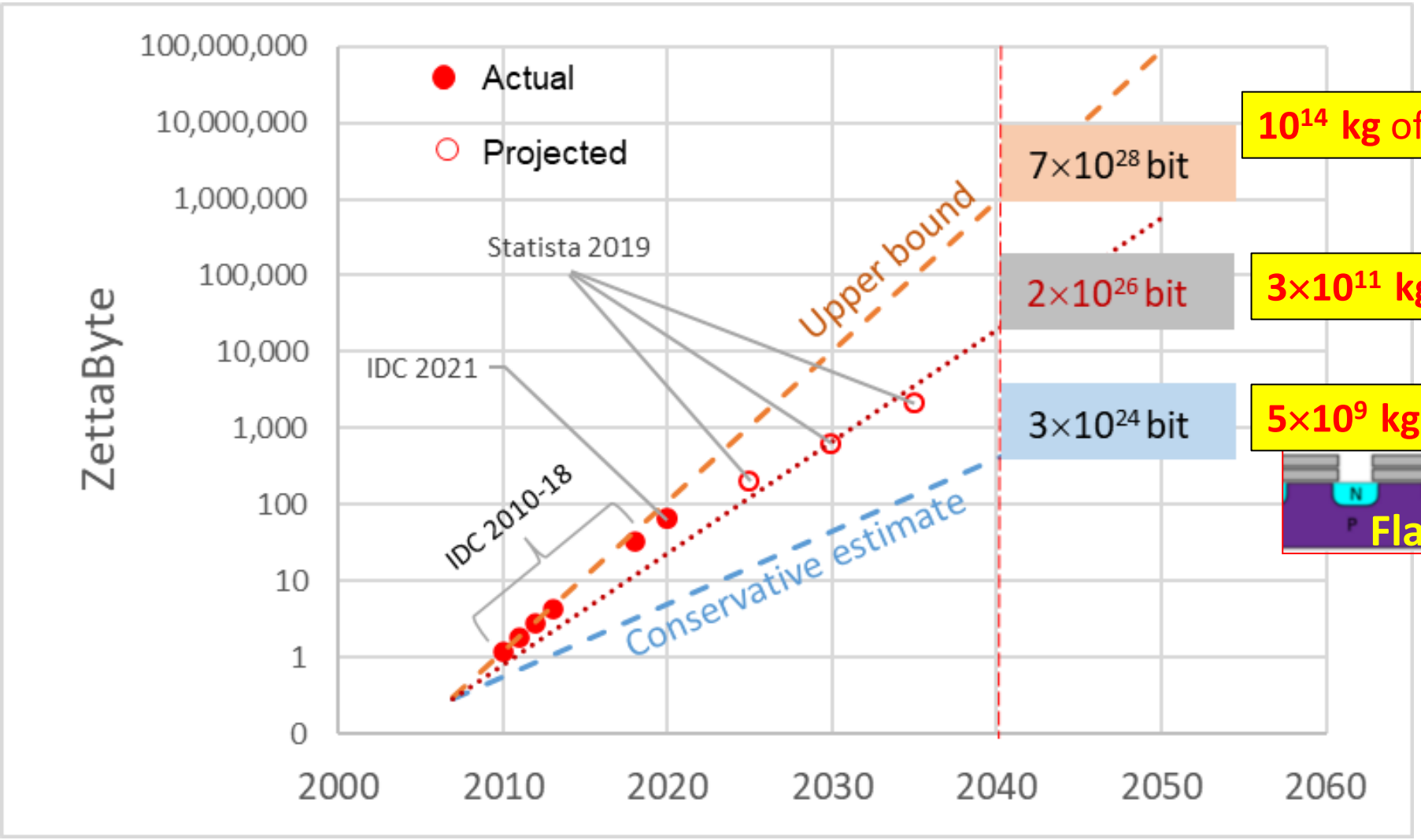
Decadal Plan model for global data storage needs

Those who own the memory innovation, own the data, and own the future



What materials resources will be needed to sustain developments of information technologies?

Trend: Dramatic storage needs increase

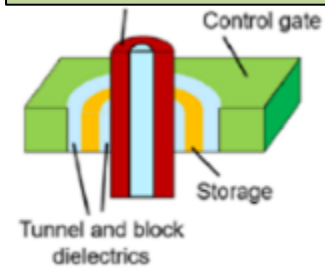


12,000 layers (QLC)

10^8 kg of *Si*

1,020 layers (TLC)

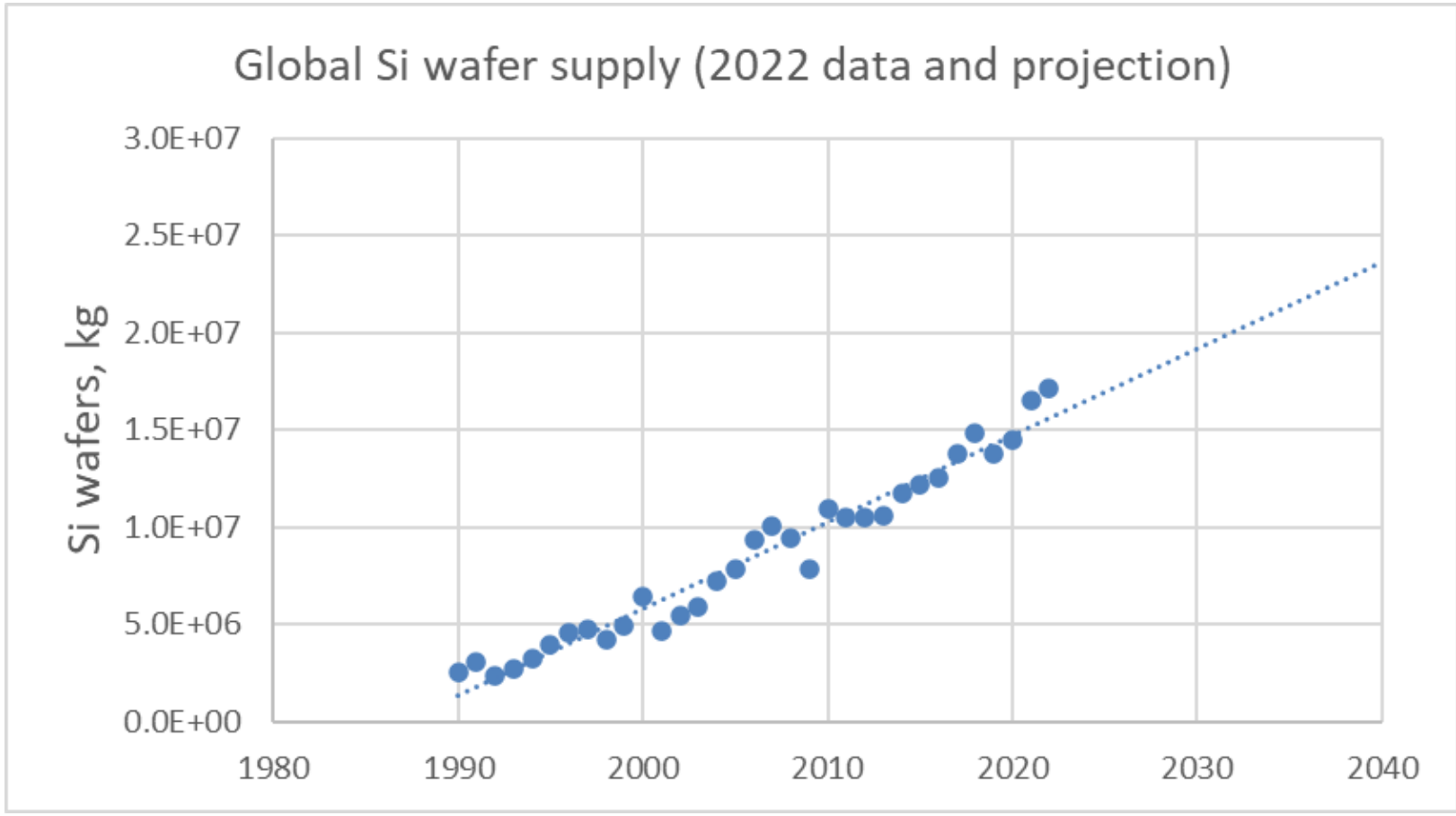
2.5×10^7 kg of *Si*



Problem: ***Projected annual global supply of Silicon wafers:* 2.4×10^7 kg in 2040**

Global Silicon Wafer Supply Trend

(updated 12/5/2022)

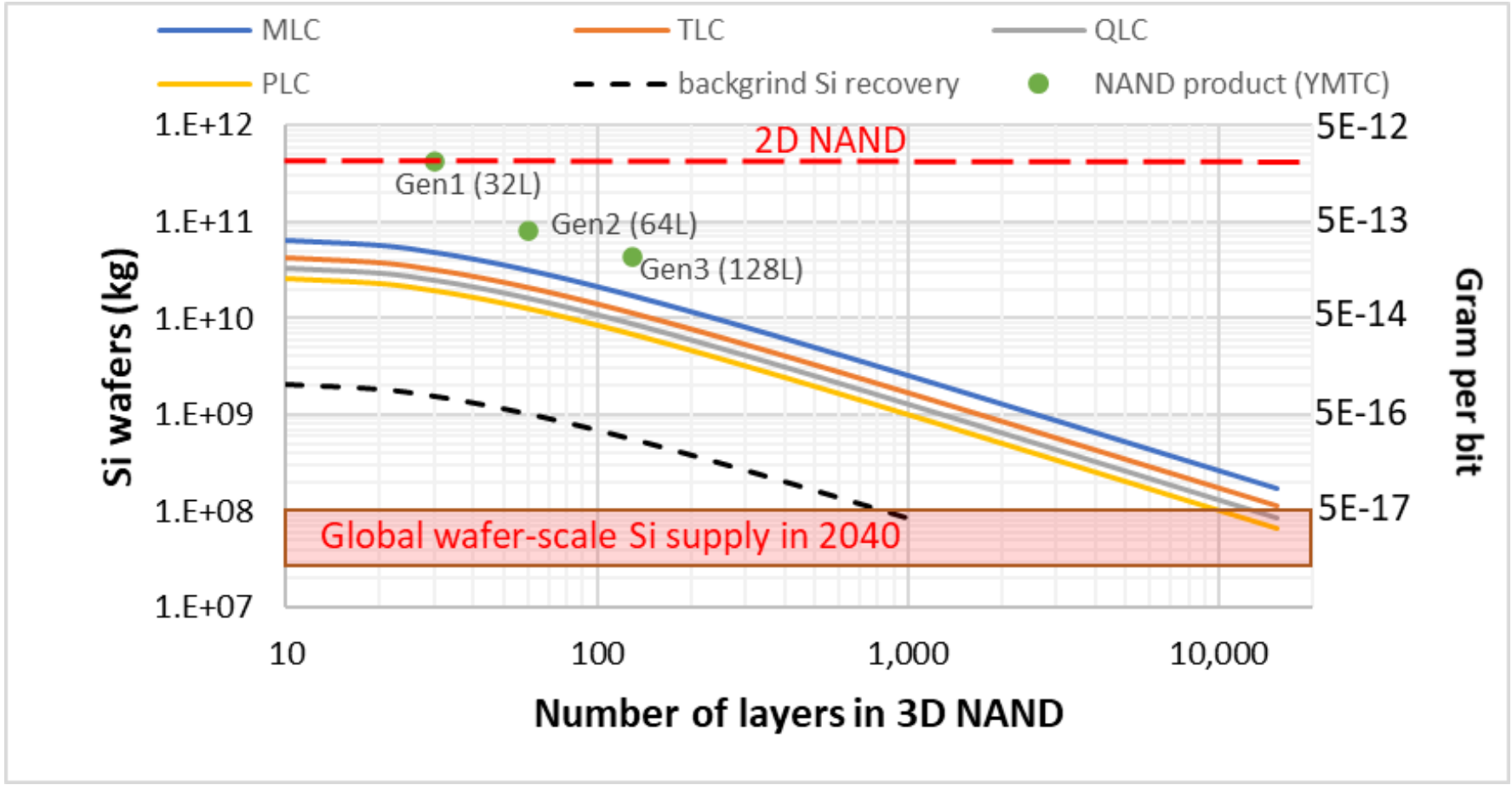


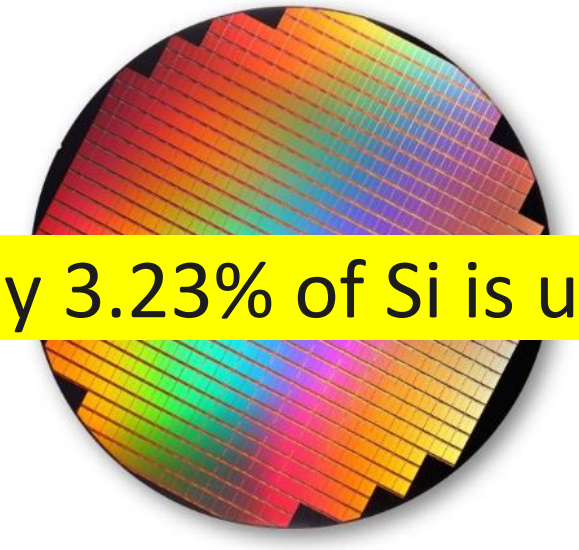
IEEE VLSI Circuits & Systems Letter
QUARTERLY PUBLICATION OF
IEEE COMPUTER SOCIETY TECHNICAL COMMITTEE ON VLSI (TCVLSI)
Volume 7 Issue 4 Nov 2021

The future of NAND flash – compute and non-volatile memory fusion!

Sean Eilert[1], Steffen Hellmold[2], Steve Kramer[1], and Victor V. Zhirnov[3]

[1]Micron Technology Inc.
[2]Western Digital Corp.
[3]Semiconductor Research Corp.





Only 3.23% of Si is used!

ESH Grand Challenge

https://esg.tsmc.com/csr/en/update/greenManufacturing/caseStudy/44/index.html

Waste Si from backgrind gets lost

Table S3 | Diameter and thickness of standard Si wafers

Wafer diameter (mm)	Wafer thickness (mm)
100	0.525
150	0.625
200	0.725
300	0.775
450*	0.925

* Preproduction wafer diameter under development

TSMC Pioneers Physical Regeneration Technique for Backgrinding Wastewater

Recycled Industrial-grade Silicon Products Are Introduced into Steel Industry to Realize Circular Economy

2021/02/25

 P.H. Chiou
 Yu-Wu Chen
 Fu-An Wu
 Kidd Hsu

TSMC's waste management strategies primarily focus on circular economy and source reduction. A large amount of wastewater can be generated during the semiconductor advanced packaging process. In 2020, TSMC led the industry to initiate the physical regeneration technique without chemical additives for backgrinding wastewater treatment. By January 2021, TSMC has saved the use of more than 55 metric tons of chemicals. In addition, the products are transformed from inorganic sludge into high-purity industrial-grade silicon. TSMC has sold out the first batch of silicon products in December 2020, achieving a circular economy with innovation. Taking a step further, the silicon products will be used as deoxidizer in the steelmaking process.

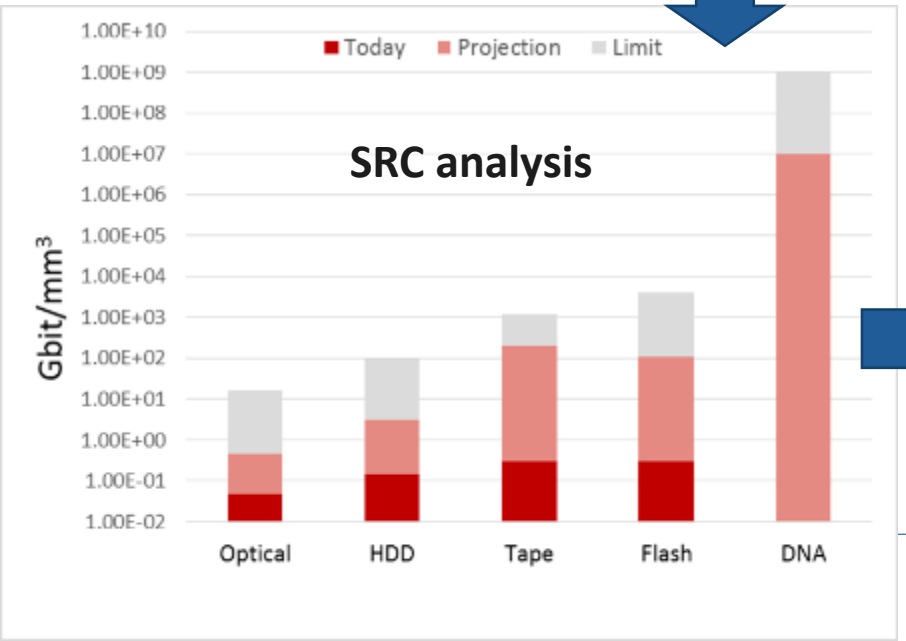
Creating New Industry

Seismic Shift: Dramatic global Storage requirement increase

2040 storage needs >1000 zettabytes (>10^{24}Bytes)

Grand Challenge

Today's storage technologies will not be sustainable in near future due to excessive material resources needed to support the ongoing Data Explosion



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SRC/NSF SemiSynBio Program

National Institute of Standards and Technology

Office of the Director of National Intelligence
IARPA
BE THE FUTURE

New Industry

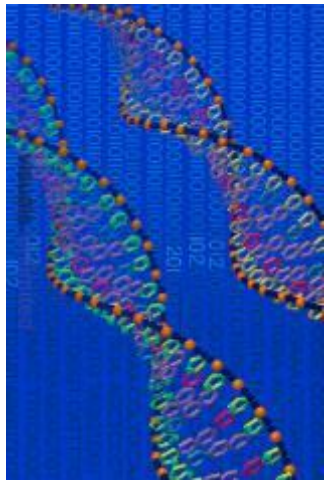
IARPA's Molecular Information STorage (MIST) Program

The birth of new industry

DNA Data Storage Alliance

Storage Networking Industry Association (SNIA)

DNA Data Storage concept



Birth of new industry

arm

Western Digital.

Micron

CATALOG
INFINITE DATA ARCHIVES

evonetix

amazon

IBM

illumina

TWIST BIOSCIENCE

IRIDIA

MARVELL

intel

DNA SCRIPT
NextGen DNA Synthesis

MOLECULAR ASSEMBLIES

Microsoft

DELL

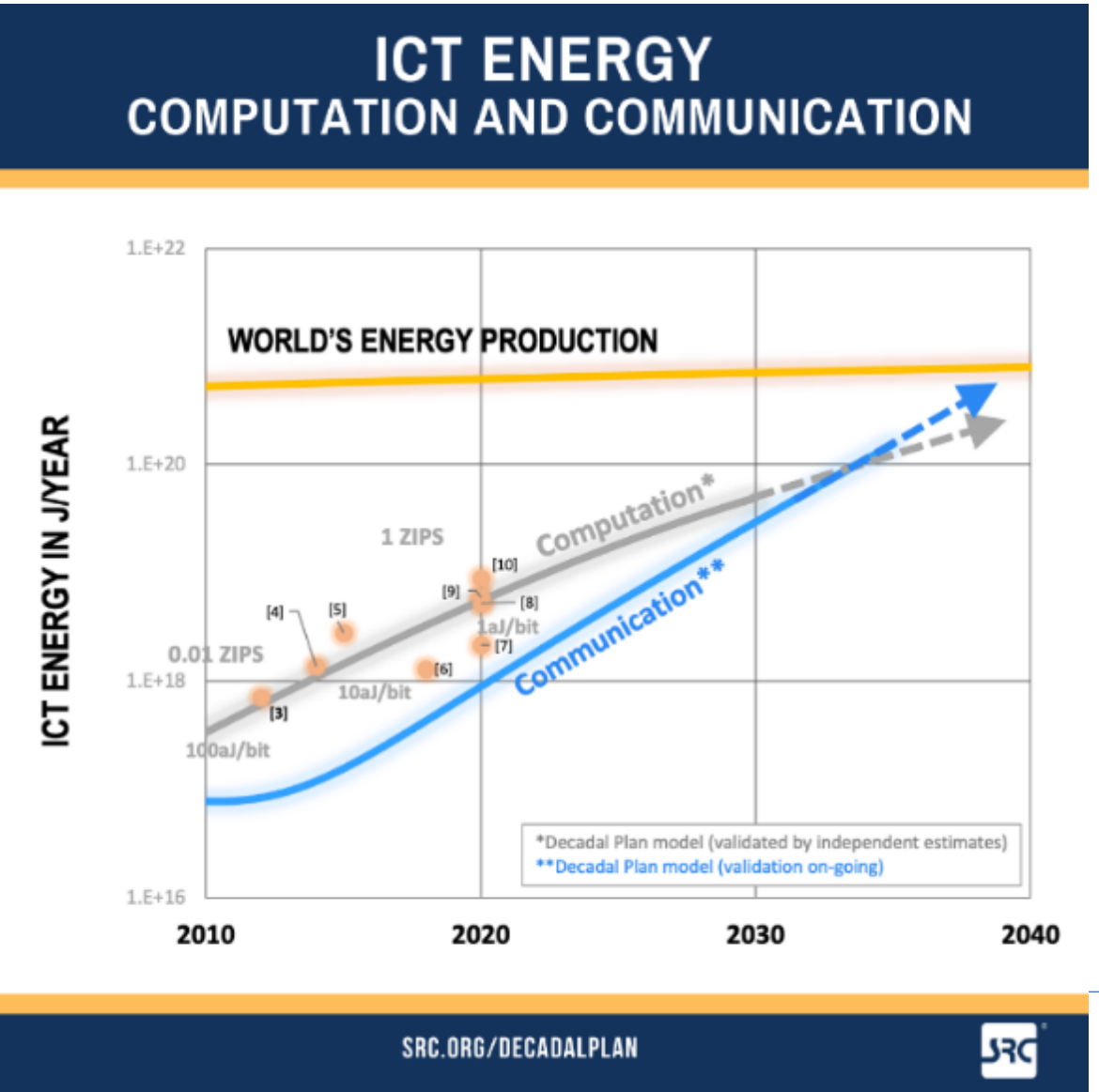
SIEMENS

FUJIFILM

مبادلة
MUBADALA

SRC

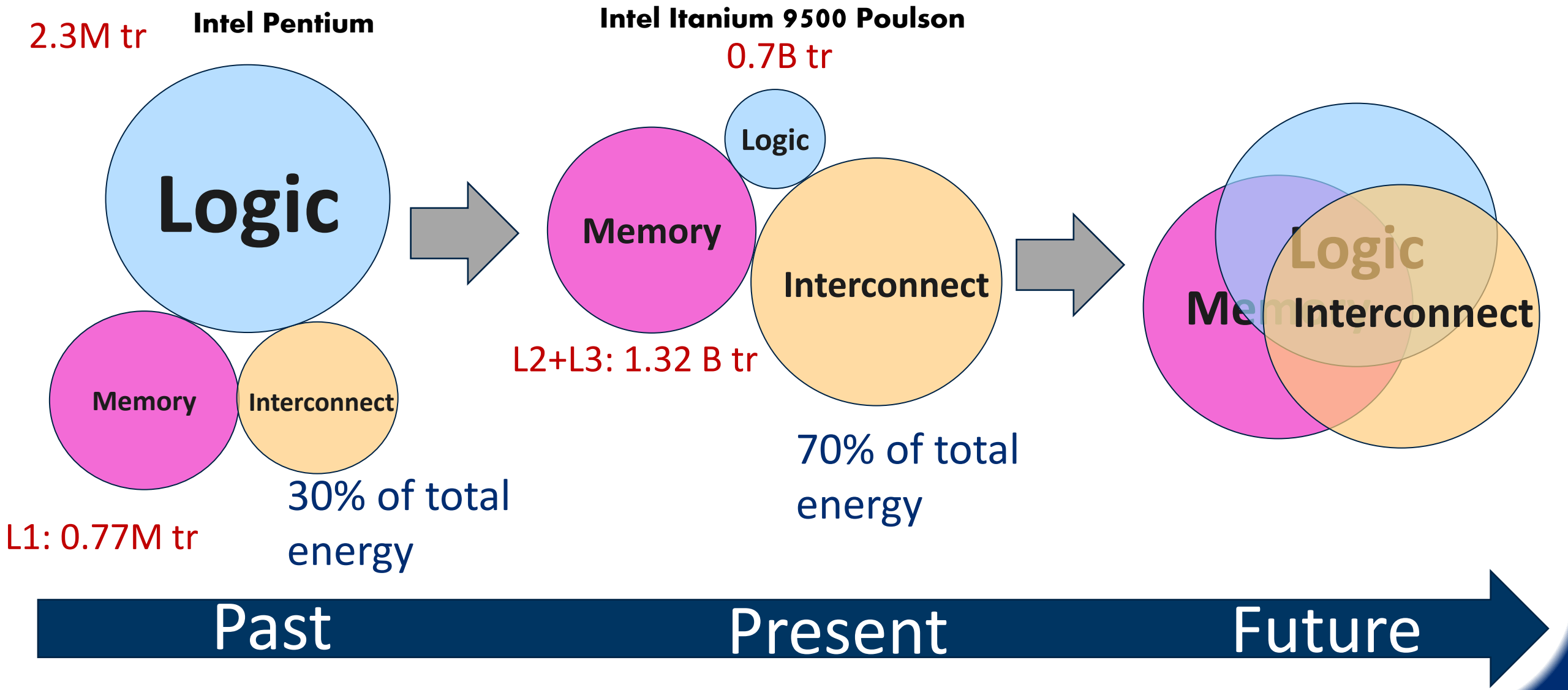
Compute Energy Challenge



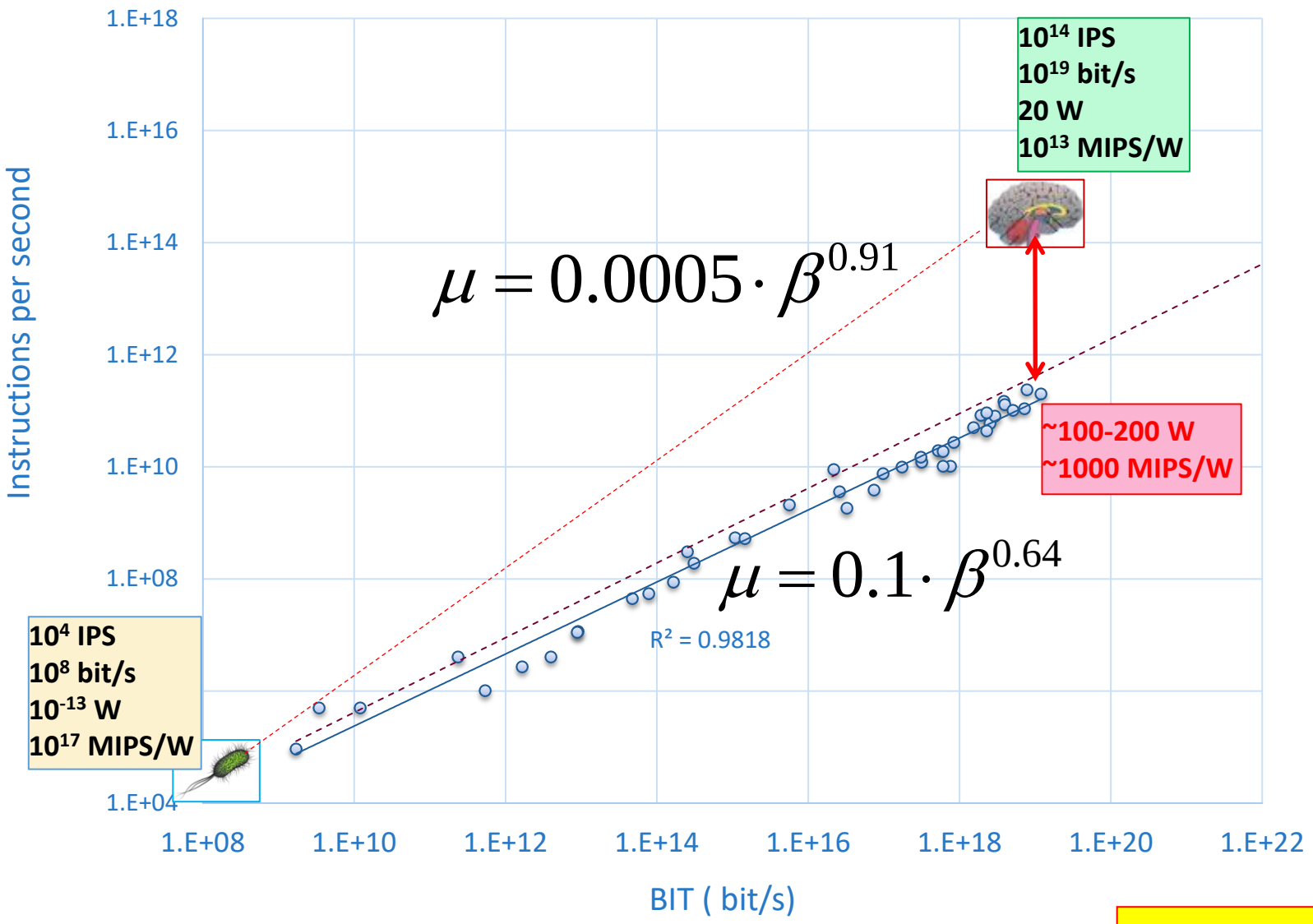
$$MIPS = k\left(BITS\right)^{p}$$

- Discover compute trajectories with $p \sim 1$
- How do we get from ~2/3 to 0.9 or 1?
- What "silicon" solutions can push the coefficient toward 1?

Energy consumption by three cornerstones of CPU



Computations vs. binary transitions



Estimates of computational power of human brain:

Binary information throughput:

$\beta \sim 10^{19}$ bit/s

Gitt W, "Information - the 3rd fundamental quantity", Siemens Review 56 (6): 36-41 1989

(Estimate made from the analysis of the control function of brain: language, deliberate movements, information-controlled functions of the organs, hormone system etc.

Number of instruction per second

$\mu \sim 10^{8}$ MIPS

H. Moravec, "When will computer hardware match the human brain?" J. Evolution and Technol. 1998. Vol. 1

(Estimate made from the analysis brain image processing)

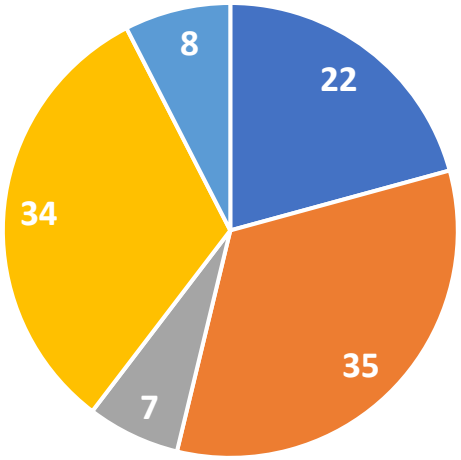
Alternative trajectory may exist!

Summary

- On March 1st, we released the Interim Report for the Microelectronic and Advanced Packaging Technologies Roadmap (MAPT)
  - an industry-wide initiative of major impact on the semiconductor industry
  - introduces a new comprehensive Roadmap to guide the forthcoming microelectronic revolution, like the ITRS has served in the past.
- The MAPT Roadmap manifests the transition from
  - a two-dimensional (2D), smaller-transistor-centric paradigm to
  - a universal 3D and heterogeneous integration microelectronics platform
    - seamless integration of multiple electronic, photonic, micromechanical, etc. chiplets
- Needed: 3D-IC platform for multi-chiplet system design and advanced packaging
  - Advanced packaging is new king of microelectronics!
- The MAPT Roadmap supports the 2030 Decadal Plan for Semiconductors
  - projects 10-15 year targets and timelines highlighting possible solutions for the identified targets including
    - Semiconductor Manufacturing Technologies
    - Environmental sustainability
    - Workforce Development

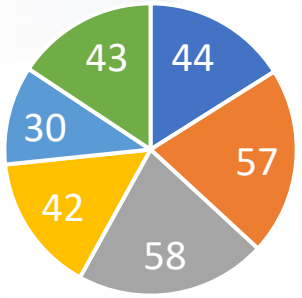
MAPT Summary

Total Organizations **106**



- SRC Members
- Universities
- Government
- Other Industry

TWGs by numbers



- TWG A: Workforce Development
- TWG B: Application Drivers & System Requirements
- TWG C: Advanced Packaging & Heterogeneous Integration
- TWG D: Digital Processing
- TWG E: AMS Processing
- TWG F: Photonics & MEMS

MAPT Summary

University (US) - 29

- Arizona State University
- Binghamton University
- Clarkson University
- Darthmouth college
- Duke University
- Georgia Institute of Technology
- Howard University
- Iowa State University
- Mass. Institute of Technology
- Morgan State University
- NC A&T State Univesity
- North Carolina State University
- Oregon State University
- Pennsylvania State University
- Purdue University
- Rochester Institute of Technology
- Stanford University
- SUNY Polytechnic Institute
- University of California, San Diego
- University of California, Irvine
- UCSB
- UCF
- University of Florida
- U Illinois, Urbana-Champaign
- University of Michigan
- University of Minnesota
- University of Notre Dame
- University of Texas, Dallas
- Washington State University

Industry - SRC Member - 22

- ASM
- Advanced Micro Devices, Inc.
- Analog Devices, Inc.
- Applied Materials, Inc.
- Arm
- Boeing
- GlobalFoundries Inc.
- IBM Corporation
- Intel Corporation
- MediaTek, Inc.
- Micron Technology, Inc.
- Mubadala Technology
- Northrop Grumman
- Qualcomm
- NXP Semiconductors
- Raytheon Technologies
- Samsung Electronics Co., Ltd.
- Siemens EDA
- SK hynix Inc.
- Texas Instruments Incorporated
- Tokyo Electron Limited (TEL)
- TSMC

University (Int'l) - 6

- Indian Inst. of Tech./Kanpur
- KAUST
- Khalifa University
- University of Guelph
- University of Sheffield
- University of Toronto

Industry - Other - 33

- 3D Glass Solutions
- Ansys
- Amazon
- Bosch
- Broadcom
- Cadence
- Cardea Bio
- Cirrus Logic
- Cisco Systems, Inc.
- eFabless
- Electronic Innovations
- Entegris
- Google
- Hewlett Packard Enterprise
- Kepler Computing
- Lumoniq
- Memcus
- Microsoft
- MITRE
- Nokia
- Rigaku
- Silicon Intervention Inc.
- Si Ware Systems
- Skywater Technologies
- Softmems
- Synopsys, Inc.

Industry - Other – 33 (con't)

- Tower Semiconductor
- Twist Bioscience
- Uhnder
- Western Digital Corporation
- X-Celeprint
- Zero Asic

Government (Agencies/National Labs) - 7

- DARPA
- Los Alamos National Laboratory
- NIST
- Oak Ridge National Laboratory
- Pacific Northwest National Laboratory
- Sandia National Laboratories
- SLAC

Associations/Societies - 8

- America's Frontier Fund
- IMEC
- Innovation Impact Partners
- IPC
- Materials Research Society
- Razdan Research Institute
- SEMI
- Semiconductor Research Corporation

Total Organizations: 106