What really is Heterogeneous Integration?

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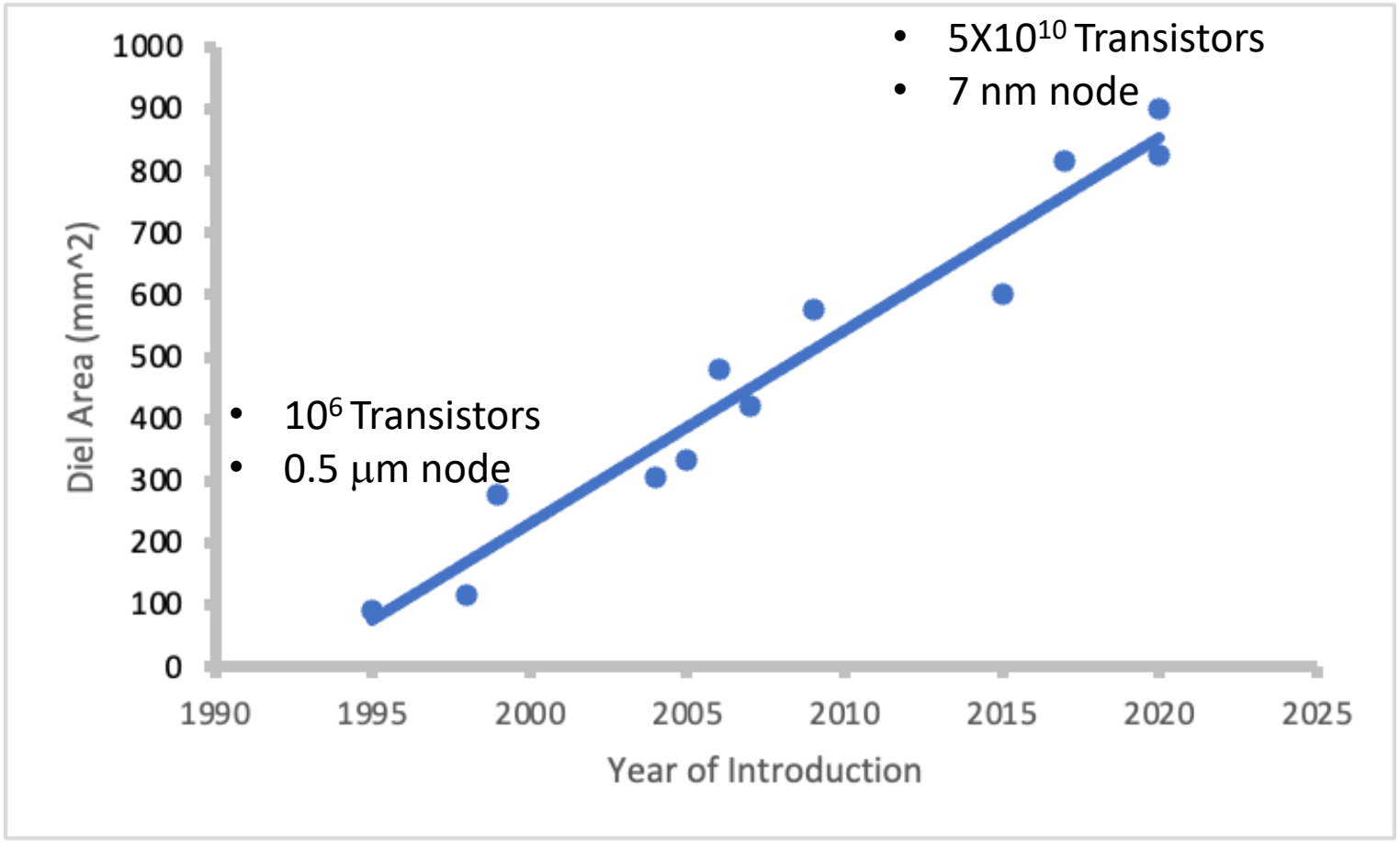
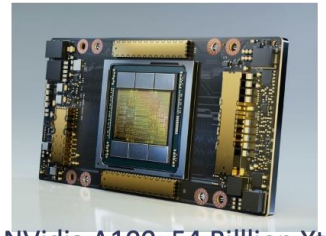
UCLA CHIPS

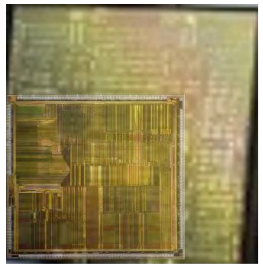
A UCLA partnership to develop applications, architectures, design methodologies, enablement, design, devices and core technologies and the eco-system that create and leverage advanced packaging and **develop our students & scholars to lead this effort in the real world**

Simplify hardware development through novel architectures, integration methods, technologies, and devices.

Transistors are shrinking but die sizes are increasing !



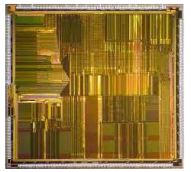




NVidia A100: 54 Billlion Xtors - 826 mm² (2020)
In TSMC 7 node

17,000 more transistors

Intel Pentium cpu ~300mm²
-3.1 Million Xtors (1993)
0.8 µm technology



More cores, more cache, larger workloads

But mainly because monolithic chips outperform multi-die packaged chips

This is driven by slow package scaling

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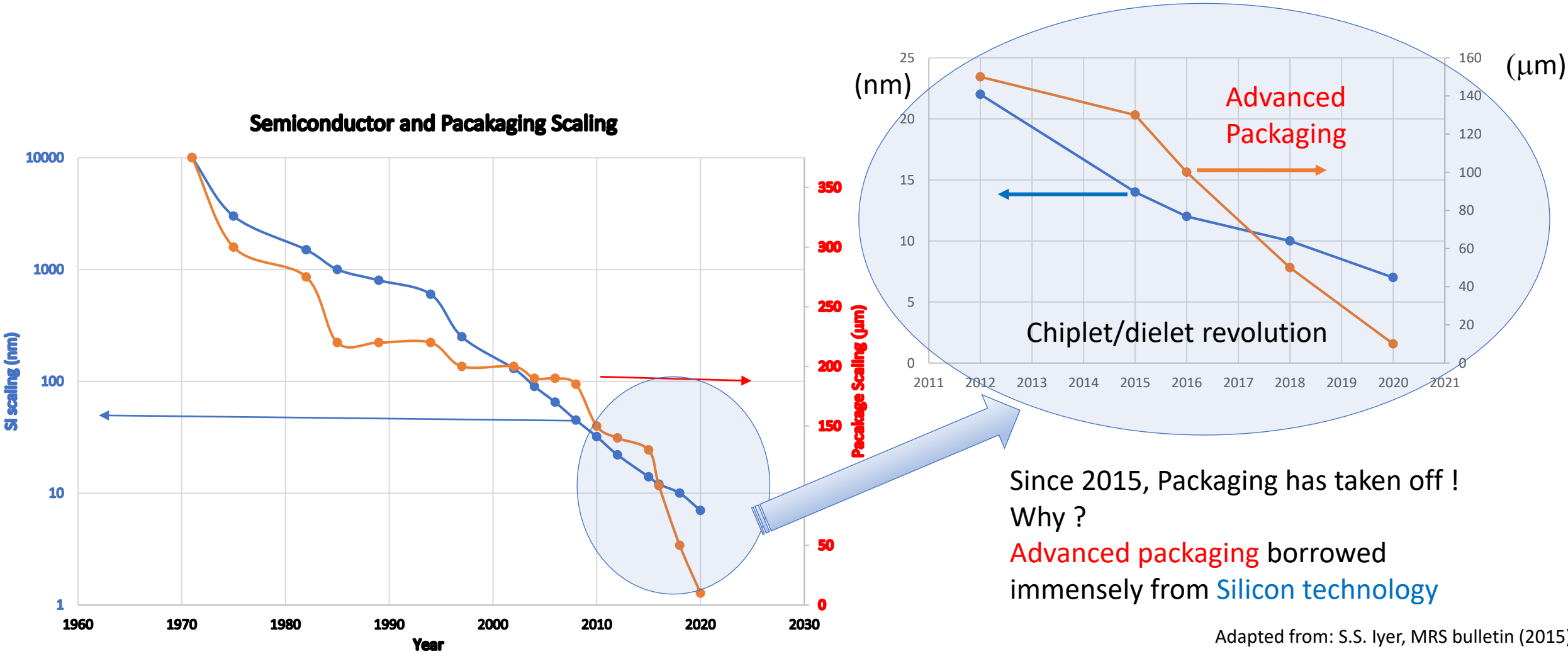
Silicon and Package scaling



Since 2015, Packaging has taken off !
Why ?
Advanced packaging borrowed immensely from Silicon technology

Adapted from: S.S. Iyer, MRS bulletin (2015)

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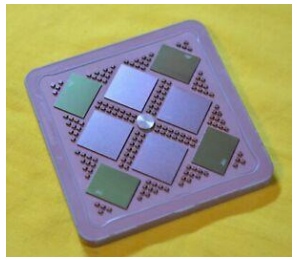
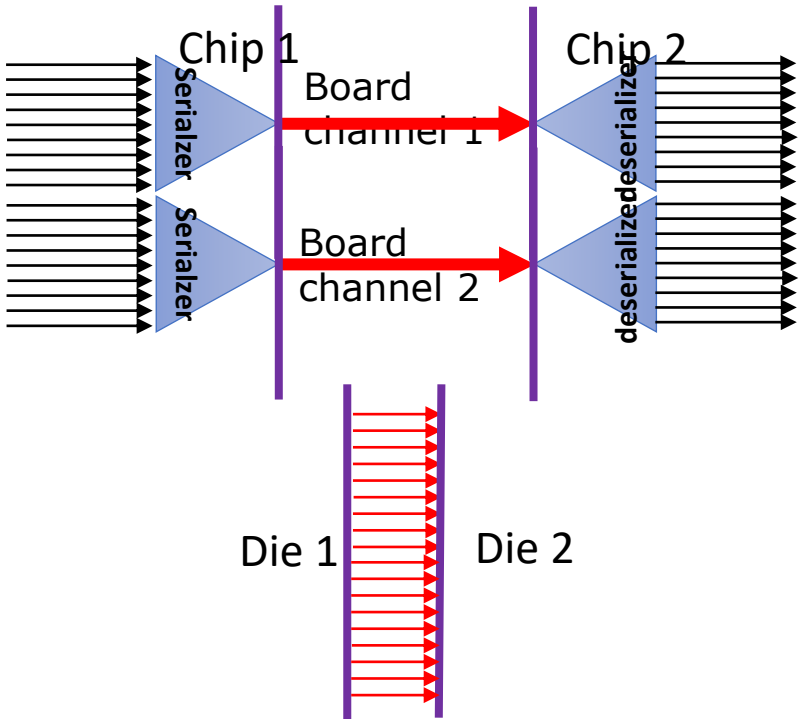
Heterogeneous Integration is Not New !





What is different now is scale:

- Finer pitch connections
- Finer traces
- Tighter inter- die spacings
- Simpler I/Os

How do you make the package behave like a monolithic solution ?

These dimensions must approach monolithic dimensions

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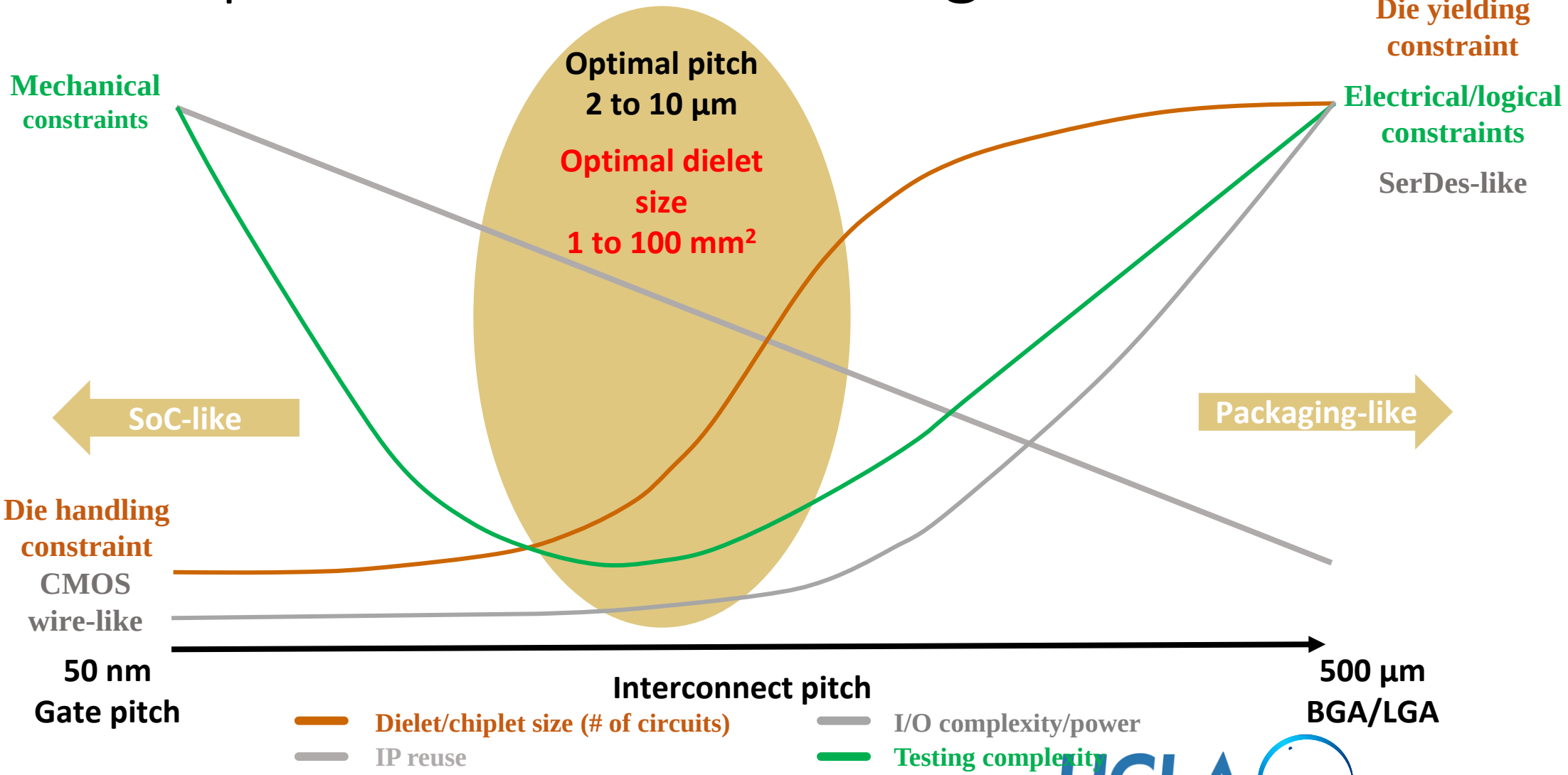
The Chiplet/Dielet Golden Regime



Iyer et al (2019)

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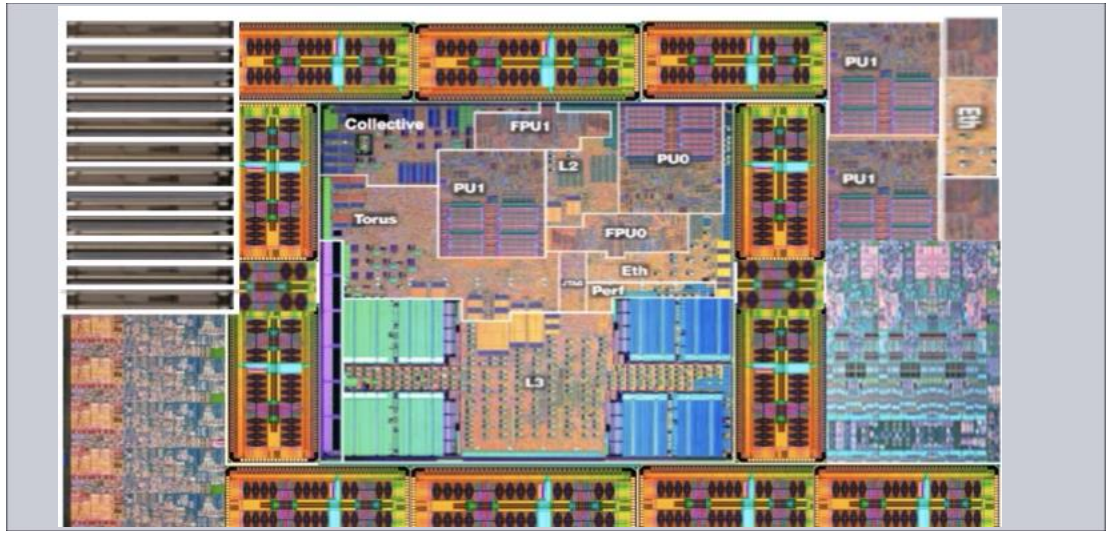
These new paradigms are changing the way we put complex systems together

- System is disaggregated into chiplets
- Bare dielets are stocked
  - Requires a dielet marketplace
- A few chiplets will need to be designed
  - Much more contained and will add to the dielet marketplace
- The interconnect fabric is designed
- Dielets are then assembled at fine pitch in an onshore secure facility



Time to market: less than 6 months

NRE: ~millions of dollars

1. S. S. Iyer, "Heterogeneous Integration for Performance and Scaling," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 6, no. 7, pp. 973-982, July 2016, doi: 10.1109/TCPMT.2015.2511626.

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Challenges of Heterogeneous Systems at Scale

Assembly Technology

- Substrate Technology
- Assembly: Fine pitch die-Substrate connections
- Passivation
- Assembling connectors for power and signal
- Assembling Thermal dissipation units

Assembly architectures

- Power delivery
- Heat dissipation
- Connectors
- Passives
- Test

Enablement

- Signaling Protocols for short and log haul
- Clocking
- EDA
- System disaggregation and reintegration
- Dielet marketplace
- Security and redundancy
- ESD and Test

Applications

- Graph processors
- Memory appliances
- mm wave and THz applications
- Medical applications

More in the Manufacturing Roadmap for Heterogenous Integration and Packaging (UCLA, SEMI -sponsored by NIST) (see the chips.ucla.edu webpage)

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US - Korea Collaborations

- Visiting Scholars from Korea:
  - Ji Won Shin (Samsung Packaging) spent a year in our Lab 2021-22
- Support through SRC funding (Samsung, SK Hynix)
  - Jump 1.0 Ascent Center
  - Jump 2.0 Chimes Center
- Some personal history on US-Korea collaborations
- We would welcome both industry and academic collaborations

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