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THE GEORGE WASHINGTON UNIVERSITY

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WASHINGTON, DC

# aJ/bit Modulators and Photonic Neuromorphic Computing

Volker Sorger

14<sup>th</sup> NSF–Korea Nanotechnology Forum 2017



# Orthogonal Physics Enabled Nanophotonics (OPEN) lab

Today

**Atto-Joule Optoelectronics**

Sorger, Zhang lab, *Nature Photonics* (2008)  
 Sorger, Zhang lab, *Nature* (2009)  
 Sorger lab, *IEEE Photonics* (2013)  
 Sorger lab, Altug lab, *Nature Nanotech.* (2015)  
 Sorger lab, Majumdar Lab, *Sci. Reports* (2016)  
 Sorger lab, *Optics Letters* (2016)  
 Sorger lab, *IEEE STQE* (2014 & 2017)

**Photonic Functions**

Sorger lab, *IEEE Photonics* (2015)  
 Sorger lab, *Nanophotonics* (2016)  
 Sorger lab, *Optics Letters* (2016)  
 Sorger lab, El-Ghazawi lab, *IPCC* (2017)  
 Sorger lab, El-Ghazawi lab, *Mircoprocess. & MS* (2017)  
 Sorger lab, *Frontiers in Optics* (2017)

**Analogue Computing**

Sorger lab, *Nanophotonics* (2017)  
 Sorger Lab, Grace lab, *Biofabrication* (2017)  
 Sorger lab, *IEEE Rebooting Computing* (2017)  
 Prucnal lab, Sorger lab, (in preparation)

# Modulators = Optical Transistors



- Contrast ratio

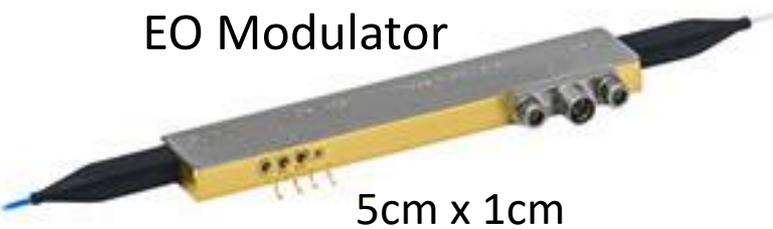
$$R_{on/off} = \frac{P_{out}(V_{off})}{P_{out}(V_{on})}$$

- Insertion loss

$$Loss = \frac{P_{in} - P_{out}(V_{off})}{P_{in}}$$

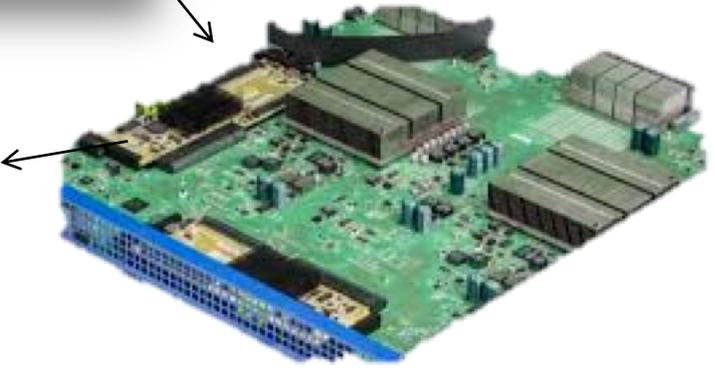
- Modulation efficiency

$$\frac{R_{on/off}}{\Delta V} \quad (=SS@FET)$$



EO Modulator

5cm x 1cm

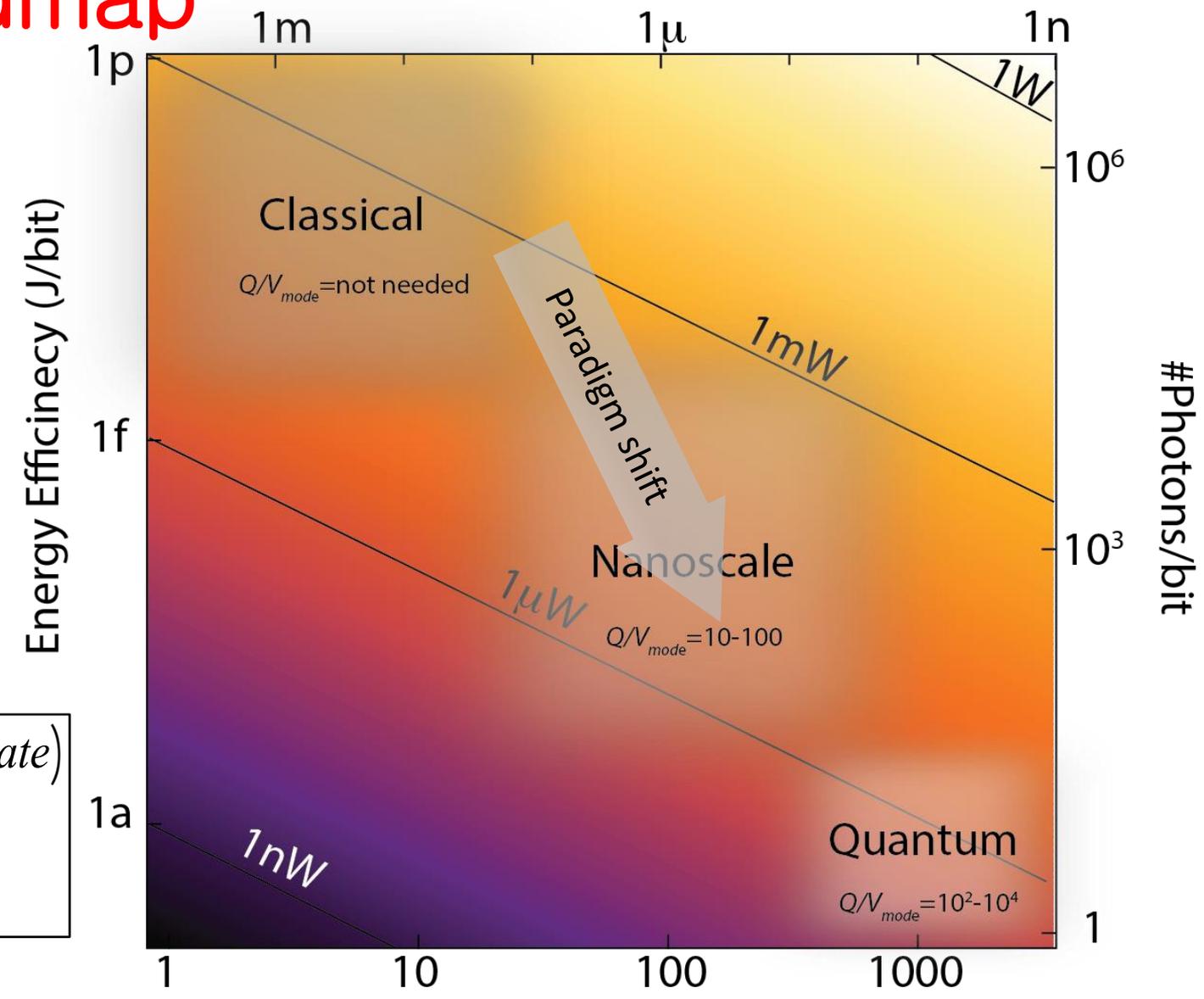




# Power-BW Roadmap

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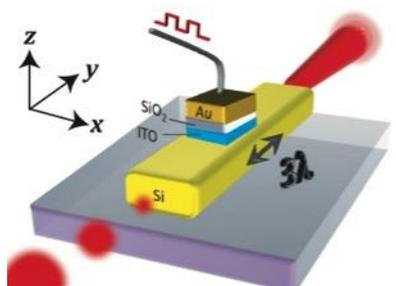
Device Length (m)



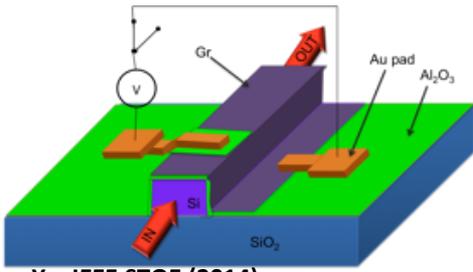
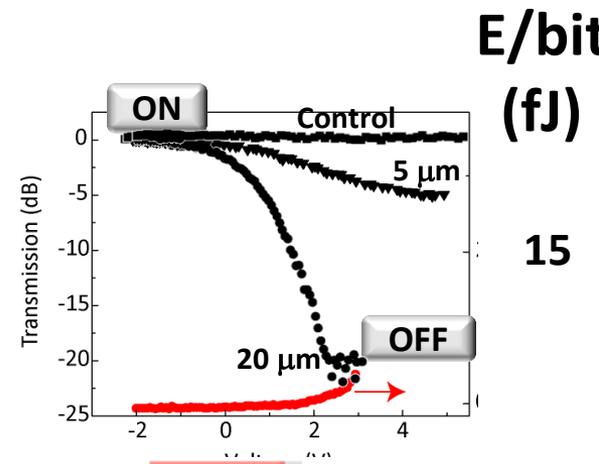
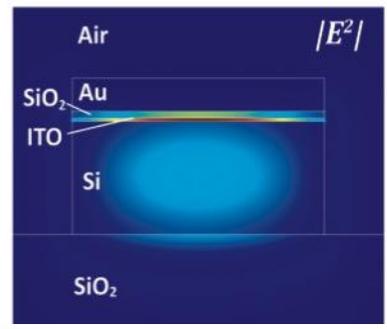
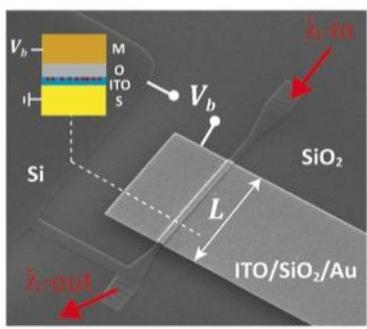
$$Power = (E/bit) \cdot (Bitrate)$$

$$\left[ \frac{J \text{ bit}}{bit \ s} = \frac{J}{s} = W \right]$$

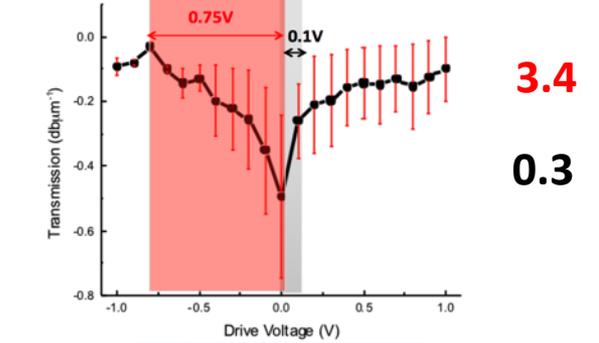
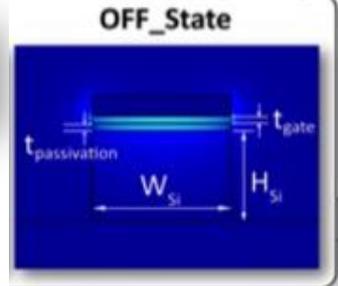
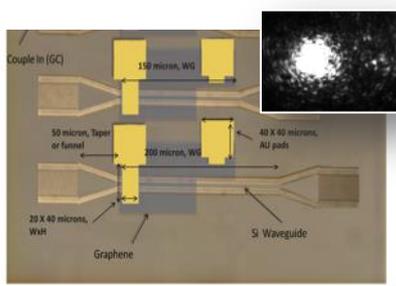
# GW EO Modulators



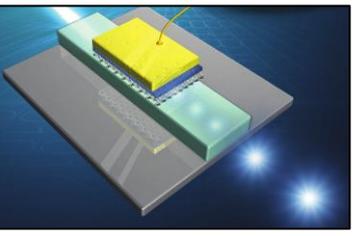
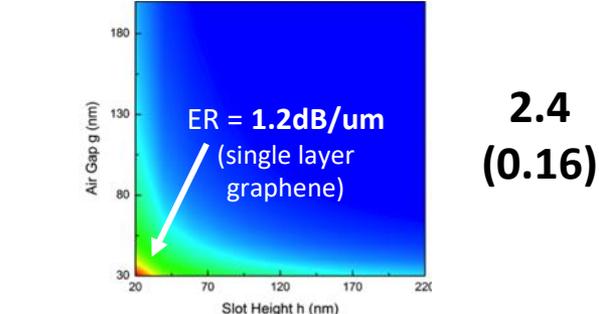
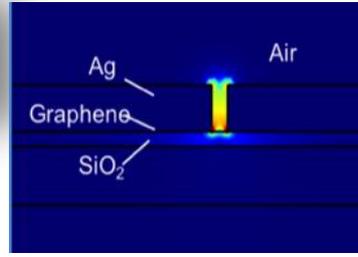
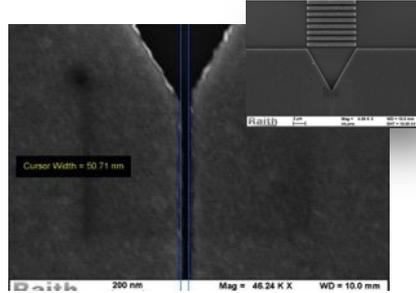
Sorger, Nanoph. (2012)  
Huang, IEEE Phot. (2013)



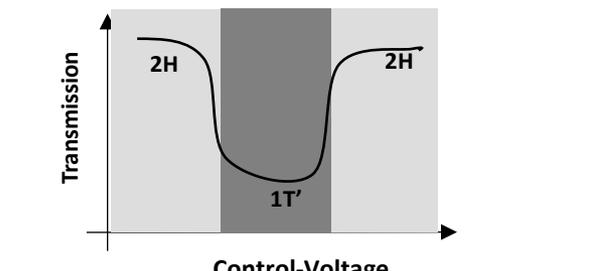
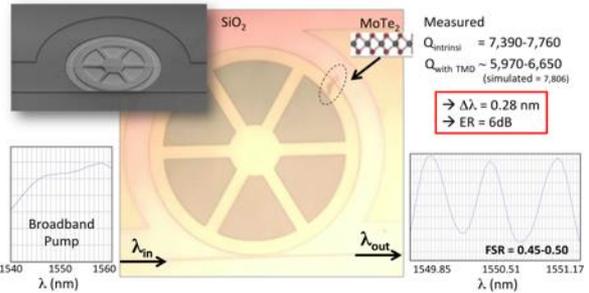
Ye, IEEE STQE (2014)  
Khan, (under review)



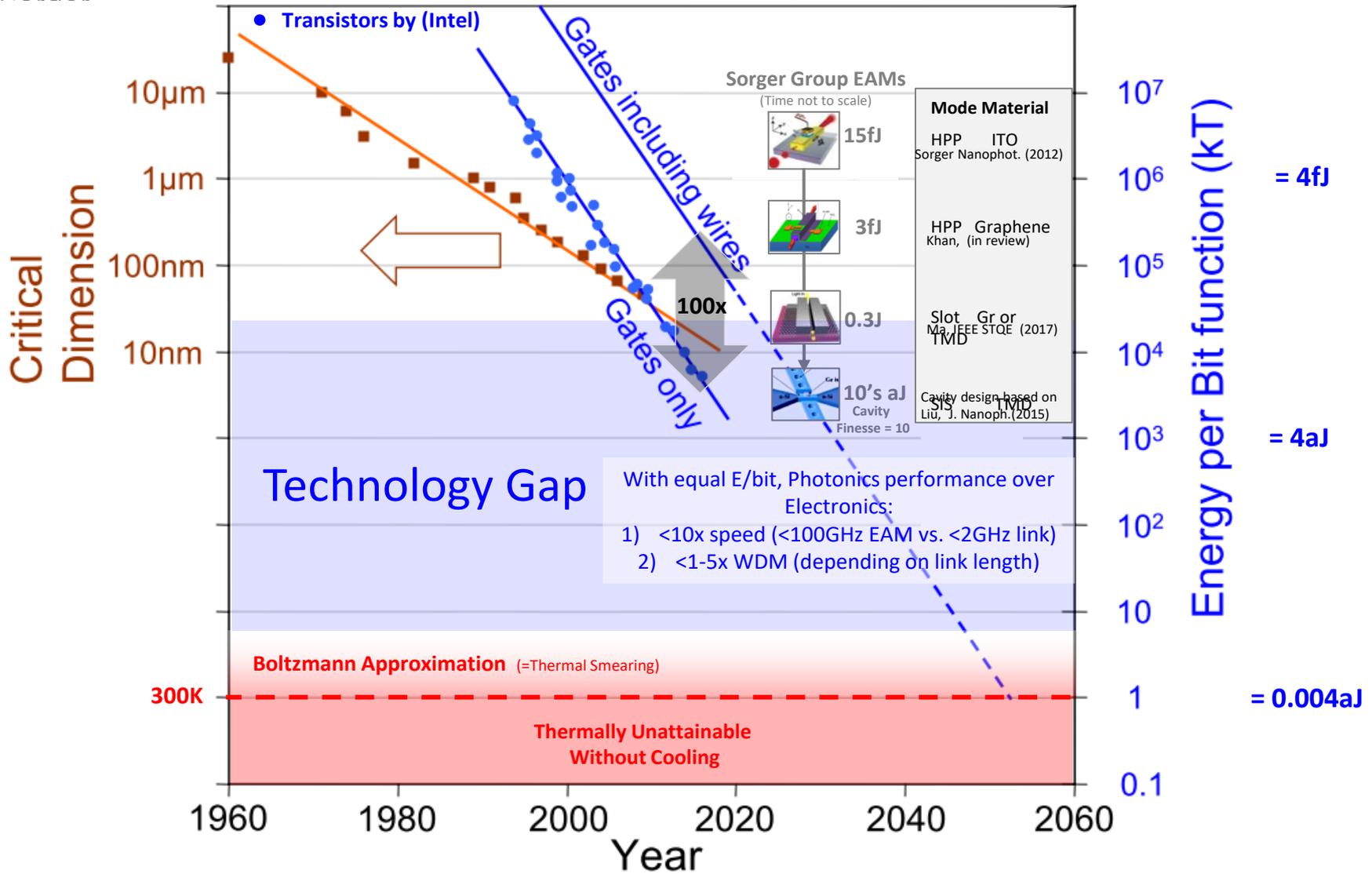
Ma, IEEE STQE (2017)



Sarpkaya, (in prep)

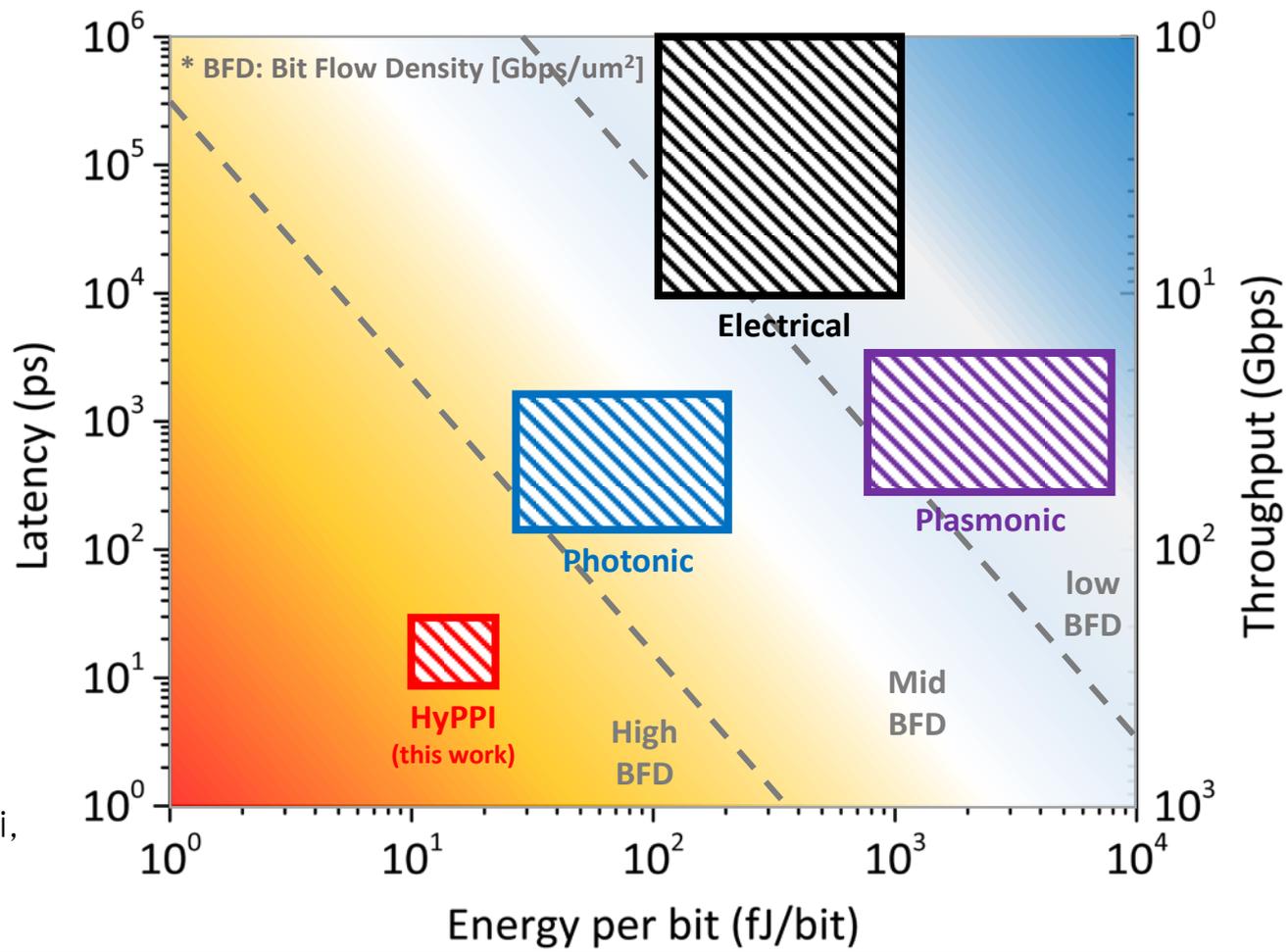


# E/bit Scaling: FET vs. EAM



# HyPPI. Hybrid Plasmon Photonics Interconnect

Chip-Scale Interconnect Performance



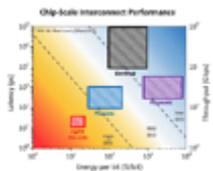
Sun, Badaway,  
Narayana, El-Ghazawi,  
Sorger, *IEEE  
Photonics*,  
7.6 (2015)

Physics & Material  $\leftarrow$  (E/bit)<sub>Device</sub>  $\leftarrow$  SNR @ Rx  $\leftarrow$  Desired BER

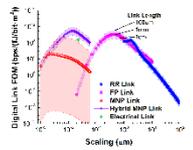
# Photonic Reconfigurable Computing

DEVICE  
LINK  
NETWORK  
SYSTEM & APPLICATION

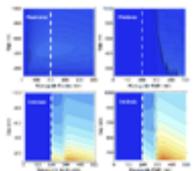
2015



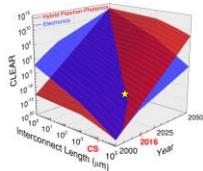
HyPPI



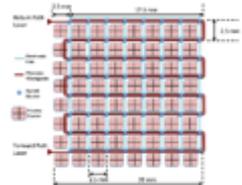
Fundamental Scaling Law



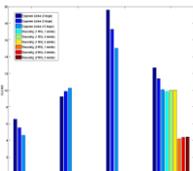
BFD



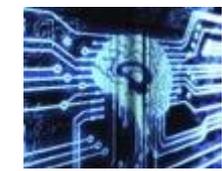
Link-CLEAR



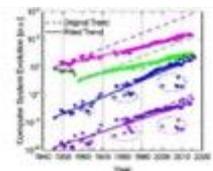
MorphoNoC



HyPPI NoC

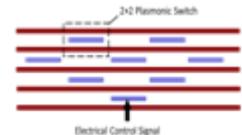


Dynamic-CHyPPI



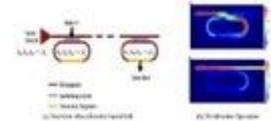
Universal CLEAR

2016

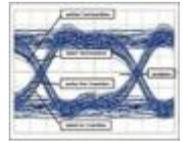


5x5 Optical Router

2017



MoDetector



Noise HyPPI

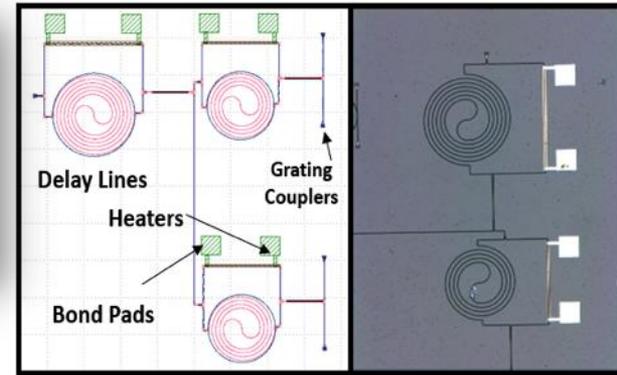
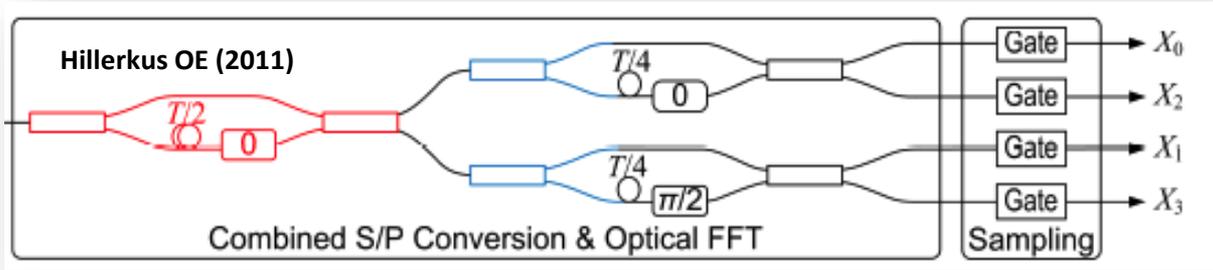


D-CHyPPI based Camera Sensor

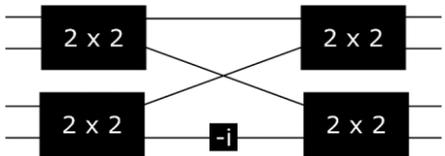


# Optical on-chip FFT

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## Cooley-Tukey Method



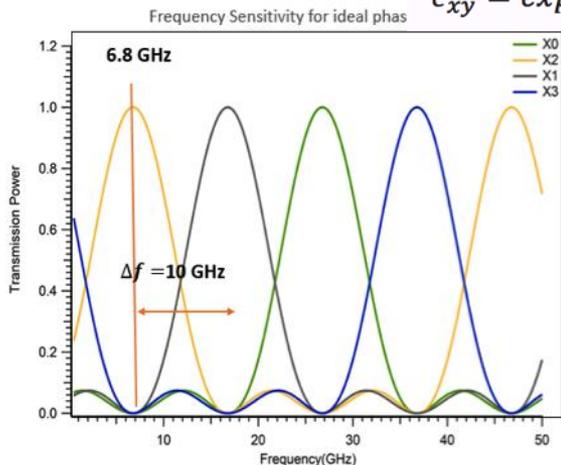
## Addition

$$\beta_1 = \frac{1}{\sqrt{2}}(-\alpha_1 + \alpha_2)$$

$$\beta_2 = \frac{1}{\sqrt{2}}(\alpha_1 + \alpha_2)$$

## Multiplication

$$\epsilon_{xy} = \exp(-i2\pi xy/N)$$

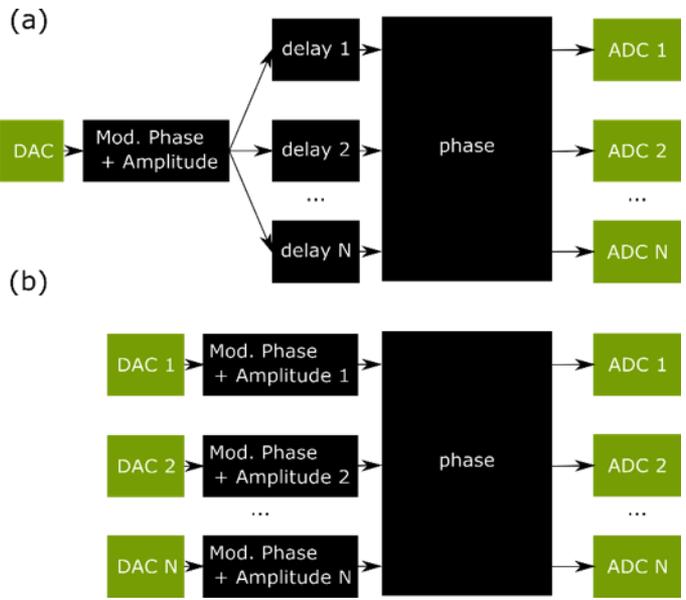
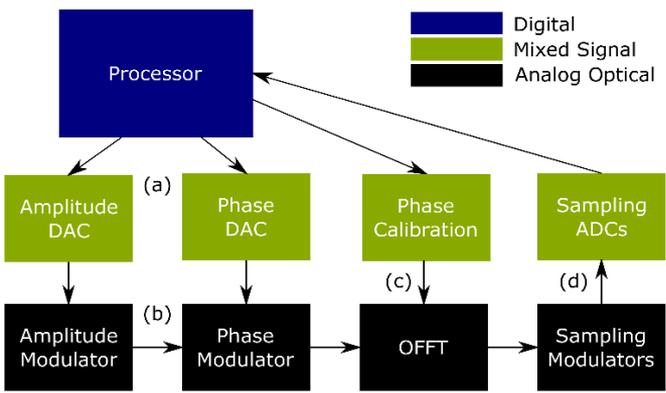


Metric	Electrical	OFFT (on-chip)
Operation Mode	Sequential	Continuous
Sampling Speed Device	GHz Slow ADC Conversion	10-100GHz short sampling window
Data BW	<10GFlop/s <a href="http://fftw.org/speed/CoreDuo-3.0GHz-icc/">fftw.org/speed/CoreDuo-3.0GHz-icc/</a>	10-100Tbps
Power	High Example: N=8 ~10-100W	Low 0.1-10W
Data/Power [GFlop/W]	1 Max 10 = CPU 'wall'	10 <sup>3</sup> -10 <sup>5</sup> Assumed: 1Flop = 1 GHz
N Scaling	N <sup>2</sup>	#Phases (physical arms) N - 1 #Coupler = Complexity (C) C <sub>DI</sub> = 2(N - 1)
GVD (Group Velocity Dispersion)	N.A.	Low

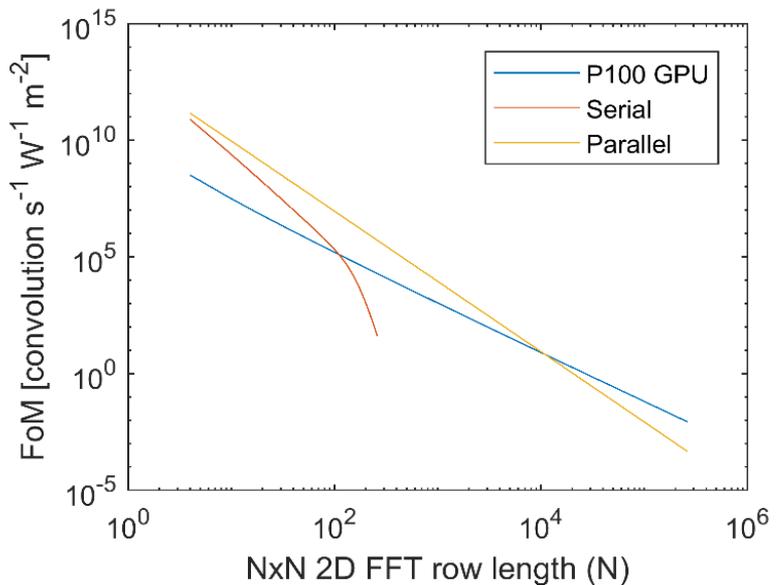


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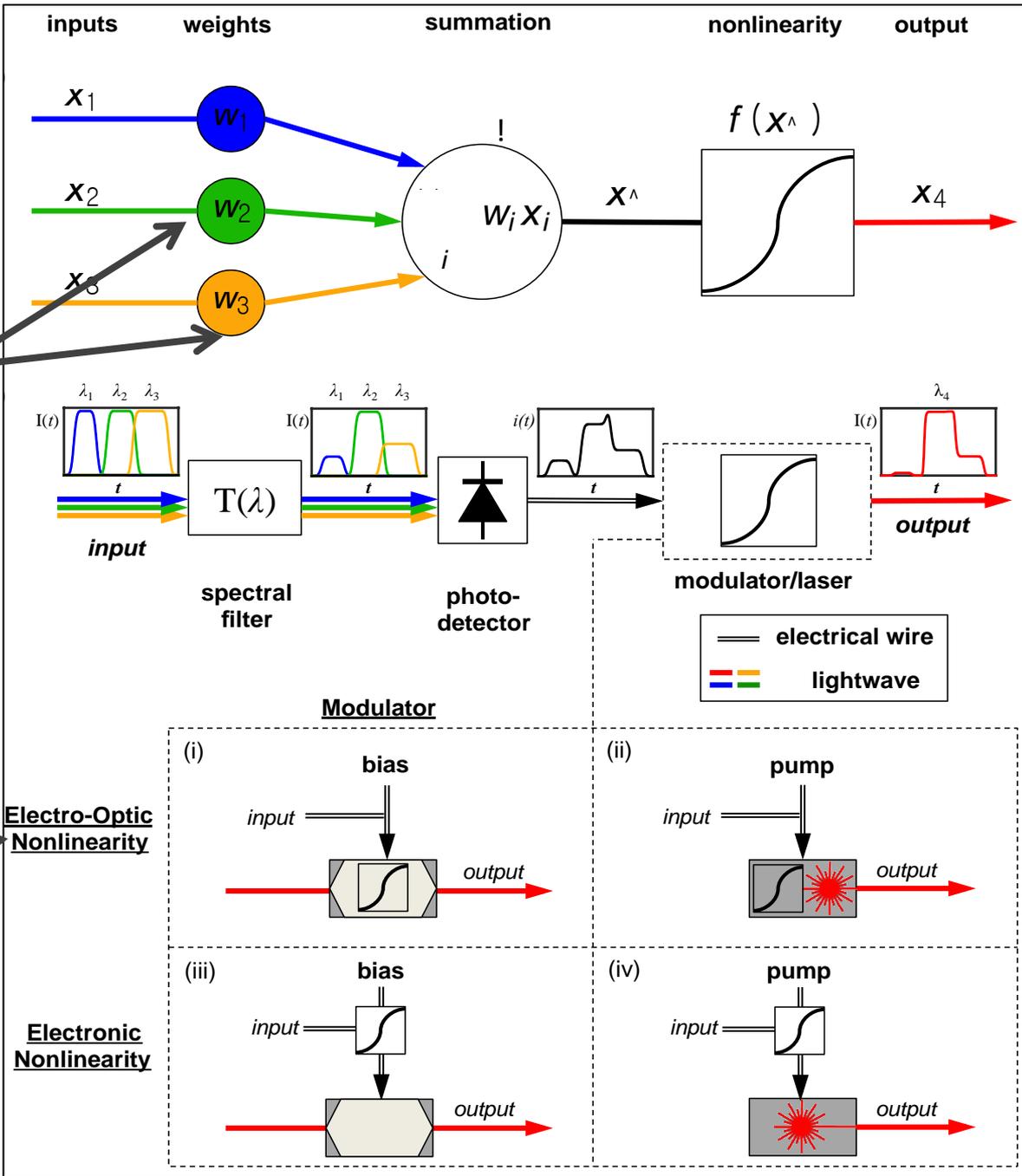
# Convolutional Neural Networks based-on Optical FFT



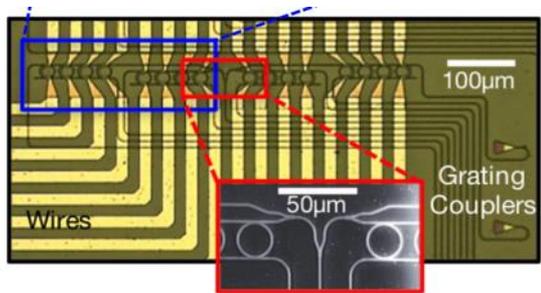
Description	Assumption
FLOPS per convolution	$20N^2 \log_2(N) + N^2$
ADC	56 GSa/s @ 2 W
DAC	100 GA/s @ 2.5 W
Optical loss first spiral	0.686 dB
Optical loss modulator	3.49 dB
Optical loss 2 x 2	0.99105 dB
Optical loss splitter	3 dB
Optical loss input grating coupler	4 dB



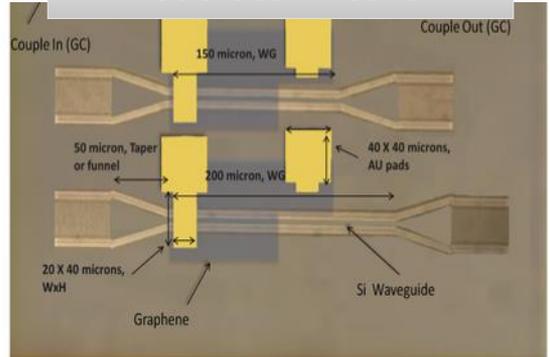
# Example: *Photonic Analogue Perceptron*



**Weight Bank = Partial Drop-Filter**



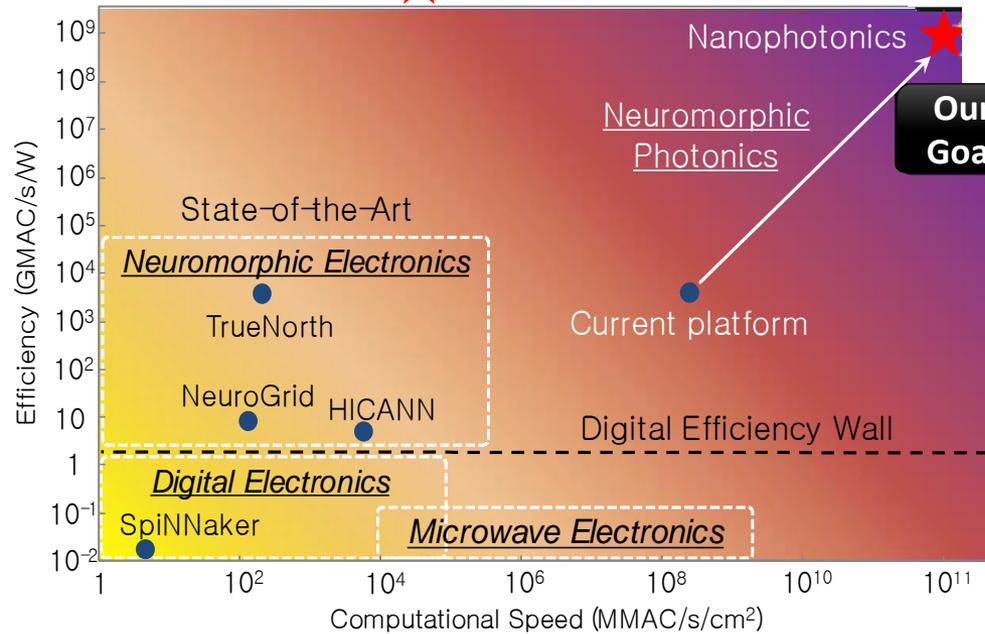
**Modulator Neuron**



# Neuromorphic Photonics

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★ = 1 GMAC/s/nW @  $1 \times 10^8$  GMAC/s/cm<sup>2</sup>



## Vector Multiply Weighted Additions

For B. MAC/s per Neuron

$$\#MAC/s/neuron = N_{FI} \cdot f_{3dB},$$

$$f_{3dB} = (2\pi R_b C_{mod})^{-1}$$

Computational Efficiency = J/MAC

$$\eta_{MAC} \equiv \frac{\#MAC/s/neuron}{P_{total}/neuron} \leq \eta \cdot \left[ \frac{N_{FI}}{N_{FO}} \right] \cdot \frac{e}{4h\nu} (V_{\pi} C_{mod})^{-1}$$

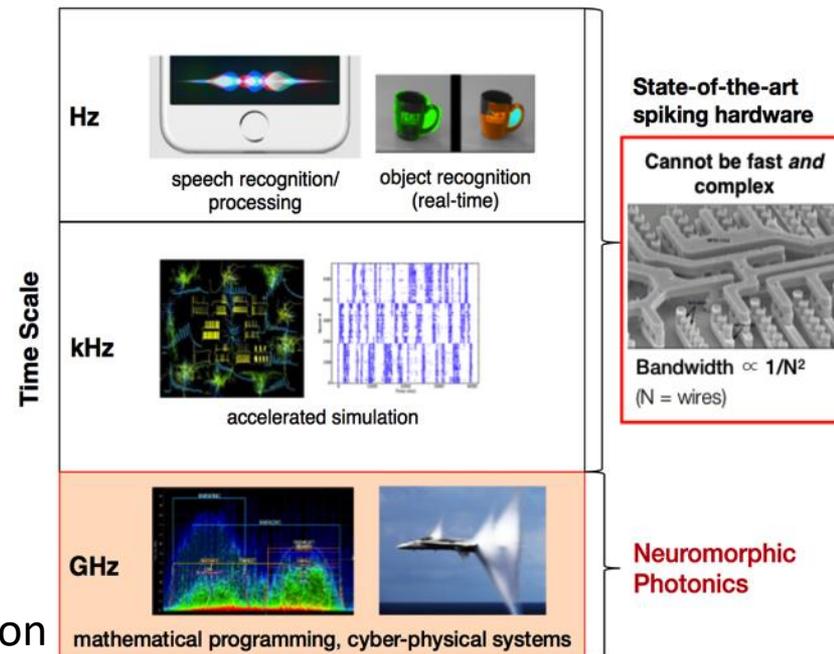
Goal: 1GMAC/nJ  $\rightarrow V_{\pi} C_{EOM} = 1-10aC$

## Implementation Options

- A. **Spiking** photonic laser neurons on III-V platform
- B. **Perceptron** photonic neurons on Si platform

## Applications

- Deep-Learning
- Real-time
- Non-linear Optimization



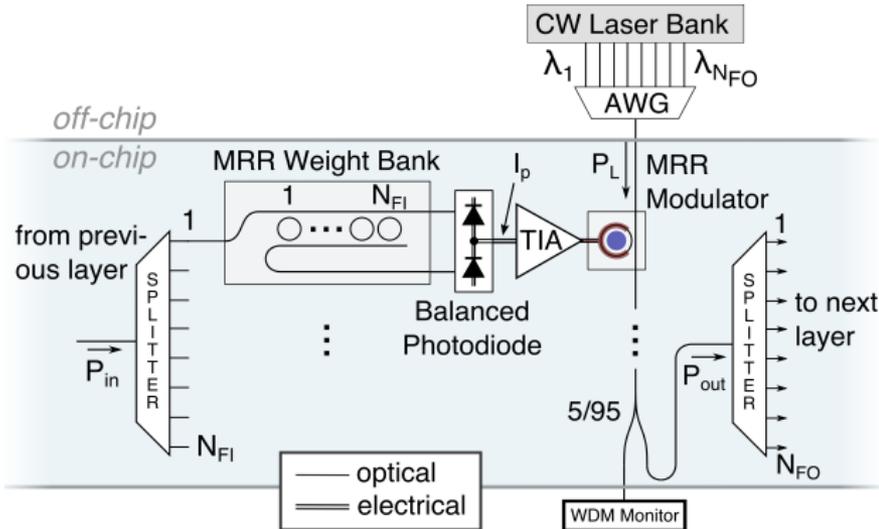


# Neuromorphic Performance

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## Deep Learning

Reference	Efficiency (J/MAC)	Speed (MAC/s)
NVIDIA GPU [15]	$3.4 \times 10^{-7}$	$1.7 \times 10^7$
AlexNet FPGA [16]	$2.6 \times 10^{-10}$	$6.2 \times 10^{10}$
UPSIDE Crossbar [17]	$1.3 \times 10^{-10}$	$4.0 \times 10^{10}$
UTK Analog Engine [18]	$1.0 \times 10^{-12}$	$11.8 \times 10^6$
IBM TrueNorth [19]	$2.6 \times 10^{-11}$	$1.3 \times 10^6$
<b>Nanophotonic Neuromorphic</b>	<b><math>7.4 \times 10^{-18}</math></b>	<b><math>2.0 \times 10^{17}</math></b>



## System Efficiency Vectors

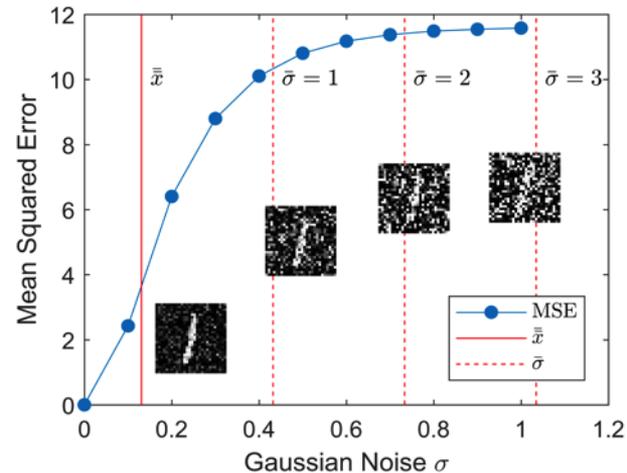
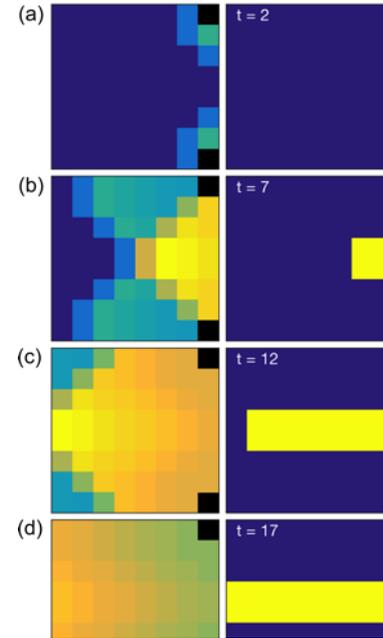
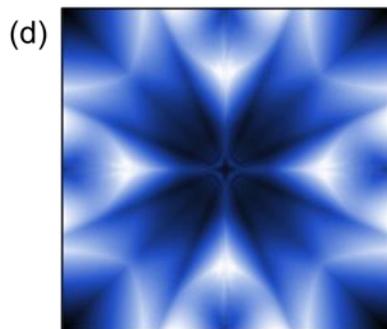
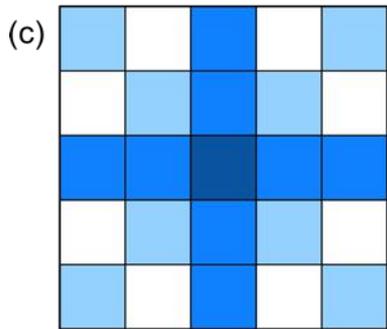
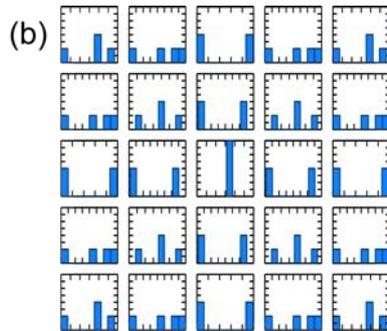
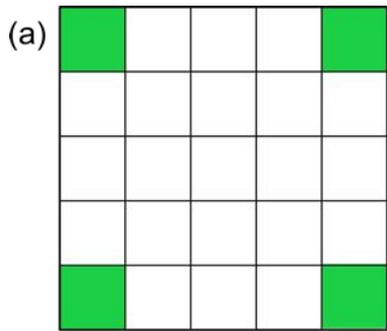
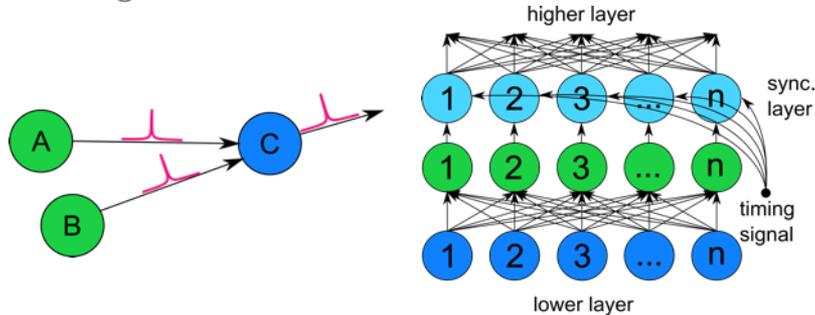
Technology	Limitation	$C_{total}$ (fF)	Quantum Efficiency	$E_{MAC}$
Silicon photonics (Eq. 1)	Gain	47	7%	5 pJ
Hybrid CMOS (Eq. 2)	Switching energy + noise	35	7%	2.1 fJ
<b>Nanophotonics (Eq. 2)</b>	<b>noise</b>	<b>0.1</b>	<b>16%</b>	<b><math>7.4 \text{ aJ}^\dagger</math></b>

$$E_{MAC} \geq \underbrace{N_{\{Z\}}^{EQ}}_{\text{fan-out}} \cdot \underbrace{\frac{1}{\text{"pd"}\{Z\}}}_{\text{quantum efficiency}} \cdot \underbrace{\frac{2^{2N_b+1}}{1 - \{Z\}^2}}_{\text{noise and resolution}} \cdot \underbrace{\frac{h\langle \lambda \rangle}{N_{\{Z\}}^{EA}}}_{\text{photon energy/MAC}} + \underbrace{\frac{E_{bit}}{N_{\{Z\}}^{EA}}}_{\text{switching energy/MAC}}$$

## Comparison Neuromorphic Processors

Chip	MAC Rate/processor	Energy/MAC	Processor fan-in	Area/MAC ( $\mu\text{m}^2$ )	MAC Rate/ $\text{cm}^2$
Silicon Photonic (Princeton)	2 TMACs/s	5 pJ	56	20,000	$1 \rightarrow 10^{14}$
Hybrid CMOS-Silicon Photonics	2 TMACs/s	2.1 fJ	148	5,000	$4 \rightarrow 10^{14}$
<b>Nanophotonic (This Project)</b>	<b>2 TMACs/s</b>	<b>7.4 aJ</b>	<b>300</b>	<b>20</b>	<b><math>1 \rightarrow 10^{17}</math></b>
TrueNorth (Electronic) [13]	2.5 kMACs/s	26 pJ	256	4.9	$2 \rightarrow 10^8$

# Mirror Symmetry Density with Delay in Spiking Neural Networks



# OPEN Sorger Team

## Post Docs

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Prof. Reed (Stanford)  
Prof. Bartels (UCR)  
Prof. Lee (KU)  
Prof. Prucnal (Princeton )  
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Dr. Sadana (IBM Watson)  
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