Feature Extraction and Image analysis using memristor networks

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Memristor Based Neural Network Hardware

Synapse – reconfigurable two-terminal resistive switches

Goal: building bio-inspired, efficient artificial neural networks

Computing with Memristor Arrays

Memristors perform learning and inference functions

- Memristor weights form dictionary elements (features)
- Image input, Pixel intensity represented by widths of pulses
- Memristor array natively performs matrix operation
  \[ \vec{I} = \vec{v} \cdot \vec{\Phi} \]
- Integrate and fire neurons
- Learning achieved by backpropagating spikes

DARPA UPSIDE program
Neural Network for Image Processing based on Sparse Coding

1. Network adapt during training following local plasticity rules
2. FF weights form neuron receptive fields (dictionary elements)
3. Output as neuron firing rates

Cost Function:
\[ E(t) = \frac{1}{2} \| s(t) - \hat{s}(t) \|^2 + \lambda \sum_m C(a_m(t)) \]
Sparse Coding Implementation in Memristor Array

Forward Pass

Update neurons/activities

\[ y = p^T W \]

\[ \frac{du}{dt} = \frac{1}{\tau} (-u + p^T \cdot W - a \cdot (W^T W - I) ) \]

\[ \frac{du}{dt} = \frac{1}{\tau} (-u + (p - \hat{p})^T W + a) \]


Backward pass

Update residual

\[ \hat{p} = a W^T \]

Neuron membrane potential
Analog Oxide Memristors

- Resistive switching can be precisely simulated after considering $V_O$ diffusion, drift, and thermophoresis effects.

Simulation of Switching Process

- **Dependent variables**
  - $n_D$: Concentration of $V_o$ [cm$^{-3}$]
  - $T$: Temperature [K]
  - $\psi$: Potential [V]

- **Constants**
  - $a$: Hopping distance, 0.1 nm
  - $f$: Escape-attempt frequency, $10^{12}$ Hz
  - $E_a$: Diffusion barrier, 0.85 eV

- **Oxygen vacancy transport**
  - Eq.(1) $\frac{\partial n_D}{\partial t} = \nabla \cdot (D \nabla n_D - v n_D + D S n_D \nabla T)$

- **Current continuity**
  - Eq.(2) $\nabla \cdot \sigma \nabla \psi = 0$

- **Heat (Joule heating)**
  - Eq.(3) $- \nabla \cdot k_{th} \nabla T = J \cdot E = \gamma \cdot \sigma \left| \nabla \psi \right|^2$
    
    ($\gamma = 1$ for DC, and $\gamma = 2$ for AC simulation)

- **Parameters** - Eqs.(4)
  - $D = \frac{1}{2} a^2 f \exp(-E_a / kT)$: Diffusivity of $V_o$ [cm$^2$s$^{-1}$]
  - $v = a f \exp(-E_a / kT) \sinh(qaE / kT)$: Drift velocity of $V_o$ [cm/s]
  - $S = -E_a / kT^2$: Soret diffusion coefficient [1/K]

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Simulation of Filament Growth

- Same set of parameters can explain both DC and pulse response

Neuromorphic Hardware Implementation

- Checkerboard pattern
- 32 x 32 array
- Direct storage and read out
- No read-verify or re-programming

9 Training Images
128x128px
4x4 patches
127449 training patches (overlaps allowed)
Trained in random order

Image Reconstruction with Memristor Crossbar

PCA Analysis Using Memristor Arrays

Wisconsin Breast Cancer Data

- Sensory data from malignant or benign cells

<table>
<thead>
<tr>
<th>Feature</th>
<th>Training Set</th>
<th>Testing Set</th>
</tr>
</thead>
<tbody>
<tr>
<td>clump thickness</td>
<td>9</td>
<td>10</td>
</tr>
<tr>
<td>uniformity of cell size</td>
<td>5</td>
<td>10</td>
</tr>
<tr>
<td>uniformity of cell shape</td>
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<td>6</td>
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<tr>
<td>marginal adhesion</td>
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<td>3</td>
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<tr>
<td>single epithelial cell size</td>
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<td>3</td>
</tr>
<tr>
<td>bare nuclei</td>
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<td>10</td>
</tr>
<tr>
<td>bland chromatin</td>
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<td>3</td>
</tr>
<tr>
<td>normal nucleoli</td>
<td>9</td>
<td>5</td>
</tr>
<tr>
<td>mitoses</td>
<td>8</td>
<td>3</td>
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</tbody>
</table>

- Principal Component Analysis (PCA) for data clustering
- Unsupervised training using Sanger’s rule

\[ \Delta g_{ij} = \eta y_j (x_i - \sum_{k=1}^{j} g_{ik} y_k) \]

Training set: 100 points
Testing set: 583 points

Input voltage pulse:
- Amplitude: fixed
- Width: \( \propto \) the values from the data

Experimental Implementation

- 9x2 memristor array
- Unsupervised learning using Sanger's rule

\[ Δg_{ij} = \eta y_j (x_i - \sum_{k=1}^{j} g_{ik} y_k) \]

Experimental Implementation

Wisconsin Breast Cancer Data

**Before training**

- Successful clustering obtained after unsupervised learning (without knowledge of the labels)
- Decision boundary drawn in a 2\textsuperscript{nd}-step, supervised training process
- Classification accuracy $\sim 97\%$, same as ideal software simulation

**After 100 cycles of training, experimental results**

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Internal Dynamics at Different Time Scales

Microscopic physical processes during SET
(1) Ionization of metal atoms in AE (anodic dissolution)
(2) Metal ions hopping in dielectrics
(3) Metal ions attachment to existing clusters
(4) Nucleation of metal ions captured by (4.1) IE and (4.2)
(5) Metal atoms in nuclei are activated to ions
(6) Electron hopping from IE to Neutralize positive charge from metal ions

• Memristor offers interesting internal dynamics at different time scales, and can emulate synapse realistically

Implementing STDP (and Spiking Rate Dependent Plasticity) Naturally

Integrated Crossbar Array/CMOS System

- Low-temperature process, RRAM array fabricated on top of CMOS
- CMOS provides address mux/demux
- RRAM array: 100nm pitch, 50nm linewidth with density of 10Gbits/cm²
- CMOS units – larger but fewer units needed. 2n CMOS cells control n² memory cells

Towards Commercialization

- **CMOS** Compatible
- **3D** Stackable, Scalable Architecture – Low thermal budget process
- **Architectures** proven include multiple Via schemes and Subtractive etching
- **Crossbar Inc** founded in 2010, $85M VC funding to date
- **Commercial Products** offered in 2016 based on 40nm CMOS
A reconfigurable hardware system with dense local connections and modular, asynchronous global connections

- Possibly FPGA-like modules, each module can be configured as a network with both feed-forward and feedback (recurrent) connections
- Spike based system with address-event coding
- Hierarchically structured interconnects: locally dense connection + globally asynchronous serial link
- “self-organized” computing modules at both fine-grained and coarse-grained levels
- Dynamically reconfigurable to adapt to the input data and the given problem (the “context”)

“General” purpose by design: the same hardware supports different tasks – image, video, speech, …

• Dense local connection, sparse global connection

• Run-time, dynamically reconfigurable. Function defined by software.
Summary

• Memristor arrays can already perform efficient image analysis and data clustering applications

• Taking advantage of the internal ionic dynamics at different time scales allow the device to more faithfully emulate biological system

• Memristor technology is already quite mature, especially for memory applications (products available)

• Towards dynamically reconfigurable circuits (i.e. software-defined chips) based on a common physical fabric
Acknowledgements

Grad students:
Jihang Lee, Wen Ma, Fuxi Cai, Yeonjoo Jeong, Jong Hong Shin, John Moon, Billy Schell, SeungHwan Lee, Qiwen Wang, Fan-Hsuan Meng

Former students
*Sung-Hyun Jo, *Kuk-Hwan Kim
*Siddharth Gaba, *Ting Chang

PostDocs:
Dr. Mohammed Zidan,
Dr. Xiaojian Zhu
Dr. Piotr Ogrodnik

*Dr. Yuchao Yang
*Dr. Sungho Kim
*Dr. Bing Chen
*Dr. Taeho Moon
*Dr. Zhongqing Ji
*Dr. Qing Wan
*Dr. L. Liu
*Xiaojie Hao

Funding:
• DARPA UPSIDE program
• National Science Foundation (ECS-0601478, CCF-0621823, ECCS-0804863, CNS-0949667, ECCS-0954621).
• DARPA SyNAPSE program
• Air Force MURI program, Air Force q-2DEG program
• Engineering Translational Research (ETR) Grant