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Byoung Hun Lee received B.S., M.S. in Physics from Korea Advanced Institute of Science and Technology in 1989, 1992 respectively and a Ph.D degree in the electrical and computer engineering from the University of Texas at Austin, Austin, Texas, USA in 2000. He became a senior member of IEEE in 2004.

He joined the School of Material Science and Engineering at Gwangju Institute of Science and Technology (GIST) in 2008. His current research focuses on the extreme low power device technology using various novel devices, reliability evaluation and electrical characterization methods for highly scaled silicon devices and photonic devices using a graphene.

Prior to join GIST, He worked as a manager for emerging technology program at SEMATECH from 2007 after managing an advanced gate stack program for 4 years as an IBM assignee to SEMATECH. He also served as a co-director of FEP transition center for advanced gate stack technology, jointly funded by SEMATECH and SRC during 2004-2006. Before assigned to SEMATECH, he worked as a lead integrator for 65nm high performance FEOL integration project at IBM, East Fishkill from 2000. He also worked for SAMSUNG Electronics from 1991-2000.

He is serving as a member of technical committee for symposium on VLSI Technology and has severed for numerous technical meetings such as VLSI-TSA, SSDM, ISIF, IRPS, IMRS, ISAGST, IIRW, IWDTF. He is an editorial board member for Scientific Reports and Electronic Material Letters. He has published more than 216 journal papers and 370 conference papers with citations over 5500 and H-index=37.