2D FETs with MoS$_2$, WSe$_2$, and black phosphorous toward practical electronics

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Introduction

The most widely studied 2-D material
Conical Dirac spectrum
Energy states without a bandgap
High mobility (< 100000cm²/Vs)
More conductive than copper
Attractive optical phenomena

More Flexible than rubber
Stretchable material
Stronger than diamond
Various formation (ribbon, tube, ball...)


Limitation of Graphene
Gapless Band Structure → Unsuitable for switching devices
Transition Metal Dichalcogenides

Transition Metal Dichalcogenides (MX$_2$)

Similar storyline of the graphene family
2D and layered (thin-film) structures
Covalently bonded X-M-X
held together by Van der Waals interactions
Broken symmetry in atomic basis

can make **Band Gap** of ~ 1 eV

<table>
<thead>
<tr>
<th></th>
<th>-S$_2$</th>
<th>-Se$_2$</th>
<th>-Te$_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nb</td>
<td>Metal</td>
<td>Metal</td>
<td>Metal</td>
</tr>
<tr>
<td>Ta</td>
<td>Metal</td>
<td>Metal</td>
<td>Metal</td>
</tr>
<tr>
<td>Mo</td>
<td>Semiconducting</td>
<td>Semiconducting</td>
<td>Semiconducting</td>
</tr>
<tr>
<td></td>
<td>(1L : 1.8eV, Bulk : 1.2eV)</td>
<td>(1L : 1.5eV, Bulk : 1.1eV)</td>
<td>(1L : 1.1eV, Bulk : 1.0eV)</td>
</tr>
<tr>
<td>W</td>
<td>Semiconducting</td>
<td>Semiconducting</td>
<td>Semiconducting</td>
</tr>
<tr>
<td></td>
<td>(1L : 1.9eV, Bulk : 1.4eV)</td>
<td>(1L : 1.7eV, Bulk : 1.2eV)</td>
<td>(1L : 1.1eV)</td>
</tr>
</tbody>
</table>


Recent Progress on 2D Nanosheet in World Researches

**FET –countless many reports (e.g. A. Kis in Nat Nano. 2011)**

**CMOS –several reports**

**pn diode–several reports**
Outline

- Introduction: Outline and Motivation
- Progress on 2D Nanosheets in World Researches

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- Progress on 2D Nanosheets in our Lab
  - Top-gate MoS$_2$ FET, Nonvolatile Memory FETs and P-N diode
  - 2D-2D, 2D-1D, 2D-Organic Hybrid Complementary Inverter
  - Black Phosphorous Dual Gate FETs
  - NiOx-MoS$_2$ van der Waals junction MESFET

- Summary
For n-channel FET (i.e., oxide semiconductor)

\[ \Delta V_{th}(\varepsilon) \rightarrow \Delta Q_{\text{eff}} = C \Delta V_{th} \rightarrow D_{it}(\text{CBM} - \varepsilon) = \frac{C_{ox}}{q} \frac{\partial V_{th}(\varepsilon)}{\partial \varepsilon} \]

Making on-state (accumulation) \rightarrow All interfacial (electron) traps are occupied…

\[ \varepsilon_1 < \varepsilon_2 \]

\[ \varepsilon_1 = h\nu_1 \]

\[ \varepsilon_2 = h\nu_2 \]

\[ E_F \]

\[ E_{C} \]

\[ E_{Fn} \]

\[ E_F \ni \partial \]

\[ \text{DOS of interfacial traps} \]

\[ \text{Modification of } Q_{\text{eff}} \]

\[ \text{Result in } V_{th} \text{ shift!!} \]

Advanced Materials, 22, 3260, 2010

Gate Voltage

Drain Current

Initial (dark state)

For n-channel FET (i.e., oxide semiconductor)

\[ e_1 < e_2 \]

\[ e_1 = h\nu_1 \]

\[ e_2 = h\nu_2 \]

\[ E_F \]

\[ E_C \]

\[ E_{Fn} \]

\[ D_{it}: \text{DOS of interfacial traps} \]

\[ \text{Modification of } Q_{\text{eff}} \]

\[ \text{Result in } V_{th} \text{ shift!!} \]

Gate Dielectric n-channel

Photo-Excited Charge Collection Spectroscopy

IGZO

LG Display

IGZO
Recent Progress on 2D Nanosheet (IM)

1. Nanosheet Band-Gap & Thickness Modulation


2. Nanosheet-Dielectric Interface Trap


<table>
<thead>
<tr>
<th>Number of MoS$_2$ layer</th>
<th>Trap density (X10$^{12}$ cm$^{-2}$) obtained from</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Hysteresis</td>
</tr>
<tr>
<td>2</td>
<td>1.92</td>
</tr>
<tr>
<td>3</td>
<td>1.26</td>
</tr>
<tr>
<td>4</td>
<td>2.47</td>
</tr>
</tbody>
</table>
Recent Progress on 2D Nanosheet (IM)

3. Nonvolatile Memory FETs

MoS$_2$ Nanosheets for Top-Gate Nonvolatile Memory Transistor Channel, Small (2012)

4. 2D-2D van der Waals p-n diode

Enhanced device performance of WSe$_2$-MoS$_2$ van der Waals junction p-n diode by fluoropolymer encapsulation, JMC C (2015)
2D-2D, 2D-1D, 2D-Organcic Hybrid Complementary Inverter


H.S. Lee et al. *Small*, 11, 2132 (2015)
Fabrication: Direct Imprinting Method

Step 1 | Flake exfoliation
Step 2 | Alignment
Step 3 | Flake imprinting

Step 4 | MoS₂ transfer
Step 5 | WSe₂ transfer
Step 6 | SD patterning

Transferred flakes on patterned-gate

Source/Drain patterning
2D p-WSe$_2$ and n-MoS$_2$ FETs on Wafer

- 285 nm-thick SiO$_2$/p$^+$-Si substrate
- Large operation voltage in a range of $V_G$=-20~10 V
  ($V_{TH}$=+5 V for p-WSe$_2$, $V_{TH}$=-15 V for n-MoS$_2$)
- Large gate-source leakage current of $I_{GS}$~100 pA
- Large overlap area between un-patterned gate and source/drain electrodes
- Negative transition voltage of $V_{TR} = -7.5\, V$
  (not suitable for practical applications)
- Voltage gain ($-dV_{OUT}/dV_{IN}$) : $\sim 6$
- Peak power consumption ($P = V_{DD} \times I_{DD}$) : $\sim 1\, \mu W$
- Large switching delay of $10\, ms$

  due to overlap capacitance-induced booster effects
2D p-WSe₂ and n-MoS₂ FETs on Glass

- 50 nm-thin Al₂O₃ (ALD)/Patterned gate on glass substrate
  - Low operation voltage of \( V_G = -5 \sim +5 \) V
  - Low gate-source leakage current of <100 fA
- Fluoropolymer CYTOP encapsulation (C-F bond-induced dipoles)
  - Induced more hole carriers into thin p-WSe₂ (positive \( V_{TH} \) shift)
  - Reduced electrons in thin n-MoS₂ (reduced on-current).
Complementary Inverter on Glass

- **Positive transition voltage shift** after CYTOP encapsulation
  
  \(V_{TR}: 0.1 \text{ V} \rightarrow 2.3 \text{ V}\)

- High **voltage gain of 23** at \(V_{DD}=5 \text{ V}\)

- Subnanowatt power consumption: \(P_{peak} \approx 1 \text{ nW}\)

- Ideal noise margin: \(NM_L=0.385xV_{DD}, NM_H=0.495xV_{DD}\) at \(V_{DD}=5 \text{ V}\)

- Switching delay: \(~800\ \mu\text{s}\)
Pass Transistor Logic Gates

### NOT gate

- **Input Voltage ($V_{IN}$):** 0 V, 3 V
- **Output Voltage ($V_{OUT}$):** 0 V, 3 V
- **Truth Table:**
  - $V_{IN} = 0$: $V_{OUT} = 1$
  - $V_{IN} = 1$: $V_{OUT} = 0$

### OR gate

- **Input A ($A$) and B ($B$):** 0 V, 3 V
- **Output Voltage ($V_{OUT}$):** 0 V, 3 V
- **Truth Table:**
  - $A = 0$: $V_{OUT} = B$
  - $A = 1$: $V_{OUT} = A$

### AND gate

- **Input A ($A$) and B ($B$):** 0 V, 3 V
- **Output Voltage ($V_{OUT}$):** 0 V, 3 V
- **Truth Table:**
  - $A = 0$: $V_{OUT} = 0$
  - $A = 1$: $V_{OUT} = 0$ if $B = 0$, $V_{OUT} = 1$ if $B = 1$
2D-1D Hybrid Complementary Inverter

Voltage gain of 60 and subnanowatt power consumption at static states

Highest gain and lowest power consumption for reported 2D material based inverter

2D-Organoic Hybrid Complementary Inverter

Forecast some possibility to use 2D FET combined with Org. Elec. ?
Dual gate black phosphorous field effect transistors on glass for NOR logic and organic light emitting diode switching

Images and Raman spectra

Thickness ~ 12 nm
I-V Characteristics of Dual gate FET

- For $V_{gs} = -5 \sim 5$ V, 11 steps
- For $V_{gs} = 3 \sim 5$ V, 3 steps
- For $V_{gs} = 2 \sim 5$ V, 4 steps

![Graphs showing I-V characteristics for different gate voltages and modes (TG Mode, BG Mode, and DG Mode).](image)
Voltage shifts & Logic gate

ambipolar transition voltage shifts from -0.5 to 1.5 V by applied top gate bias
Dynamic OLED Switching

Well switching operated as Green, blue OLED pixel
Dynamic OLED Switching

Well switching operated as Green, Blue OLED pixel
NiO$_x$-MoS$_2$ metal-semiconductor field-effect transistor for high mobility and photoswitching speed

H.S. Lee et al. ACS Nano, 9, 8312, (2015)
“Thermally evaporated NiO\textsubscript{x} is known to have quite a deep work function of more than 5.1\textasciitilde5.2 eV as a Ni-rich semi-transparent conducting oxide (x\textasciitilde0.9).”
NiO$_x$ van der Waals Schottky Interface

- The better rectifying behavior for the thinner MoS$_2$

- The higher Schottky barrier height for the thinner MoS$_2$

$q\Phi_B = q\Phi_{NiOx} - qX_{MoS2}$
MESFET: Channel Thickness Effects

- NiOₓ/MoS₂ van der Waals interface: 0.3 nm gap by calc.!

\[ \mu = \frac{L g_{Max}}{q N_d t W} \]

, where \[ g_m = \frac{\partial I_D}{\partial V_g} = \frac{q N_d \mu t W}{L} \]
4-Probe Hall Measurement

**MoS$_2$ Hall Coeff-H(T) Curve**

\[
R_H = \frac{V_H}{I} = -\frac{H}{n_s q} \quad \Rightarrow \quad n_s = -\frac{1}{q} \left(\frac{\partial R_H}{\partial H}\right)^{-1}
\]

- $n_s = 4.03 \times 10^{10}$ cm$^{-2}$ (2.52 x $10^{16}$ cm$^{-3}$) for 16 nm-thick MoS$_2$ at 300 K
- Hall mobility of 16 nm-thick MoS$_2$: ~200 cm$^2$/V s
**MESFET vs. MISFET**

Saturation behavior in MESFET: easier channel-depletion (pinch-off) in drain side
“The carrier transport in MESFET may hardly be interfered by insulator-semiconductor interface traps or an on-state gate field.”

<table>
<thead>
<tr>
<th>Parameters</th>
<th>MESFET</th>
<th>MISFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Subthreshold swing</td>
<td>83 mV/dec</td>
<td>200 mV/dec</td>
</tr>
<tr>
<td>Mobility</td>
<td>950 cm$^2$/V s</td>
<td>13 cm$^2$/V s</td>
</tr>
<tr>
<td>Hysteresis</td>
<td>0.06 V</td>
<td>8.56 V</td>
</tr>
<tr>
<td>Threshold voltage</td>
<td>-1 V</td>
<td>-25 V</td>
</tr>
</tbody>
</table>
Photo-detecting properties & Dynamic

<table>
<thead>
<tr>
<th></th>
<th>MESFET</th>
<th>MISFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Photo-to-dark current ratio</td>
<td>$2.85 \times 10^3$</td>
<td>$1.4 \times 10^2$</td>
</tr>
<tr>
<td>Responsivity (ON state)</td>
<td>5000 A/W</td>
<td></td>
</tr>
<tr>
<td>Responsivity (OFF state)</td>
<td>1.1 A/W</td>
<td></td>
</tr>
<tr>
<td>Delay</td>
<td>2 ms</td>
<td>250 ms</td>
</tr>
</tbody>
</table>
Summary

- **2D-FETs**
  analysis MoS$_2$ band gap, nonvolatile memory, p-n diode

- **Hybrid complimentary Inverter:** nW power, high gain
  2D-2D, 2D-1D, 2D-Organic

- **Black Phosphorous Dual Gate FETs:** High current, NOR gate
  TG BG bipolar transition voltage shifts, OLED switching

- **NiOx-MoS$_2$ van der Waals junction MESFET:**
  Intrinsic high mobility and photo-switching speed
IM’s group activity on 2D Devices

FET
Im’s group activity toward 2D semi.

**Hybrid (Complimentary) Inverter**
12. High-gain subnanowatt power consumption hybrid complementary logic inverter with WSe₂ nanosheet and ZnO nanowire transistors on glass *Advanced Materials*, 27, 150 (2015)

**P-N and Schottky Diode**

**Memory FET**
Acknowledgement

- National Research Foundation of Korea
  National Research Laboratory: 2014R1A2A1A01004815,
- Yonsei University
- Brain Korea 21 plus

Collaboration Groups

- LG Display & Samsung Display
- Dr. Won-Kook Choi (KIST - Optoelectronic Materials and Devices Post-Silicon Semiconductor)
- Prof. Takhee Lee (Seoul National Univ. - Dept. of Physics and Astronomy)
- Prof. Myung Mo Sung (Hanyang Univ. - Dept. of Chemistry)
- Prof. Jae Hoon Kim, Hyoung Joon Choi, Yeonjin Yi (Yonsei Univ. - Dept. of Physics)
- Prof. Hyungjun Kim, Jong-Hyun Ahn (Yonsei Univ. - Dept. EE)
Thank you for listening

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