Nanoscale Silicon Based Nonvolatile Memory

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Acknowledgements

Collaboration

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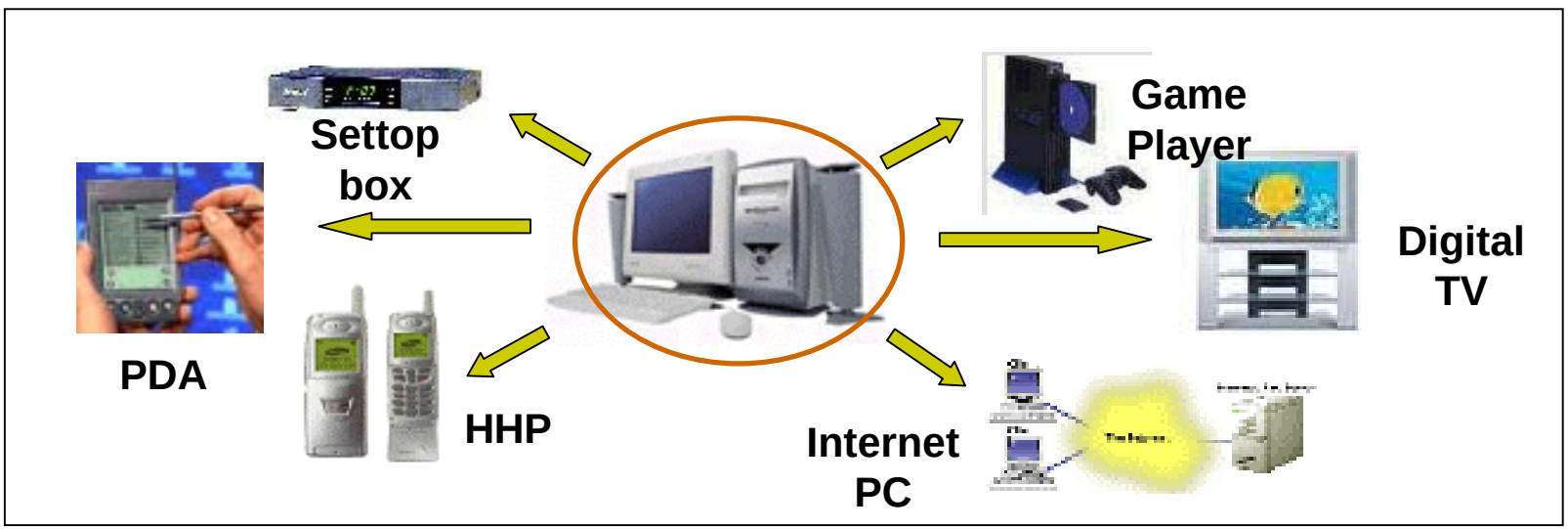
Outline

- Introduction
- Current research status
  - Nano fabrication Process
    - Nanoscale patterning
    - SiN thin film
    - Si Nanoparticle
  - Nano devices
    - Nanoscale SONOS memory
    - Vertical channel memory
- Future Work

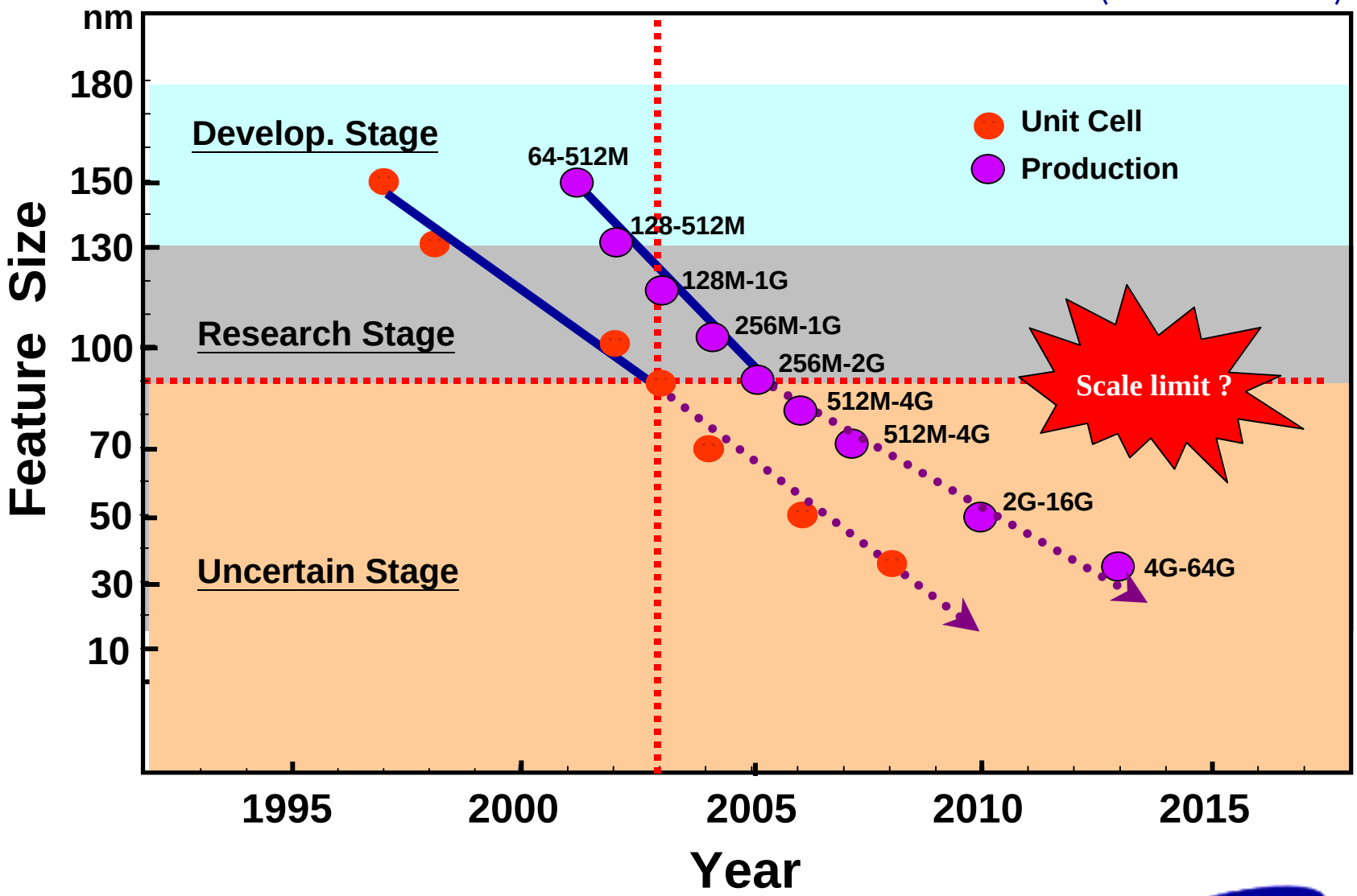
Environment of Memory

- **New application, unification**
  - Diversfied from PC into digital application
  - Increasing capacity of voice, motion picture information
    - ➔ Need higher density of memory
  - Increasing demand for unified memory
- **Uncertainty of DRAM & Flash Memory scalability**
- **Memory Market: $35 billion (2001), $72 billion (2010), 8.3% increase/year**



Flash Memory Roadmap

(Source: ITRS 2001)



Flash Technology Requirements

(Source: ITRS 2001)

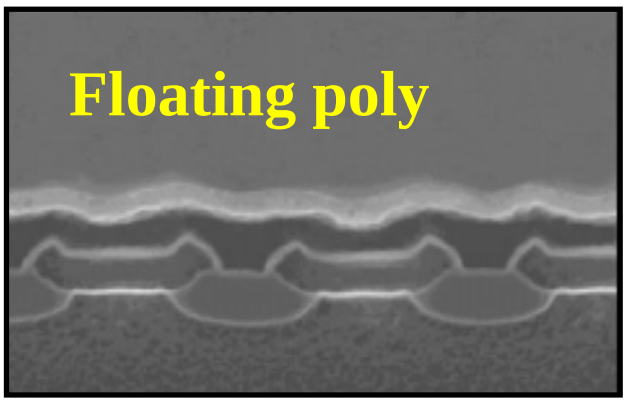
Year of Production	2001	2002	2003	2004	2005	2006	2007
Flash tech. Node, F[nm]	150	130	115	100	90	80	70
NOR highest W/E Voltage[V]	8-10	8-10	8-10	8-10	7-9	7-9	7-9
NAND highest W/E Voltage[V]	19-21	18-20	18-20	18-20	18-20	17-19	17-19
NOR tunnel dielectric thickness[nm]	9.5-10.5	9.5-10	9-10	9-10	8.5-9.5	8.5-9.5	8.5-9.5
NAND tunnel dielectric thickness[nm]	8.5-9.5	8.5-9	8-9	8-9	8-9	7.5-8	7.5-8
NOR interpoly dielectric thickness[nm]	13-15	12-14	11-13	11-13	10-12	9-11	9-11
NAND interpoly dielectric thickness[nm]	14-16	13-15	12-14	12-14	12-14	11-13	10-12

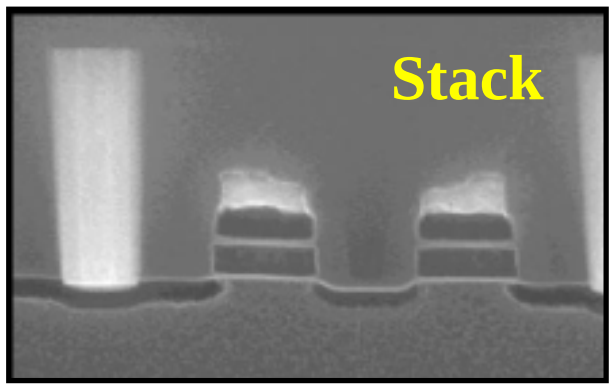
참고자료 : ITRS 2001

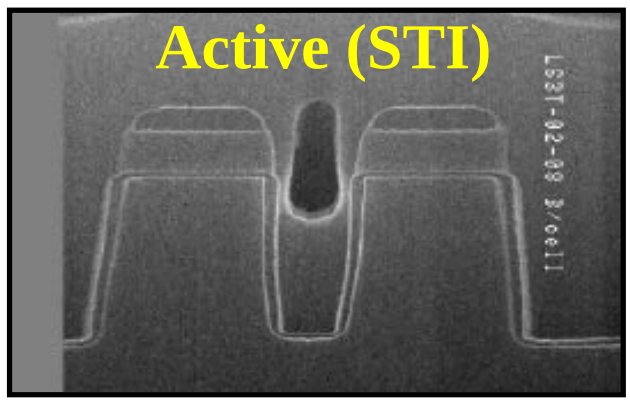
	Solutions Exist
	Solutions are Known
	Solutions are NOT Known

Problems of conventional technologies

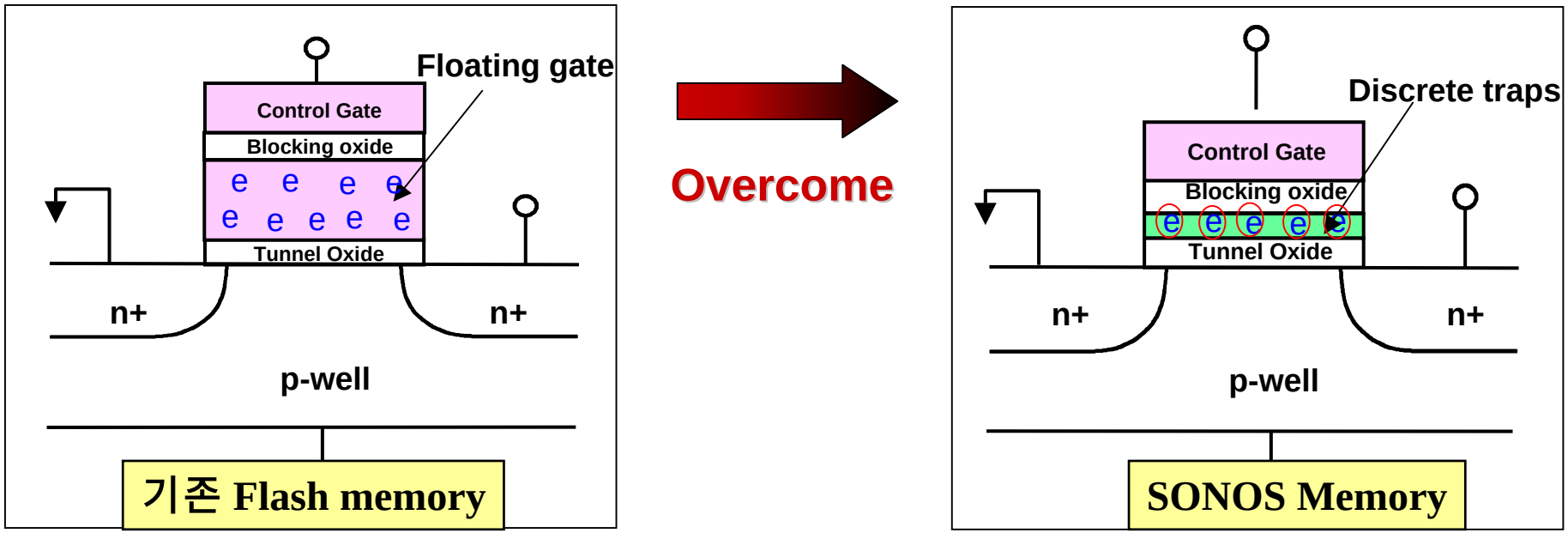
- What's the limits of flash scaling ?







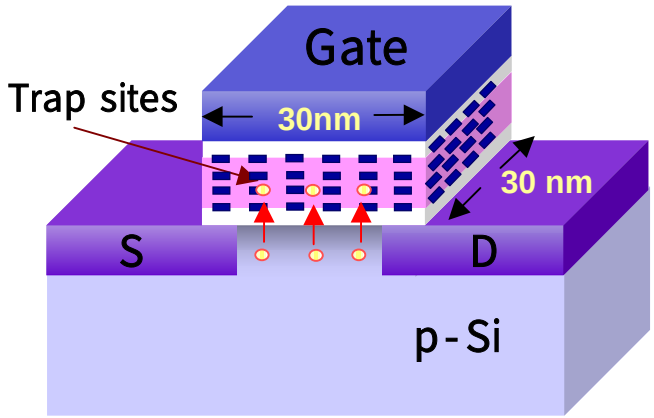
Discrete traps



☞ **Discrete traps (SiN traps or Nanocrystal)**

*** SONOS (Silicon-Oxide-Nitride-Oxide-Silicon)**

Motivation for SONOS



US Patent # 6313503 (2001.11.6)

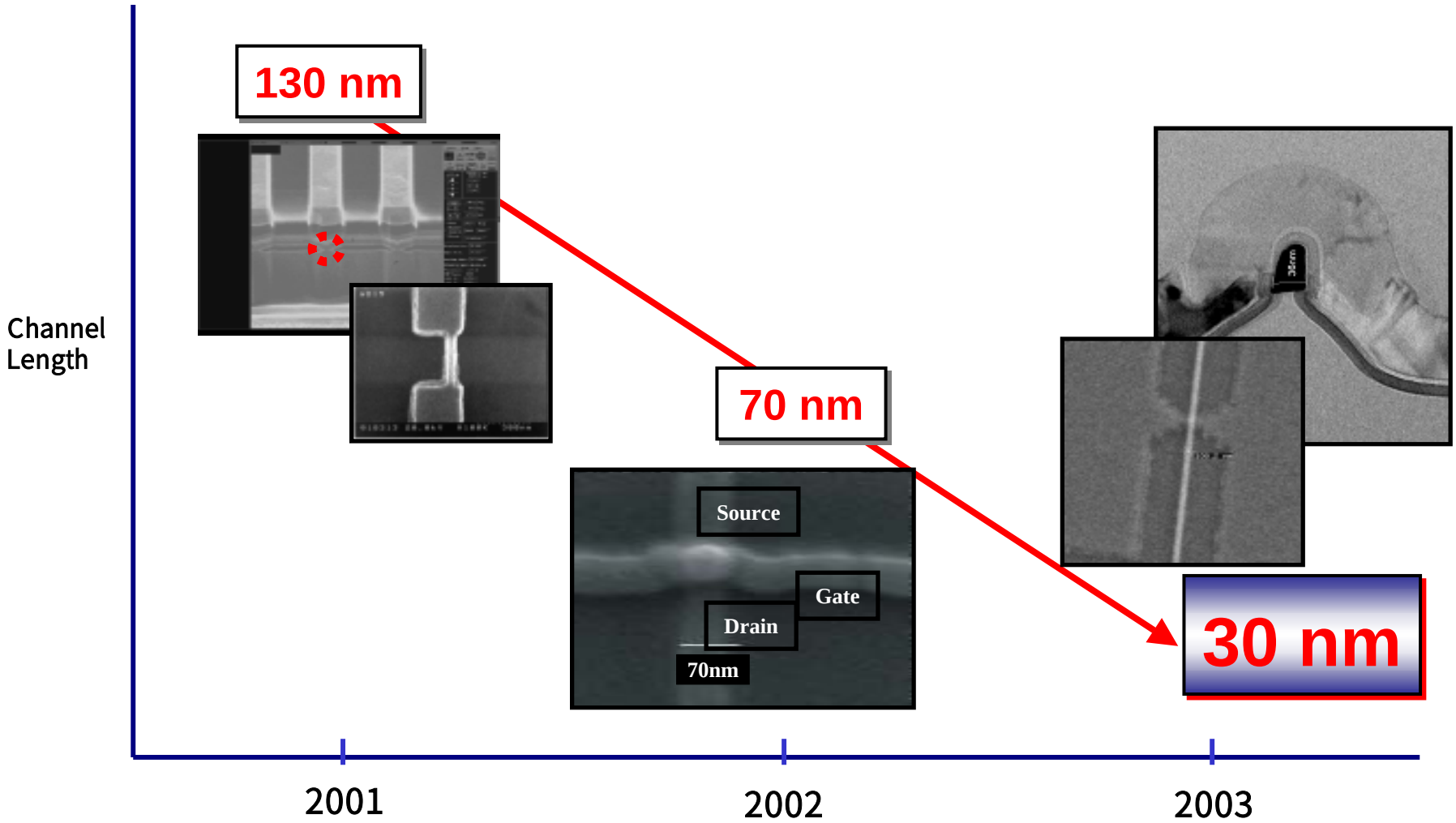
< Advantages >

- Compatibility of SONOS with CMOS with the use of thin nitride
- Lower programming voltage
- Smaller dimension capability than FG EEPROM
- Longer retention & low defect induced tunneling leakage (Nitride instead of poly Si)
- Higher programming speed (depends on ONO thickness)

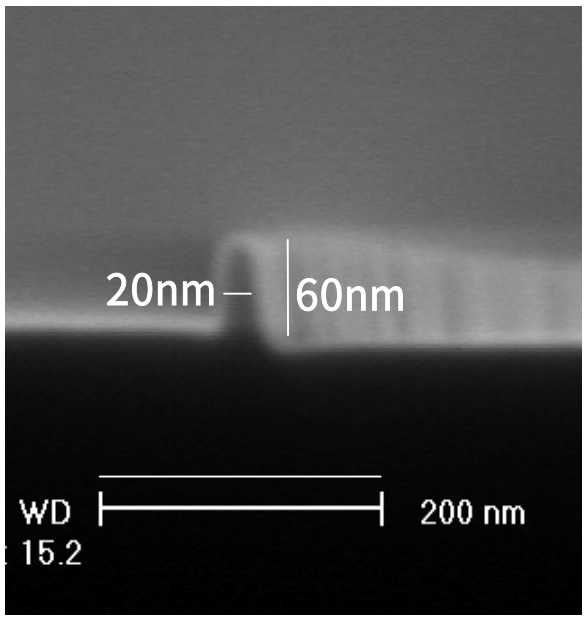
Comparison of Memory Technologies

	FRAM	MRAM	PRAM	SONOS
Cell size	8~25 F^2	8~9 F^2	6 F^2	4~10 F^2
Read time	30~200 ns	10~100 ns	10~100 ns	20~120 ns
Write time	30 ns	10~15 ns	10~100 ns	1 μs ~ 1 ms
Retention	> 10년	> 10년	> 10년	>10년
Endurance	> 10E12	> 1E13	> 10E13	> 1E5
Current/Power	Low	High	High	Low
Cost	High	High	Low	Low
Process	Special	Special	Special	CMOS
Issues	Etching process Cost Retention, Fatigue	Etching process Uniform thin films Cost	Power consumption	Thin Oxide film Faster P/E time

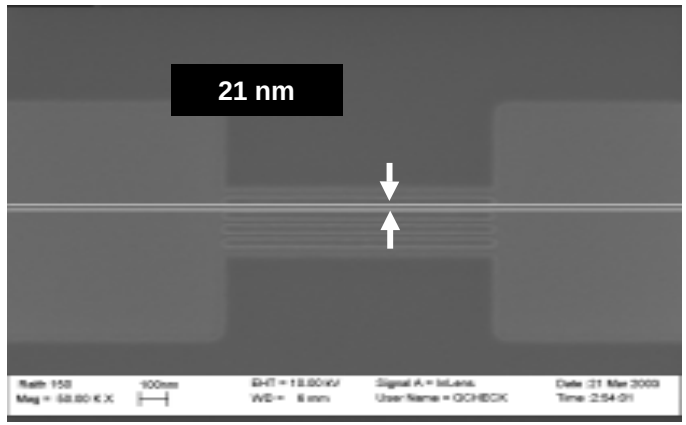
SONOS Memory Development



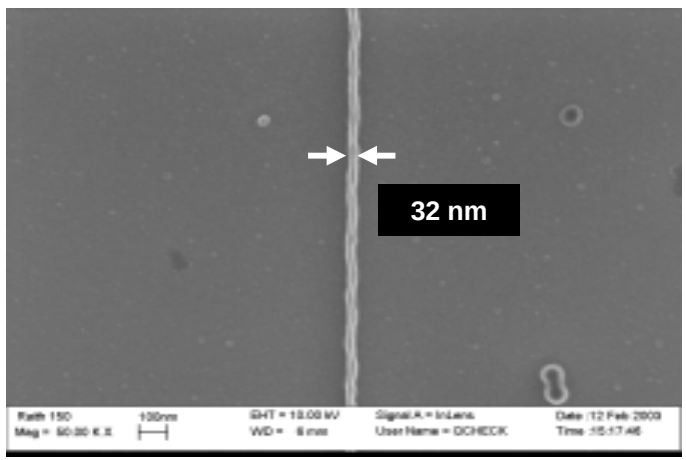
Nano Lithography



Sidewall Patterning

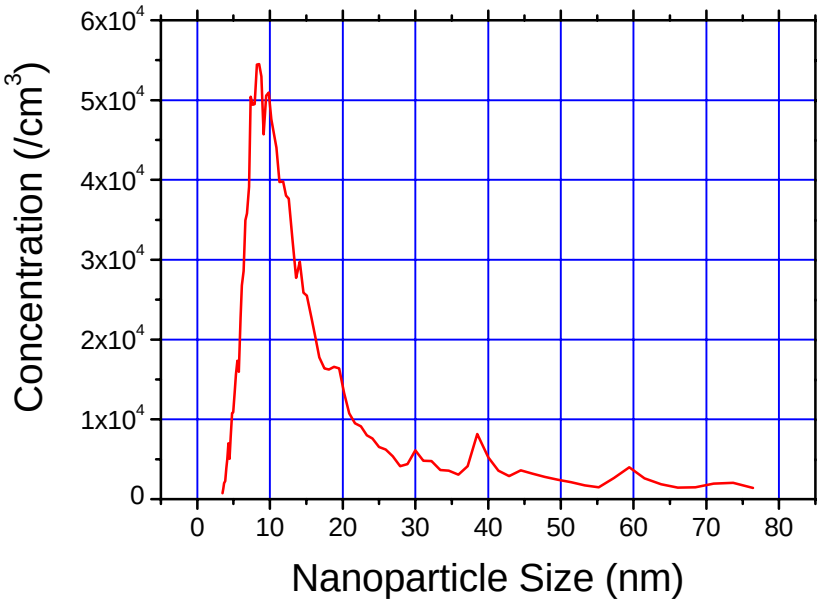


Positive Resist : PMMA

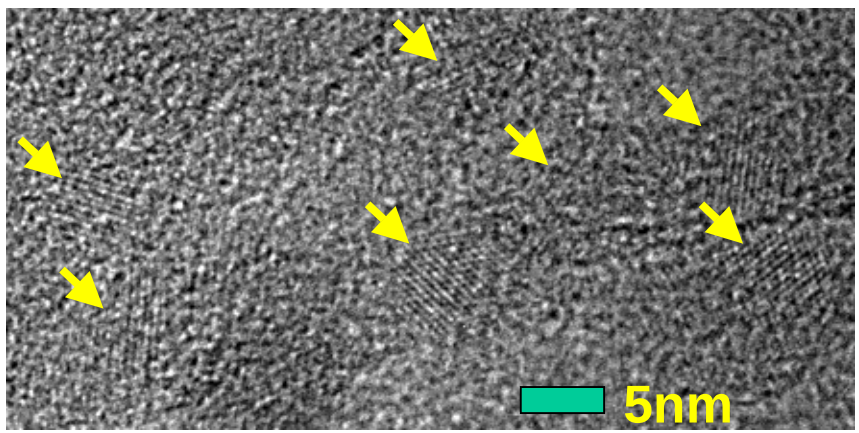


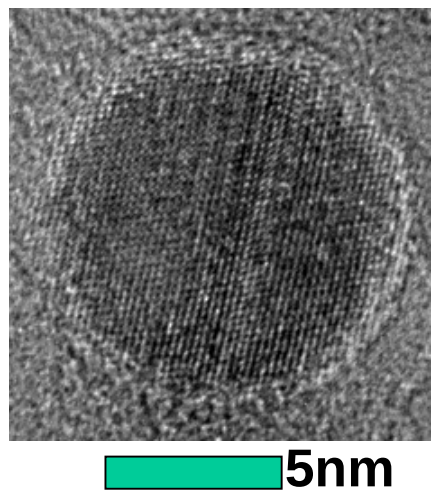
Negative Resist : Calixarene

Si Nanoparticle Fabrication by Aerosol Laser Ablation

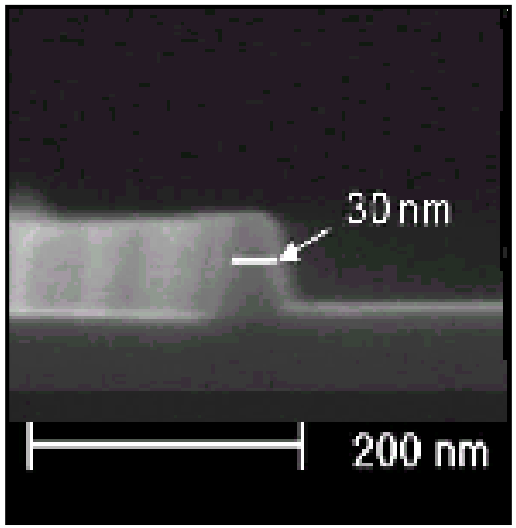


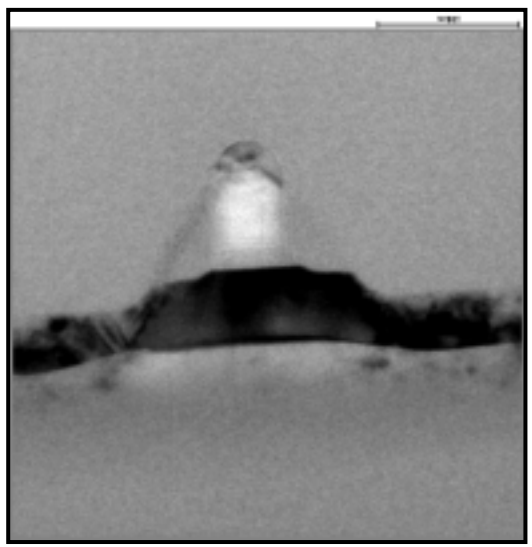
- D <10nm
- ρ ~ 1×10¹¹ /cm²

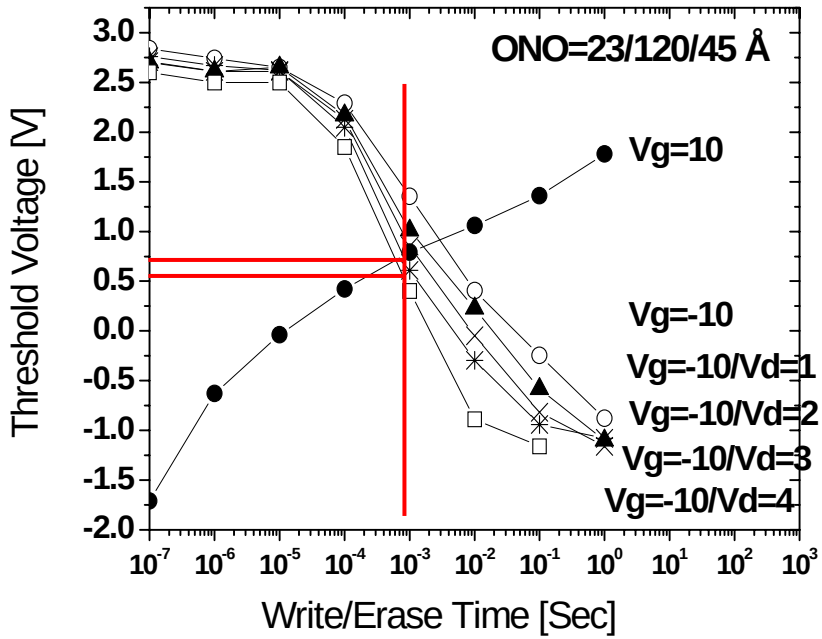




30nm SONOS Memory by SWP



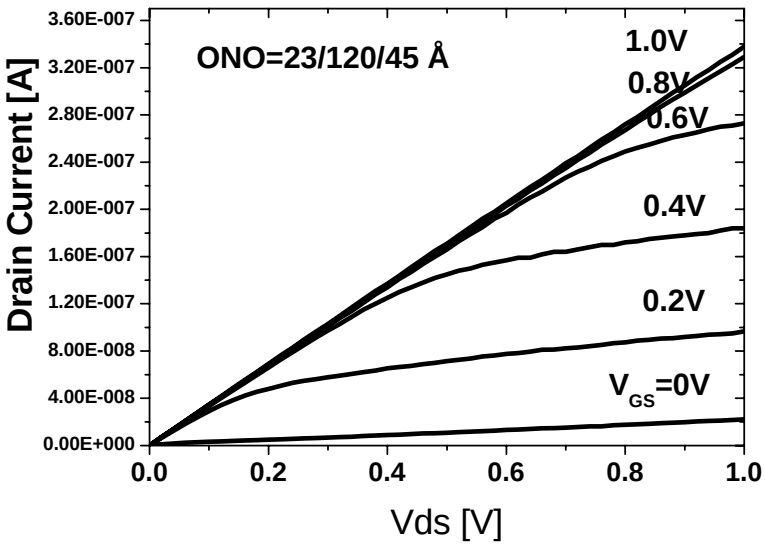


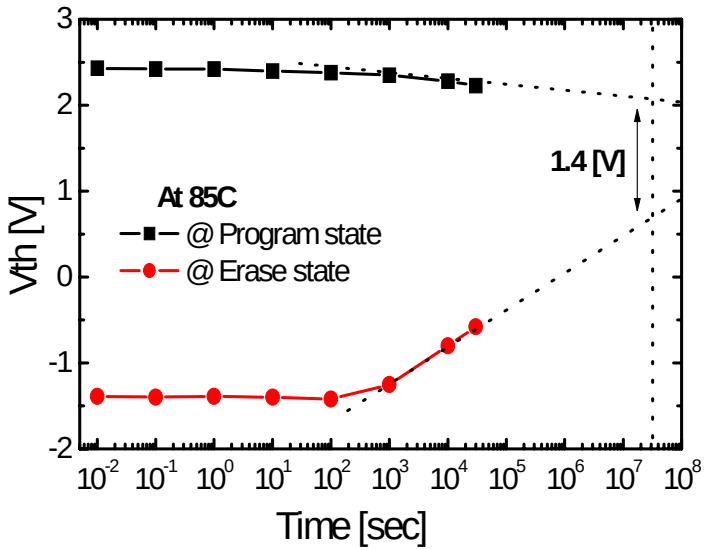


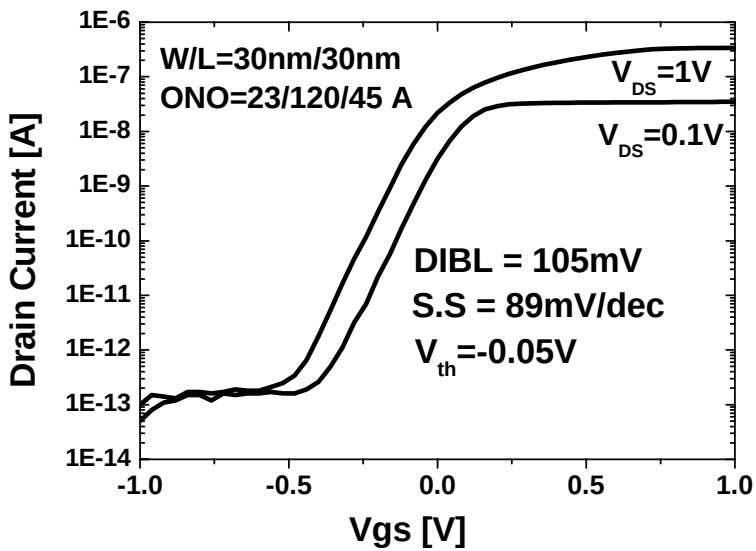
Key Features of SONOS Cell

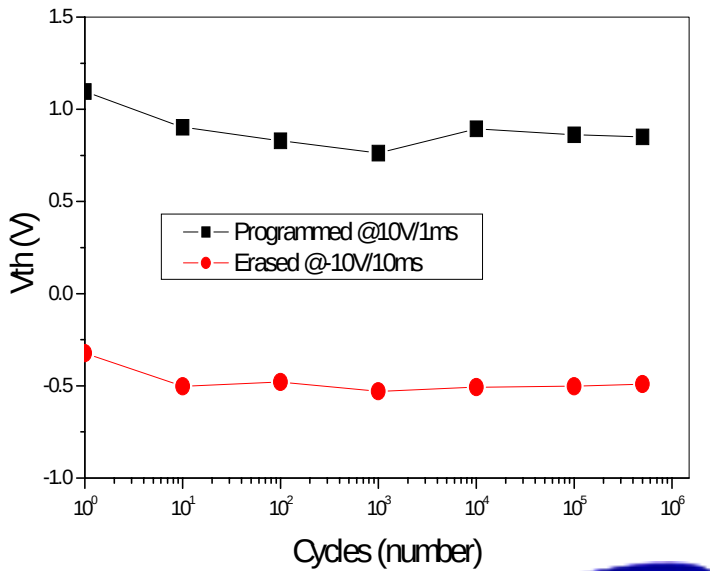
- ❒Memory Node Size: 30 x 30 nm2
- ❒ Write/ Erase Voltage: <10V
- ❒ Write/Erase Time: 1 msec
- ❒ Endurance: >10^6 cycles
- ❒ Retention = 1year @T=85°C

Key Characteristics of SONOS Memory

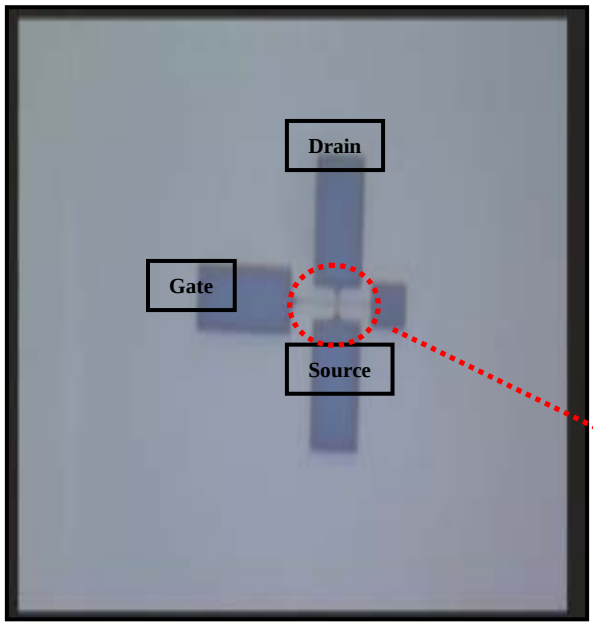


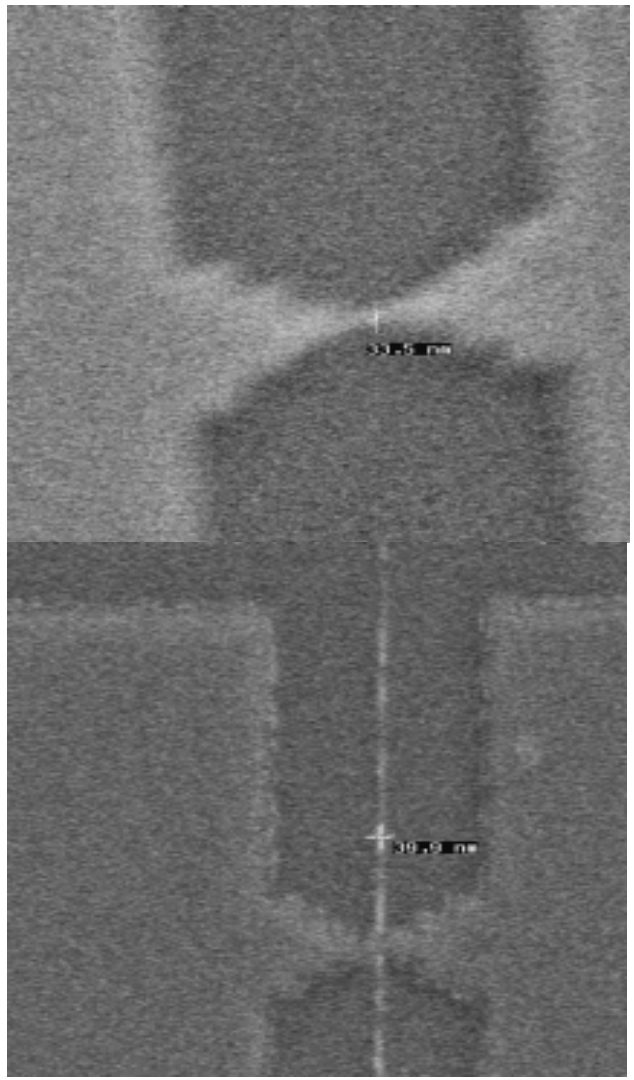






SONOS Memory by E-beam Lithography

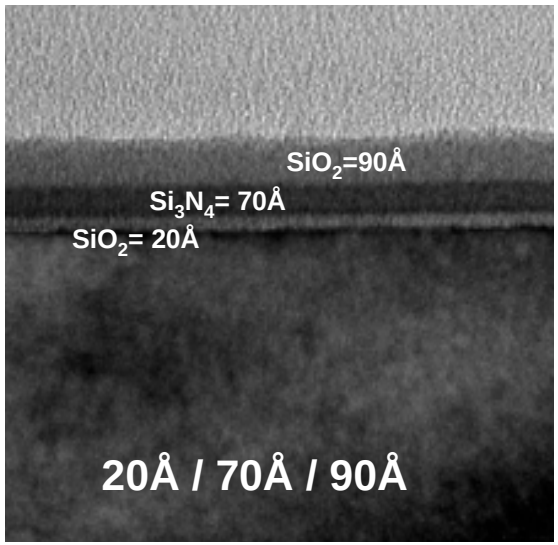


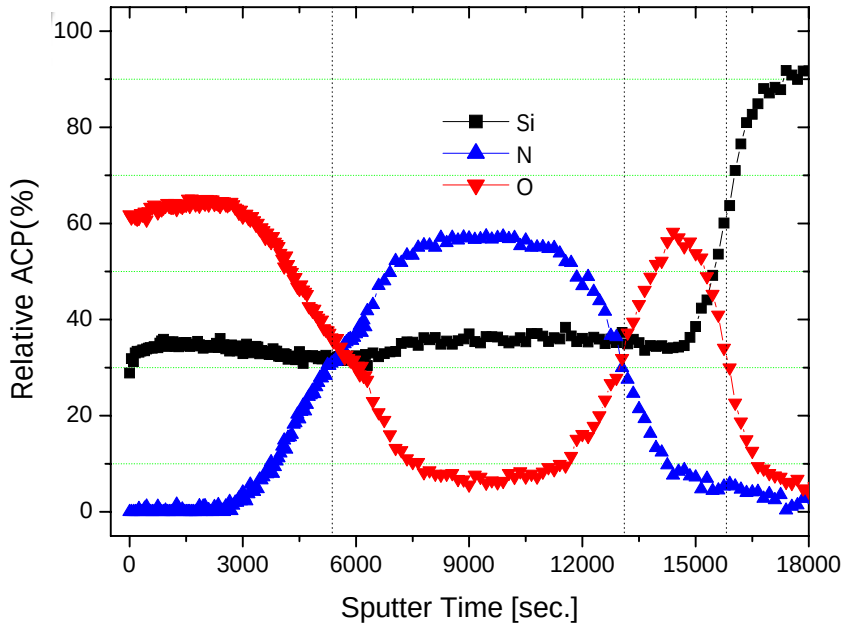


SONOS Cell by E-beam Lithography

W/L : 33nm / 46nm

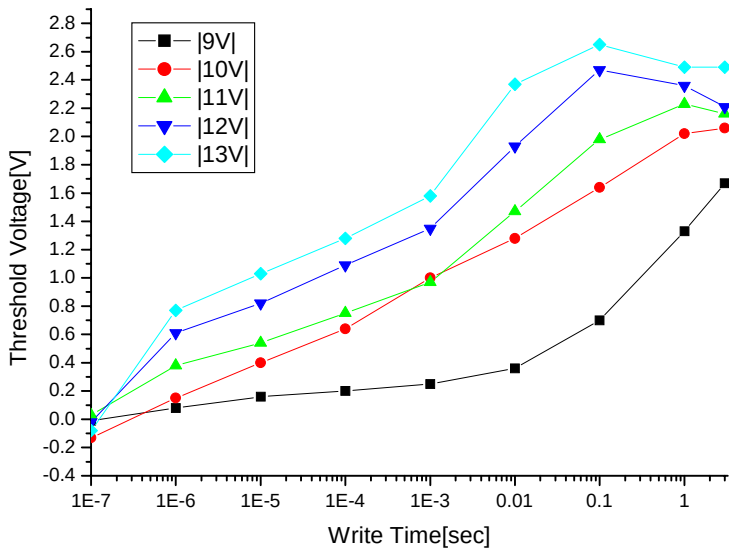
ONO layer TEM & AES Analysis

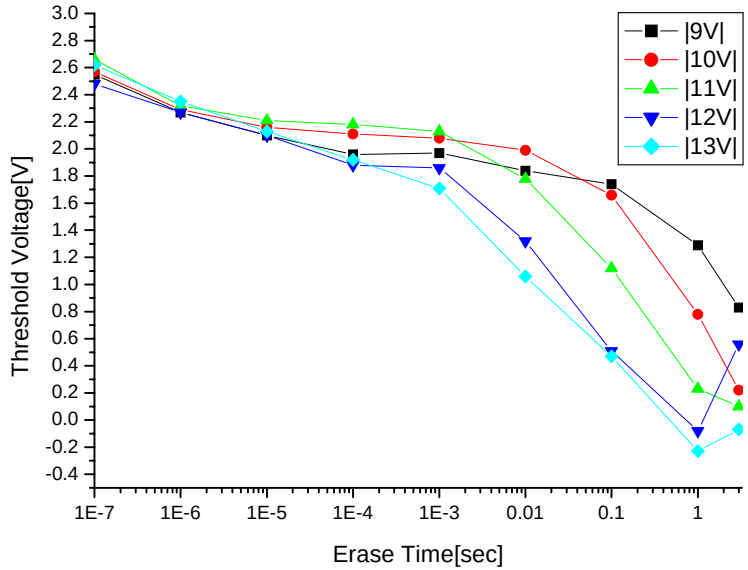




- TEM of the ONO (2 nm/7 nm/9 nm) stack
- Auger profile showing the stoichiometric of ONO layer.

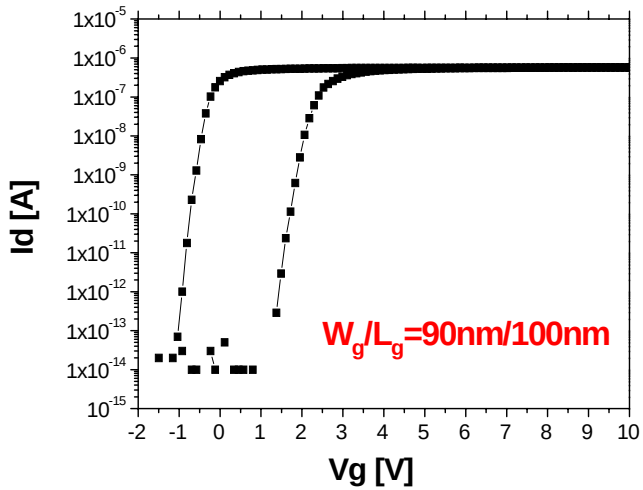
Program & Erase Characterisics

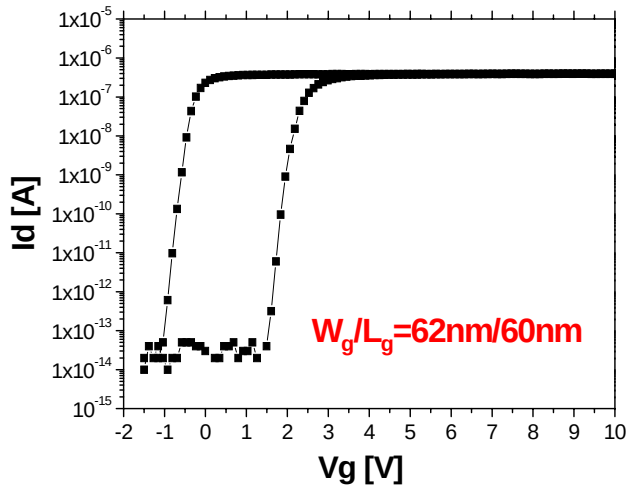


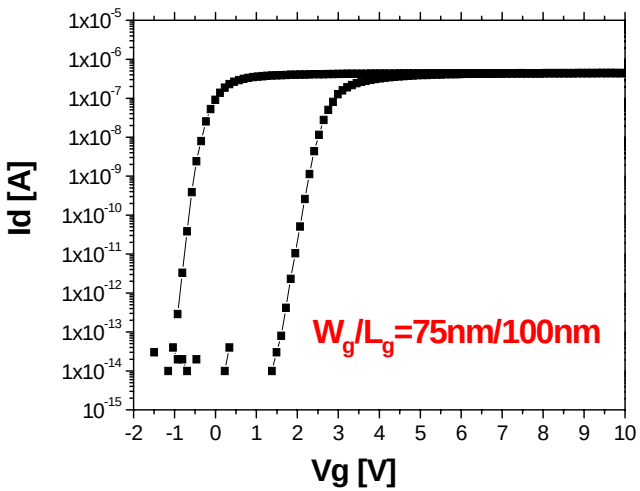


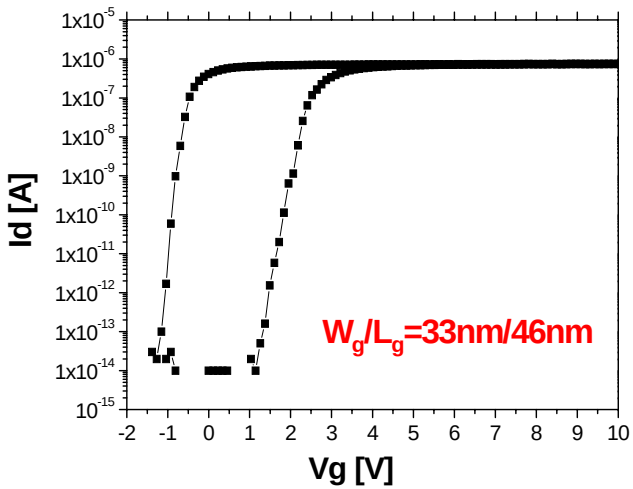
- ΔVth ~ 2.4V
- Trapped Charge density = 4.1 ~ 5.9 x 10^{12} cm^{-2}
- No. of e^- = 61 ~ 88 for 33nm x 46nm node size

Memory Window Comparison



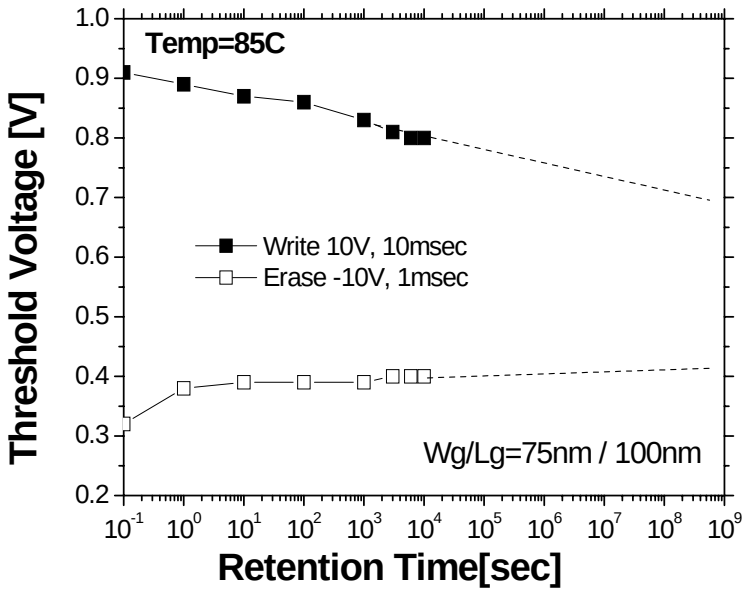






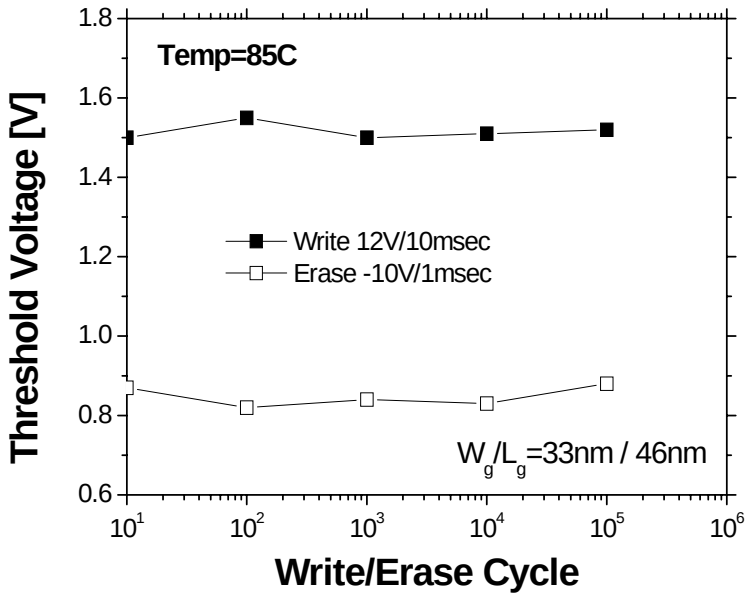
- **Memory window is nearly similar for SONOS devices with different memory node areas**

Retention Time



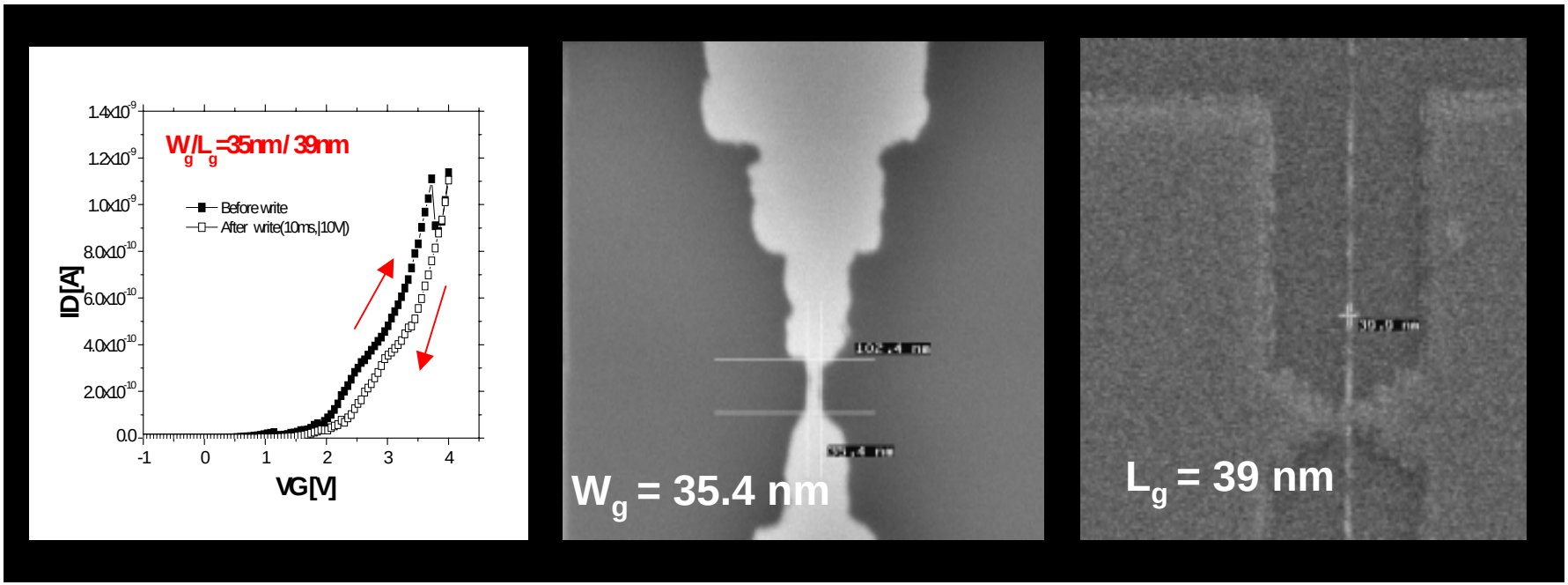
- Retention time is good with 75nm width and 100 nm length at 85℃.

Endurance



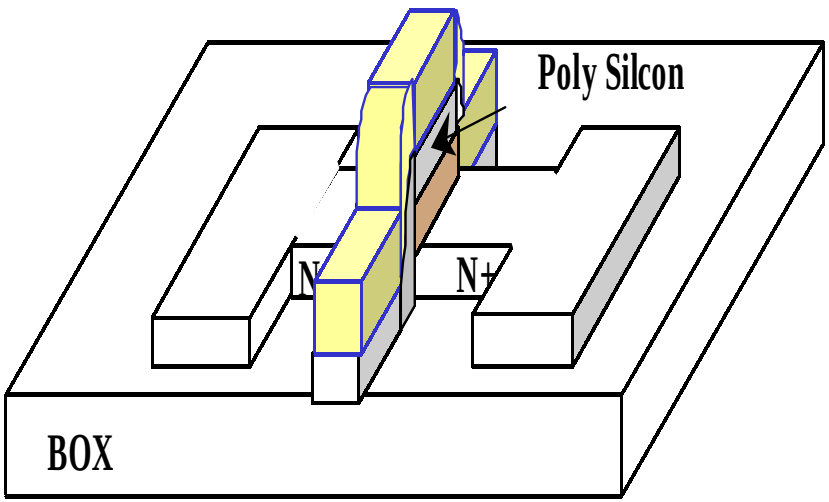
- It remains unchanged up to 10^5 cycles, indicating superior endurance characteristics at 85℃.

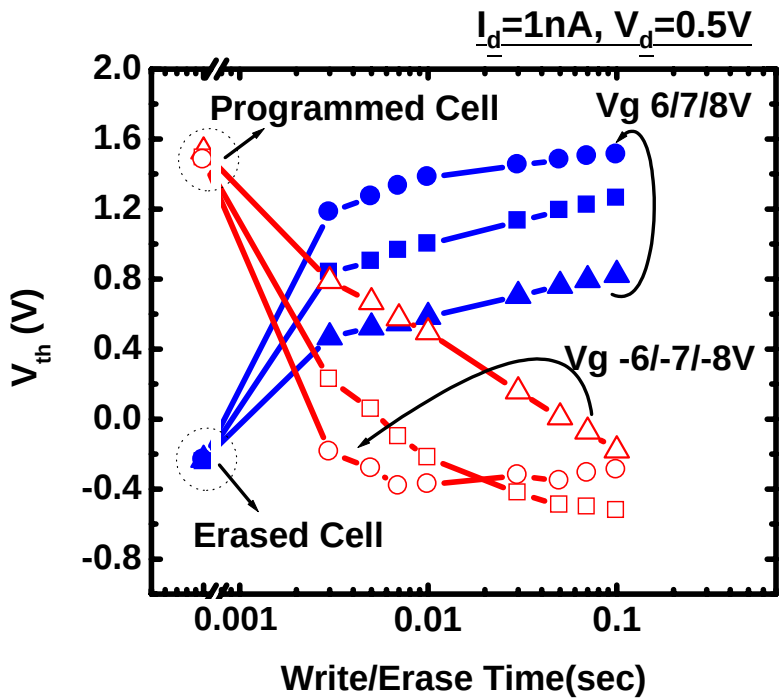
Memory Effect at 30 nm dimensions



- Single electron charging effect at 30 nm dimensions.

Vertical Channel SONOS

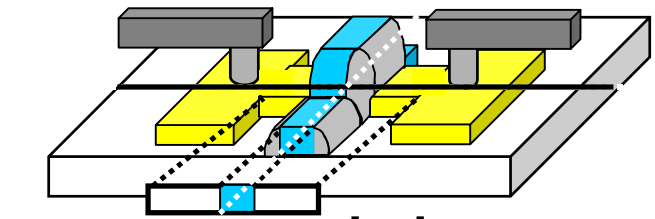


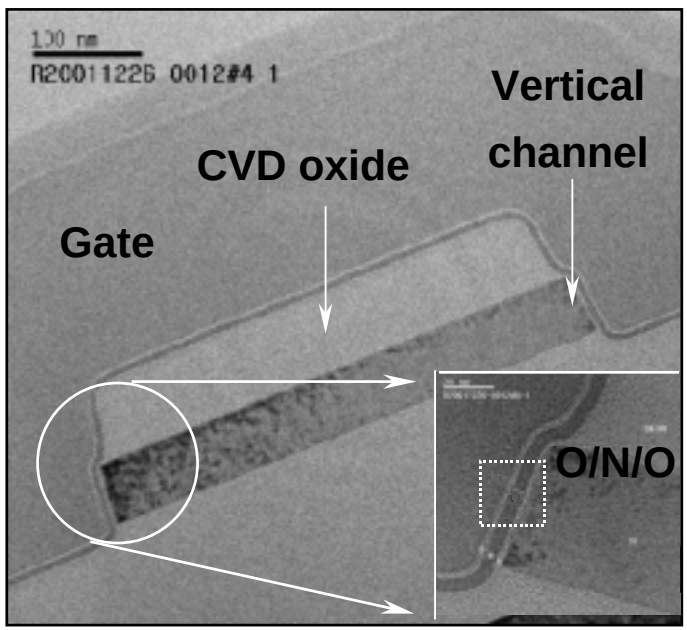


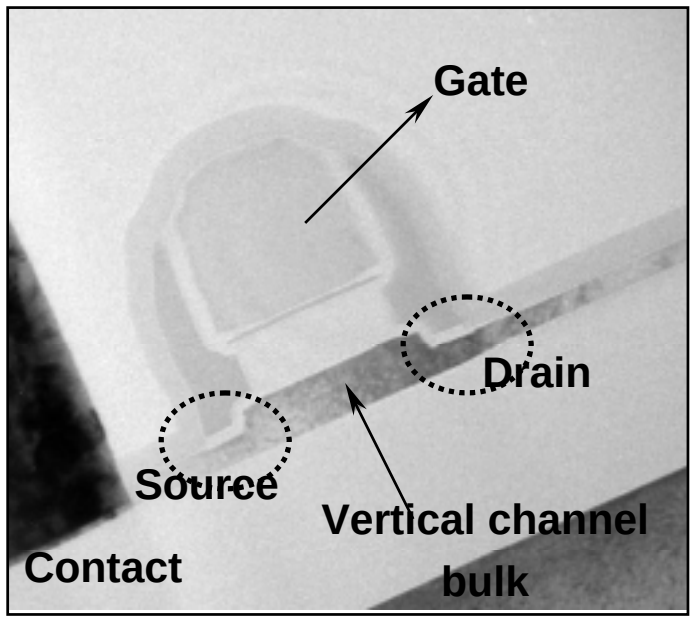
Schematic of VC SONOS

• ΔVth=1.6V @ 8/-8V &10ms

TEM images


source gate drain


100 nm
R2C011226 0012#4 1
Vertical
channel
CVD oxide
Gate
O/N/O


Gate
Drain
Source
Vertical channel
Contact
bulk

Future Work

- **Nano fabrication process for Integration**
- **Improvement of SONOS memory characteristics**
  - High-k materials
  - New memory cell structure
  - Optimal bias conditions
- **Device physics**
  - Single electron effect
  - Reliability failure mechanism
  - Memory cell Modeling/Simulation