Nanoscale Silicon Based Nonvolatile Memory

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Acknowledgements

**Collaboration**

Seoul National University (SNU)
Prof. Park, Byung-GooK

Korea Institute for Advanced Study (KIAS)
Prof. Kim, Dae Mann

Cornell University, USA
Prof. Sandip Tiwari

Institute of Semiconductor Physics, Russia
Prof. Vlradmir Gritsenko

**Funding**

Kwangju Institute of Science and Technology (KJ IST)
Prof. Hwang, Hyun sang

Sungkyunkwan University
Prof. Chung Ilsueb

Tera-level Nanodevices
21st Century Frontier R&D Program, Ministry of Science and Technology
SEC and SAIT
Outline

- Introduction
- Current research status
  - Nano fabrication Process
    - Nanoscale patterning
    - SiN thin film
    - Si Nanoparticle
  - Nano devices
    - Nanoscale SONOS memory
    - Vertical channel memory
- Future Work
New application, unification
- Diversified from PC into digital application
- Increasing capacity of voice, motion picture information
  → Need higher density of memory
- Increasing demand for unified memory

Uncertainty of DRAM & Flash Memory scalability

Memory Market: $35 billion (2001), $72 billion (2010), 8.3% increase/year
Flash Memory Roadmap

(Source: ITRS 2001)

- **Research Stage**: Scale limit?
- **Uncertain Stage**: 130, 180, 70, 50, 150, 100, 90, 80, 70, 60, 50, 40, 30, 20, 10, 10

Year:
- 1995
- 2000
- 2005
- 2010
- 2015

- **Unit Cell**
- **Production**

### Flash Technology Requirements

(Source: ITRS 2001)

<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2001</th>
<th>2002</th>
<th>2003</th>
<th>2004</th>
<th>2005</th>
<th>2006</th>
<th>2007</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flash tech. Node, F[nm]</td>
<td>150</td>
<td>130</td>
<td>115</td>
<td>100</td>
<td>90</td>
<td>80</td>
<td>70</td>
</tr>
<tr>
<td>NOR highest W/E Voltage[V]</td>
<td>8-10</td>
<td>8-10</td>
<td>8-10</td>
<td>8-10</td>
<td>7-9</td>
<td>7-9</td>
<td>7-9</td>
</tr>
<tr>
<td>NAND highest W/E Voltage[V]</td>
<td>19-21</td>
<td>18-20</td>
<td>18-20</td>
<td>18-20</td>
<td>17-19</td>
<td>17-19</td>
<td></td>
</tr>
<tr>
<td>NOR tunnel dielectric thickness[nm]</td>
<td>9.5-10.5</td>
<td>9.5-10</td>
<td>9-10</td>
<td>9-10</td>
<td>8.5-9.5</td>
<td>8.5-9.5</td>
<td>8.5-9.5</td>
</tr>
<tr>
<td>NAND tunnel dielectric thickness[nm]</td>
<td>8.5-9.5</td>
<td>8.5-9</td>
<td>8-9</td>
<td>8-9</td>
<td>7.5-8</td>
<td>7.5-8</td>
<td></td>
</tr>
<tr>
<td>NAND interpoly dielectric thickness[nm]</td>
<td>14-16</td>
<td>13-15</td>
<td>12-14</td>
<td>12-14</td>
<td>12-14</td>
<td>11-13</td>
<td>10-12</td>
</tr>
</tbody>
</table>

**Notes:**

- Solutions Exist
- Solutions are Known
- Solutions are NOT Known

What’s the limits of flash scaling?
Discrete traps

Discrete traps (SiN traps or Nanocrystal)

* SONOS (Silicon-Oxide-Nitride-Oxide-Silicon)
Motivation for SONOS

< Advantages >

- Compatibility of SONOS with CMOS with the use of thin nitride
- Lower programming voltage
- Smaller dimension capability than FG EEPROM
- Longer retention & low defect induced tunneling leakage (Nitride instead of poly Si)
- Higher programming speed (depends on ONO thickness)
# Comparison of Memory Technologies

<table>
<thead>
<tr>
<th></th>
<th>FRAM</th>
<th>MRAM</th>
<th>PRAM</th>
<th>SONOS</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Cell size</strong></td>
<td>8~25 F²</td>
<td>8~9 F²</td>
<td>6 F²</td>
<td>4~10 F²</td>
</tr>
<tr>
<td><strong>Read time</strong></td>
<td>30~200 ns</td>
<td>10~100 ns</td>
<td>10~100 ns</td>
<td>20~120 ns</td>
</tr>
<tr>
<td><strong>Write time</strong></td>
<td>30 ns</td>
<td>10~15 ns</td>
<td>10~100 ns</td>
<td>1 µs ~ 1 ms</td>
</tr>
<tr>
<td><strong>Retention</strong></td>
<td>&gt; 10¹⁰</td>
<td>&gt; 10¹⁰</td>
<td>&gt; 10¹⁰</td>
<td>&gt;10¹⁰</td>
</tr>
<tr>
<td><strong>Endurance</strong></td>
<td>&gt; 10E12</td>
<td>&gt; 1E13</td>
<td>&gt; 10E13</td>
<td>&gt; 1E5</td>
</tr>
<tr>
<td><strong>Current/Power</strong></td>
<td>Low</td>
<td>High</td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td><strong>Cost</strong></td>
<td>High</td>
<td>High</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td><strong>Process</strong></td>
<td>Special</td>
<td>Special</td>
<td>Special</td>
<td>CMOS</td>
</tr>
<tr>
<td><strong>Issues</strong></td>
<td>Etching process Cost, Retention, Fatigue</td>
<td>Etching process Uniform thin films Cost</td>
<td>Power consumption</td>
<td>Thin Oxide film Faster P/E time</td>
</tr>
</tbody>
</table>
**SONOS Memory Development**

- **Channel Length:**
  - 130 nm (2001)
  - 70 nm (2002)
  - 30 nm (2003)

- **Source, Drain, Gate:**
  - 70 nm

Nano Lithography

Sidewall Patterning

Positive Resist: PMMA

Negative Resist: Calixarene
Si Nanoparticle Fabrication by Aerosol Laser Ablation

- D < 10nm
- \( \rho \sim 1 \times 10^{11} \, \text{cm}^{-2} \)

```
Concentration (cm\(^{-3}\))
```

```
Nanoparticle Size (nm)
```

![Graph showing concentration vs. nanoparticle size](image)

![Micrograph of Si nanoparticles](image)
30nm SONOS Memory by SWP

Key Features of SONOS Cell
- Memory Node Size: 30 x 30 nm²
- Write/Erase Voltage: <10V
- Write/Erase Time: 1 msec
- Endurance: >10⁶ cycles
- Retention = 1 year @ T=85°C

ONO=23/120/45 Å

Threshold Voltage [V] vs Write/Erase Time [Sec]

Key Characteristics of SONOS Memory

- Drain Current [A] vs. Vds [V]
  - ONO=23/120/45 Å
  - Vth=-0.05V
  - W/L=30nm/30nm
  - S.S = 89mV/dec
  - DIBL = 105mV
  - Vth=0V

- Vth (V) vs. Cycles (number)
  - At 85°C
  - Program state
  - Erase state

- Vth vs. Time [sec]

SONOS Memory by E-beam Lithography

SONOS Cell by E-beam Lithography

W/L : 33nm / 46nm
ONO layer TEM & AES Analysis

- TEM of the ONO (2 nm/7 nm/9 nm) stack
- Auger profile showing the stoichiometric of ONO layer.
Program & Erase Characteristics

- $\Delta V_{th} \sim 2.4V$
- Trapped Charge density = $4.1 \sim 5.9 \times 10^{12} \text{ cm}^{-2}$
- No. of $e^- = 61 \sim 88$ for 33nm x 46nm node size
• Memory window is nearly similar for SONOS devices with different memory node areas.
• Retention time is good with 75nm width and 100 nm length at 85°C.

• It remains unchanged up to $10^5$ cycles, indicating superior endurance characteristics at 85°C.
Memory Effect at 30 nm dimensions

- Single electron charging effect at 30 nm dimensions.
Vertical Channel SONOS

Schematic of VC SONOS

- $\Delta V_{th} = 1.6V$ @ 8/-8V & 10ms
TEM images

Source gate drain

CVD oxide
Vertical channel

Gate

Source

Drain

Contact

Vertical channel bulk
Future Work

- Nano fabrication process for Integration
- Improvement of SONOS memory characteristics
  - High-k materials
  - New memory cell structure
  - Optimal bias conditions
- Device physics
  - Single electron effect
  - Reliability failure mechanism
  - Memory cell Modeling/Simulation