An Intel Perspective on Silicon, Nanotechnology and Microelectronics

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Intel Research & Development

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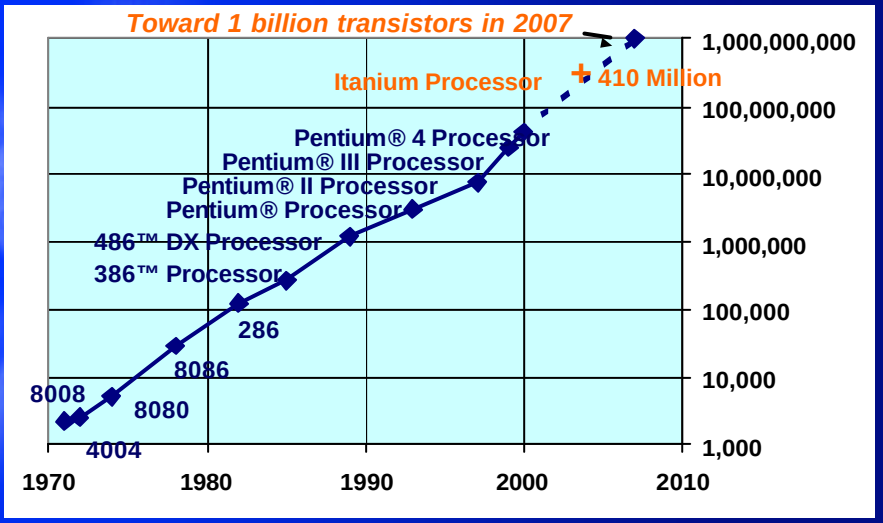
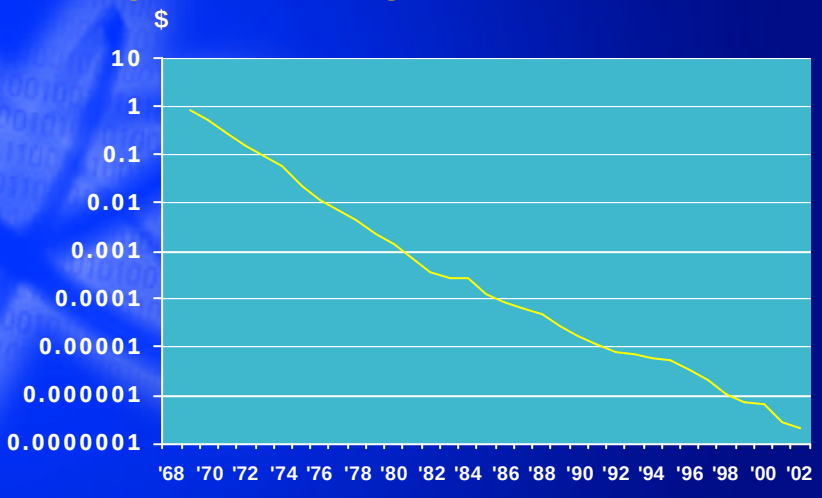
Agenda

- Moore's law is alive and well
- Dramatic cost reduction continues
- Silicon Nanotech is a production reality
- Silicon Nanotech is extendable through 2015
- Non-silicon features will integrate with silicon
- We are open-minded about options beyond 2015
- Complementary technologies
- Collaboration between industries, universities, and governments is essential

Moore's Law Continues



Transistor cost decreases, driving increasing investments



Source: WSTS/Dataquest/Intel, 8/02

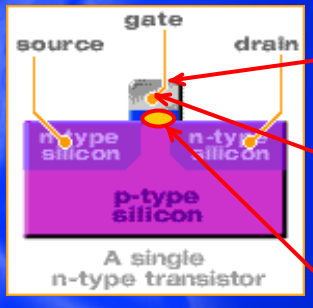
What is nanoscale science, engineering, & technology?

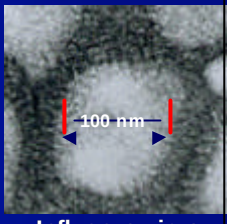
- "Research and technology development at the atomic, molecular or macromolecular levels, in the length scale of approximately **1 - 100 nanometer** range, to provide a fundamental understanding of phenomena and materials at the nanoscale and to create and use structures, devices and systems that have novel properties and functions because of their small and/or intermediate size."
  - Dr. Mike Roco, National Science and Technology Council, February 2000)

Intel's chip technology has novel properties, both because of its small size, and specific nanoscale design strategies

90 nanometer technology

Nanodesign Strategy - Focus on controlling interfaces and monolayers
Surface preparation is key





Influenza virus
Source: CDC

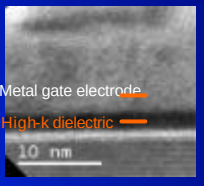
1.2 nm gate oxide is ~5 Silicon atom layers thick!

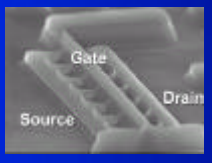
"Strained Silicon" - Separating the Silicon Atoms for Faster Electron Flow

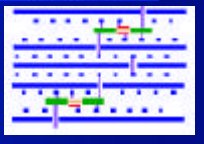
Intel's current technology exploits the novel properties that are found at very small dimensions, by manipulating processes and materials at the nanoscale, to create nanoscale devices

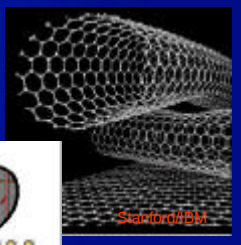
Physical limits

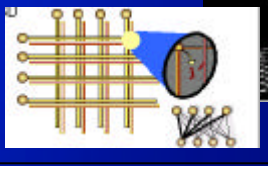
- Next 10 years- No fundamental changes in CMOS down to 10nm
  - Expect new
    - materials,
    - processes
    - Structures
- After 2015
  - Open minded on options
  - Scalable quantum devices
  - Co-existence with Silicon
- Many funding gaps exist

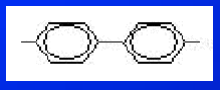










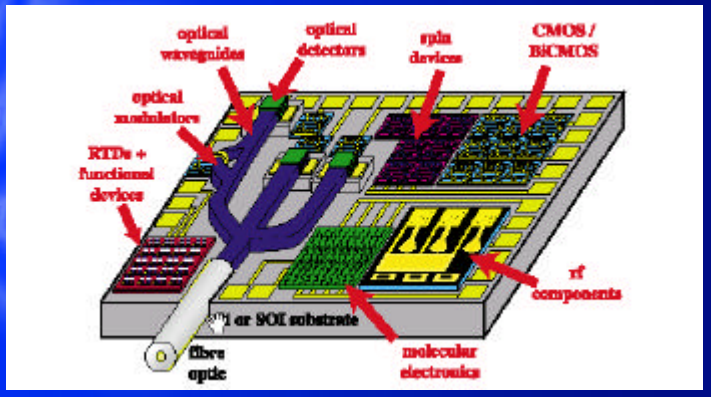


Going Beyond CMOS: Drivers and Approaches

- **Required characteristics:**
  - Scalability
  - Performance
  - Energy efficiency
  - Gain
  - Operational reliability
  - Room temp. operation
- **Preferred approach:**
  - CMOS process compatibility
  - CMOS architectural compatibility

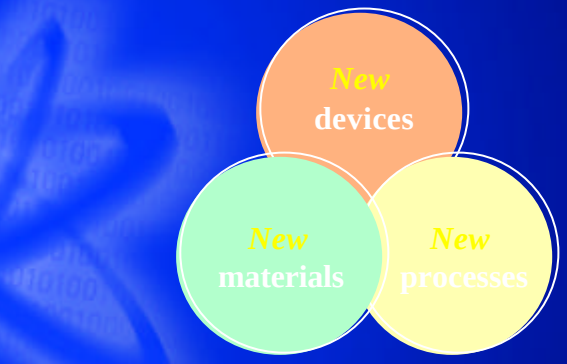
- **Alternative state variables**
  - Spin–electron, nuclear, photon
  - Phase
  - Quantum state
  - Magnetic flux quanta
  - Mechanical deformation
  - Dipole orientation
  - Molecular state
  - …

Heterogeneous integration of alternative technologies



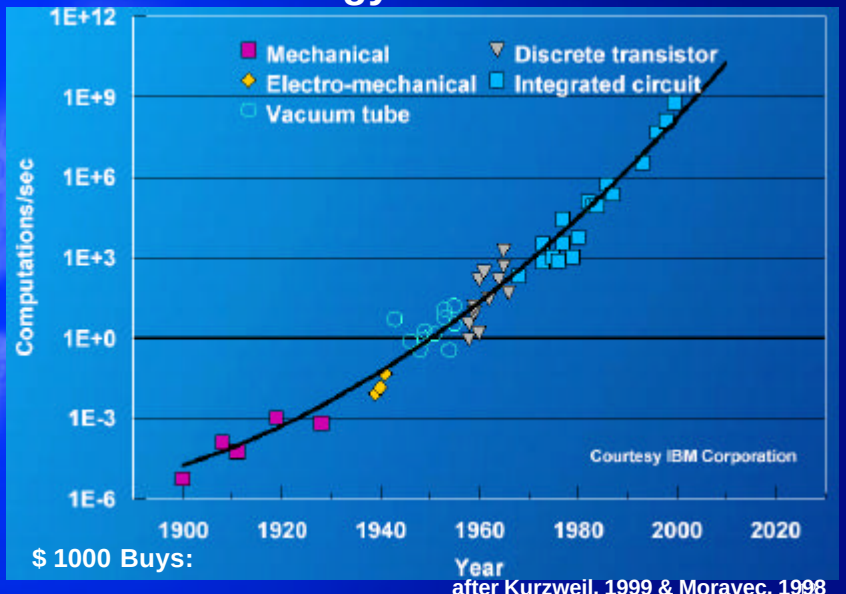
European Technology Roadmap for Nanoelectronics

Major Acceleration in Materials, Processing and Devices Required



12 years is a short time for major breakthroughs

Complementary vs. Disruptive Technology Transitions



after Kurzweil, 1999 & Moravec, 1998

New scalable quantum technologies will first find niches on silicon for specialty applications in the future. They will complement, not disrupt, silicon based technology

Collaboration between industries, universities, and governments will be essential

Acknowledgments

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A host of researchers whose open literature material is included