Process-Based Cost Modeling of Photonics Manufacture: The Cost Competitiveness of Monolithic Integration of a 1550-nm DFB Laser and an Electroabsorptive Modulator on an InP Platform

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***Abstract*—The monolithic integration of components holds promise to increase network functionality and reduce packaging expense. Integration also drives down yield due to manufacturing complexity and the compounding of failures across devices. Consensus is lacking on the economically preferred extent of integration. Previous studies on the cost feasibility of integration have used high-level estimation methods. This study instead focuses on accurate-to-industry detail, basing a process-based cost model of device manufacture on data collected from 20 firms across the optoelectronics supply chain. The model presented allows for the definition of process organization, including testing, as well as processing conditions, operational characteristics, and level of automation at each step. This study focuses on the cost implications of integration of a 1550-nm DFB laser with an electroabsorptive modulator on an InP platform. Results show the monolithically integrated design to be more cost competitive over discrete component options regardless of production scale. Dominant cost drivers are packaging, testing, and assembly. Leveraging the technical detail underlying model projections, component alignment, bonding, and metal–organic chemical vapor deposition (MOCVD) are identified as processes where technical improvements are most critical to lowering costs. Such results should encourage exploration of the cost advantages of further integration and focus cost-driven technology development.**

***Index Terms*—Indium compounds, lasers, manufacturing economics, modeling, monolithically integrated circuits.**

I. Introduction

THE PAST four years have seen the optoelectronics industry transform from one dominated by the speed and performance of innovation to one where efficiency and cost play a determinant role in a company's future. The collapse of the optical fiber market and the burst of the Internet bubble in 2000 were a driving force behind this transformation. By 2002, actual optical fiber sales fell short of 24-month projections by more than 80% [1], [2] (see Fig. 1). This protracted difference between projected and actual sales belies a market dynamic sufficient to change both the operating climate and the strategies of stakeholders throughout the industry.

In response to such changes, optoelectronics firms began turning to economic methods, such as cost of ownership models, to support technical decisions. Although the field of activity-based costing and other process-based cost research [3] has extended these methods to include the implications of both nonmanufacture and individual process activities, current costing approaches lack a critical capability for an industry with rapid technology turnover. Critical to such an industry is the ability to forecast the cost implications of technology advances—in the form of new materials, processes, or architectures—while those advances are still in their early stages of development. For an industry like optoelectronics, early stage understanding of economic implications will be essential to realizing new market potential and avoiding inefficient development.

Process-based cost modeling (PBCM) (or technical cost modeling) was developed to address just such a problem, serving as a method for analyzing the economics of emerging manufacturing processes without the prohibitive economic burdens of trial and error innovation [4]. Its application has been extended to the implications of alternative design specifications and process operating conditions on production costs within and across manufacturing processes [5]. In the same way that present-day engineering models allow designers and manufacturing engineers to understand the physical consequences of their technical choices before those choices are put into action, technical cost models harness the engineering approaches at work within these physical models to avoid expensive strategic errors in product development and deployment.

A precedent exists for using PBCM to look at the cost implications of electronics technologies still in their early stages of development. The Materials Systems Lab at MIT has shown PBCM to provide key decision insights in electronic packaging [6], printed circuit board design [7], [8], and materials selection

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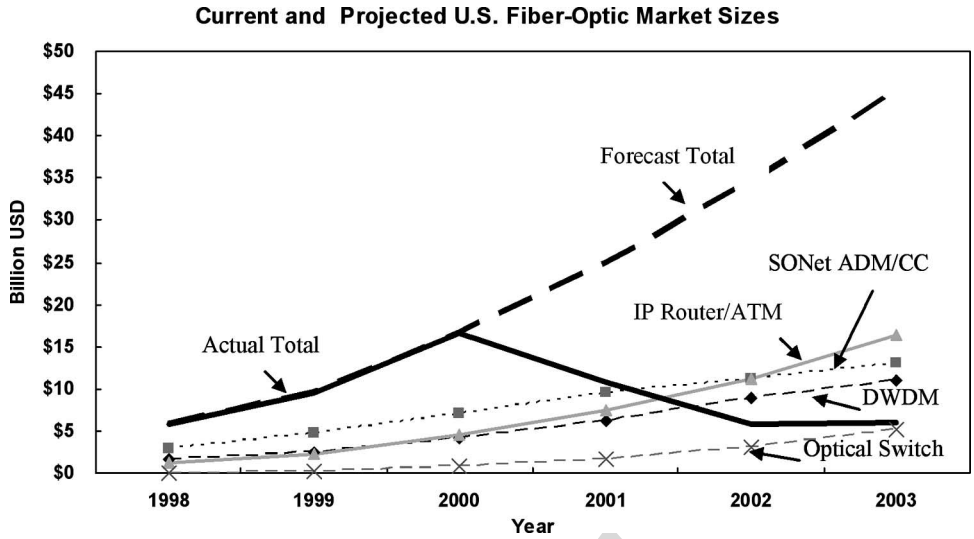

Fig. 1. Mid-2000 optical communications market forecast [1] versus actual sales [2].

for integrated circuit applications [9]–[11]. This paper has been extended by Sandborn to look at early stage design decisions in electronics system assembly [12], [13]. Recently, the need for costing methods that can assess the cost implications of emerging design alternatives has also been identified for the optoelectronics industry. The National Electronic Manufacturers Initiative (NEMI) has begun a cost analysis of optical versus copper backplanes using the PBCM approach. However, progress has been slow, and so far only a cost model of the copper backplane exists [14]. A yield-focused costing approach for evaluating emerging technologies also independently emerged in the late 1990s, focused on optoelectronic devices [15], [16]. This approach is strongly based in theoretical yield models—calculating the yield impact of design changes on thermal dissipation, mechanical expansion and stress, and optical coupling efficiency [16]. This paper relies on models built around plant-level performance data, leading to different results from these previous theoretical analyses.

This paper presents the application of PBCM to the economic questions associated with optoelectronic device production. The work focuses on the feasibility of a particular technology solution—monolithic integration—for meeting the industry's need to drive down costs. The monolithic integration of separate components on a single device not only is believed to minimize packaging expenses but also holds promise to increase network speed and device functionality. However, problems arising from increasingly structured wafer surfaces and increased opportunities for defects during the extended process flow of a monolithic device [17] cause concerns that yield losses will outweigh cost savings. Modeling results are used to demonstrate the importance of yield losses along with several other technological and operational characteristics of device production. The model that is described represents a broad-scope PBCM developed as an element of the MIT Communications Technology Roadmapping Project (CTR) [18] for the optoelectronics components industry. This PBCM is based on data collected during a 1.5-year period (September 2003 to January 2005) from 20 firms across the optoelectronics supply chain located in the U.S., the U.K., and developing East Asia. The cost results that follow are based on the processing conditions found in the U.S.- and U.K.-based manufacturing facilities. The impact of manufacturing in developing East Asia on the cost competitiveness of monolithically integrated designs is explored in a separate paper [19]. Although the model was developed around a specific InP device case, the aim was to develop a model architecture easily expanded to address new designs, processes, and materials as might be relevant to future questions facing the optoelectronics industry.

II. Model Architecture

CTR PBCM allows the user to project and analyze optoelectronics production cost. The model, using basic engineering principles and industry data, first estimates required processing conditions. These estimates are used to project the resource requirements—capital, labor, materials, and energy—needed to meet specified production targets. These resource requirements can be mapped to corresponding operating and investment expenses and then aggregated into unit cost figures as detailed subsequently. Ultimately, the model projects the minimum efficient fabrication line that is capable of producing a defined annual volume of good devices and then calculates the cost of installing and operating that line. The scale of the line is determined by the gross devices (both acceptable and rejected) that must be processed to achieve the desired annual volume of good units.

The cost per good device is developed in (1)–(17). Aggregate costs are calculated as

$$C_{\mathrm{Tot}} = C_{\mathrm{Material}} + C_{\mathrm{Labor}} + C_{\mathrm{Energy}} + C_{\mathrm{Equipment}} + C_{\mathrm{Tooling}} + C_{\mathrm{Building}} + C_{\mathrm{Overhead}} \quad (1)$$

$$C_{\mathrm{El}} = \frac{\mathrm{AC_{El}}}{\mathrm{PV}} \quad (2)$$

where C represents the unit cost (per good unit), AC the annual cost (per year), PV the good devices per year, and El the cost element (materials, labor, energy, equipment, tooling, maintenance, and overhead).

TABLE I
FRONT-END PROCESS MODULES IN THE TRANSMITTER PBCM

Surface Treatment	Growth/ Deposition	Etch	Lithography	Thermal
Clean	MOCVD	Plasma Etch	HMDS	Cure
Device Labeling	MBE	Asher	Spin-On Resist	Anneal
	PECVD	RIBE	Pre-Bake	
	H-Ion Implant	Wet Etch	Litho (Photo/UV)	
		Spin-Dry	Develop	
		Descum	Post-Bake	
		E-Beam Evap.		
		Metal Lift-Off		
		Lapping		

TABLE II
CLEAVING AND BACK-END PROCESS MODULES IN THE TRANSMITTER PBCM

Backend Assembly	Backend Package	Backend Test
Wafer Cleave	Alignment	Incoming Inspection
Bar Cleave	Bake	Post-Deposition Test
HR Coating	Lidding & Lid Check	Automatic Inspection
AR Coating	Package Clean	Plant Transfer Test Set
Bench Attach	Fiber Attach	Post Wire-Bond Visual
Cooler Assembly	Sleeve Attach	Final Chip on Carrier Visual
Chip Bond		Assembly Visual
Wirebond		Pre-Lid Visual
Burn-In		Post-Ash Visual
Bench Assembly		Chip-On Carrier Test
		Cooler Assembly Test
		Post-Bake Test
		Temperature Cycle
		Final Package Test

TABLE III
PROCESS SUBMODEL INPUTS (REQUIRED FOR EACH PROCESS STEP)

Process: (e.g., MOCVD)		
Incidental Yield	Direct Labor: Higher Ed.	Operating Time Per Batch
Embedded Yield	Direct Labor: Technician	Setup Time Per Batch
Machine Cost	Direct Labor: Skilled	Maintenance Freq. (/batch)
Capital Dedication (Y/N)	Direct Labor: Unskilled	Maintenance Time
Capital Usage Life	Installation Cost (%)	Tool/Mask Initial Investment
Max. Batch Size	Maintenance Cost (%)	Tool/Mask Add'l Unit Cost
Average Batch Size	Auxiliary Equipment (%)	High-Grade Cleanroom Space
Unplanned Downtime	Energy Consumption (kWh)	Low-Grade Cleanroom Space
		Non-Cleanroom Space

The cost projections in this paper are based on a detailed description of component processing including front-end component fabrication, assembly, packaging, and all forms of testing. Model users have full flexibility to define the type and order of process steps as well as set the operating conditions for each process module. Currently, the model comprises 52 submodels each covering a different process. The user identifies from these options both the types and order of processes required to produce the desired device. The 52 processes (including testing processes) included in the model are shown, classified by process function, in Tables I and II.

In defining the process flow necessary to produce a device, process type and order must by augmented by a description of the materials, actions, and operating conditions occurring at a given process step. In the model, the user may choose from one of several preset operational descriptions provided for each process, or may enter his or her own recipe for the model to use at that process step. In all cases, these operational descriptions are created from the 26 inputs shown in Table III.

A. Materials, Labor, and Energy Costs

The model currently tracks a range of materials, which are either incorporated into the product or used as consumables (e.g., cover gases). Each process module allows the user to specify the rate of consumption of these materials per production batch for that step. For some steps, these material consumption rates are forecast from descriptions of the product, but can be overridden by user input. Regarding primary wafer consumption, users may specify the density of chips that are processed on one wafer. Previous work has suggested there are wafer real estate benefits to system on chip solutions [20], [21]. In the firms studied, the authors found wafer handling requirements to limit the minimum chip size for the case studied in this paper. Based on this observation, the analysis presented assumes the same component density per wafer regardless of whether the component is a laser, modulator, or monolithically integrated laser modulator.

Ultimately, material costs are directly driven by the effective production volume for each step (effPV_i), defined as the gross number of units processed at step i to achieve the desired number of good units (PV) after step n. The calculations for effective production volume and material costs are

$$\text{effPV}_n = \text{PV}/Y_n \tag{3}$$

$$\text{effPV}_i = \text{effPV}_{i+1}/Y_i \quad \forall i \in [1, \ldots, n-1] \tag{4}$$

$$\text{effAB}_i = \text{effPV}_i/\text{Batch}_i \tag{5}$$

$$\text{AC}_{\text{Material}} = \sum_{i,m} U_i^m \cdot \text{effAB}_i \cdot P^m \tag{6}$$

where i is the process step number, n is the total number of process steps, Y_i is the yield at step i, effAB_i is the gross annual batch processed at i, Batch_i is the mean batch size for i, m is the material type, P^m is the unit price of material m, and U_i^m is the unit usage of material m per Batch_i.

Energy costs are based on user-specified energy consumption rates for each machine. Energy consumption values are estimated for each process according to equipment requirements, leading to annual energy costs calculated as

$$\text{AC}_{\text{Energy}} = \sum_i \text{reqLT}_i \cdot \text{EI}_i \tag{7}$$

where EI_i is the energy intensity of step i in kilowatts and reqLT_i is the line time required to produce effPV_i.

Users may specify direct labor requirements in four separate classifications, namely 1) higher education labor, 2) technicians, 3) skilled labor, and 4) unskilled labor. The annual cost of these laborers is computed as

$$\text{AC}_{\text{Labor}} = \sum_{i,l} \text{APT}_i^l \cdot P^l \tag{8}$$

where l is the labor type (Ph.D., technician, skilled, unskilled) and APT_i^l is the annual paid labor time for labor type l for step i.

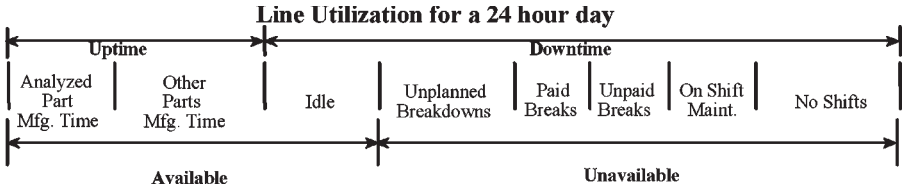

Fig. 2. Computation of available operating time based on line utilization for a 24-h day.

B. Capital Costs

A key element of any cost forecast is the method used to allocate nonuniform cash flows to appropriate activities, here the production cost of a specific component. In the CTR PBCM, costs are assumed to be distributed evenly in time over the usable lifetime of a resource for those cash flows with periodicity longer than one year (e.g., equipment investments). The opportunity cost associated with tying up these funds in this long-term investment is incorporated using a standard capital recovery factor [22]

$$R_{\mathrm{El}} = I_{\mathrm{El}} \frac{[d(1+d)^{s_{\mathrm{El}}}]}{[(1+d)^{s_{\mathrm{El}}}-1]} \qquad \forall\, \mathrm{El} \in \mathbb{Z} \tag{9}$$

where $\mathbb{Z} = \{\mathrm{Tool}, \mathrm{Equipment}, \mathrm{Building}\}$, $R =$ the allocated cost for a defined period (here, one year), $I =$ the nonperiodic investment to be allocated, $d =$ the periodic discount rate (here, $d = 10\%$), $s =$ the number of periods over which is investment is distributed (here, $s_{\mathrm{Tool}} = 3$, $s_{\mathrm{Equipment}} = 10$, and $s_{\mathrm{Building}} = 25$).

Along with each machine's direct cost, an input is provided to establish whether the machine is (a) dedicated to the production of the product being analyzed or (b) shared across other products. In the latter case, following the approach of time-based allocation, investment expense is apportioned according to the fraction of equipment available time that is dedicated to the manufacture of the component of interest. The details of this forecast are described in Section II-B1. For the purposes of the case analysis presented subsequently, the model was configured based on an assumption that even if a production line is dedicated to a single product, processes that require the same equipment in that production line will choose, when possible, to run on the same machine. This approach was based on observation of industry practice and recognition of the exceptionally low utilization that would result otherwise for low production volume high-performance products. Based on this approach, fixed costs are calculated as

$$\mathrm{AC}_{\mathrm{El}} = \mathrm{AC}_{\mathrm{El,ded}} + \mathrm{AC}_{\mathrm{El,nonded}} \qquad \forall\, \mathrm{El} \in \mathbb{Z} \tag{10}$$

$$\mathrm{AC}_{\mathrm{El,nonded}} = \sum_i (R_{\mathrm{El},i} * \mathrm{LR}_i) \qquad \forall\, i \in \{\mathrm{nondedicated}\} \tag{11}$$

$$\mathrm{AC}_{\mathrm{El,ded}} = \sum_j R_{\mathrm{El},j} \left(\left\lceil \sum_i (\mathrm{LR}_{ij} - \lfloor \mathrm{LR}_{ij} \rfloor) \right\rceil + \sum_i \lfloor \mathrm{LR}_{ij} \rfloor \right) \qquad \forall i \in \{\mathrm{dedicated}\} \text{ and } \forall j \in [1, \ldots, J] \tag{12}$$

where {nondedicated} represents the set of all steps that have nondedicated processes, {dedicated} represents the set of all steps that have dedicated processes, j is the process type, J is the total number of process types, and LR_i is the ratio of required operating time to effective available operating time at step i, as shown in the next section.

1) Operating Time: The time required for a given process step is a key determinant of many process costs, including labor, energy, and capital requirements. Three quantities of time are tracked within any PBCM: 1) amount of time that a particular resource (machine, labor, etc.) is required—required operating time, 2) amount of time that a unit of that resource is available in a given year—available operating time, and 3) amount of time that a laborer would be paid for a full year—annual paid labor time.

Several factors influence the required operating time, including 1) operating time per batch, 2) setup time per batch, 3) machine simultaneous preparation capacity (i.e., maximum batch size), 4) typical simultaneous preparation, 5) maintenance frequency, and 6) maintenance duration.

The annual available operating time is required to compute the number of parallel resources necessary to meet production targets. Several operations metrics for a facility must be integrated to compute the available operating time, including unplanned breakdowns, worker breaks, maintenance time, and the time when the facility is not operating (see Fig. 2). To properly allocate the cost of inefficient capital utilization, the available operating time should be modified by also subtracting that time when the plant is operational and staffed but is not producing due to lack of demand (i.e., idle time). This modified quantity, referred to as effective annual available operating time, is shown to the right in Fig. 2.

Annual paid labor time, lines required, required operating time, and available operating time are calculated as

$$\mathrm{APT}_i^l = \mathrm{DPY} \cdot (24 - \mathrm{NS} - \mathrm{UB}) \cdot \mathrm{WPL}_i^l \cdot \mathrm{LR}_i \tag{13}$$

$$\mathrm{LR}_i = \mathrm{reqLT}_i / \mathrm{availLT} \tag{14}$$

$$\mathrm{reqLT}_i = \mathrm{effAB}_i \cdot (\mathrm{cycT}_i + \mathrm{suT}_i) \tag{15}$$

$$\mathrm{availLT} = \mathrm{DPY} \cdot (24 - \mathrm{NS} - \mathrm{UB} - \mathrm{PB} - \mathrm{UD}) \tag{16}$$

where DPY represents the operating days per year, NS represents no operations (hours per day the plant is closed), UB represents the unpaid breaks (hours per day), WPL_i^l represents the fractional labor type l assigned to step i, cycT_i represents the operating cycle time of i per batch, suT_i represents the setup time of process i per batch, PB represents the paid breaks (hours per day), and UD represents the unplanned downtime (hours per day).

For some processes, selected time quantities are not user inputs, but instead are computed based on descriptions of the product or desired operating conditions. For example, set up time can be correlated to the extent of automation of the machine and operating time per batch can be modeled from processing or product requirements such as thickness deposited, number of wires in wire bond, or type of epoxy and temperature of oven.

2) Yield: The unit costs (C_{Tot}) reported in this paper represent what is often known in the industry as "yielded costs," in other words the effective cost per good nondefective device. Unlike classic industry models, two yield numbers are assigned to each step in the process flow—an incidental yield and an embedded yield. Both of these yield values are inputs provided for each step by the user. The incidental yield represents the yield hit taken immediately at a given step due to obvious problems that can be identified without testing (e.g., occasional wafer breakage). The embedded yield represents defects caused within a process step but not discarded from the production line until later when identified as defective during testing. Thus, embedded yields accumulate during production until they are identified and removed during a testing step. Although only process steps that are not test steps can have embedded yields, test steps may have their own incidental yield. Equation (17) shows how yield (Y_i) would be calculated for some step $i = k$, where $k \in [0, \ldots, n]$, i.e.,

$$Y_{i=k} = \begin{cases} \mathrm{inc}Y_k \cdot \displaystyle\prod_{x=(t^*+1)}^{k} \mathrm{emb}Y_x, & k = \text{test} \\ \mathrm{inc}Y_k, & k \neq \text{test} \end{cases} \tag{17}$$

where $\boldsymbol{t}^* = \max \Im, \forall \boldsymbol{i} \in \{\text{test}\}$, where $\Im = \{\boldsymbol{i}\}_{i=1}^{k-1}$ and $\{\text{test}\}$ represents the set of steps that are test steps. In words, $\boldsymbol{t}^*$ is the most recent step prior to k that was a test. The user inputs incidental yield $(\mathrm{inc}Y_i)$ and embedded yield $(\mathrm{emb}Y_i)$ for all i. Assuming a total of n steps in the process flow, the cumulative yield $Y_{\mathrm{Cumulative}}$ can be calculated as

$$Y_{\mathrm{Cumulative}} = \prod_{i=1}^{n} Y_i. \tag{18}$$

The yields (Y_i) used for the analysis presented in this paper are based on the yields the studied firms were able to achieve post-rework. Future modeling efforts to integrate the direct cost of rework would be a useful extension of this analysis.

III. Case Study

The main goal of this study has been to develop a model whose architecture will become the foundation for investigating future techno-economic questions facing the optoelectronics industry. Particularly important is for the model to provide insights on the cost feasibility of integrating separate components on a single device. Limits of time and resources required choosing a single case from which future studies and model developments could be built. Three attributes are particularly important in the case chosen for study, namely 1) the case provides insights on a large range of processes necessary in optoelectronic chip production, 2) the case focuses on emerging but extant technology for which significant data are available within the industry (i.e., from which to develop models of relevant processes and against which model results can be calibrated), and 3) the case addresses a key integration decision being faced by firms. In light of these criteria, production of a 1550-nm DFB laser and an electroabsorptive modulator on an InP platform was chosen as the case for study. This laser modulator is designed for use in long- and short-haul STM-64/OC-192 time-division multiplexing applications over 40, 60, and 80 km with low dispersion penalty (less than 2 dB). Such a laser modulator would be suitable for use in SONET and SDH ($\sim$ 9.953 Gb/s), and as a Digital Wrapper ($\sim$ 10.3 Gb/s), with FEC ($\sim$ 10.7 Gb/s) (Table IV).

TABLE IV
Exogenous Financial Parameters Used in Case Study Analyses

Facility Description		
Working Days per Year	240	Days / Year
Facility Downtimes:		
No shifts	7	Hours / Day
Worker unpaid breaks	1	Hours / Day
Worker paid breaks	1.2	Hours / Day
Unplanned	*Set in process specifications*	
Cost of Building Space		
High Grade Cleanroom	$3,000	$ / m^2
Low Grade Cleanroom	$2,000	$ / m^2
Non-cleanroom	$1,000	$ / m^2
Building Maintenance (% fc)	5.0%	% Fixed Cost
Indirect workers/ Direct Worker	0.250	
Indirect workers/Line	1.000	

Three scenarios around this case were investigated, namely 1) a discretely packaged 1550-nm InP DFB laser and a discretely packaged electroabsorptive modulator, 2) a discrete 1550-nm InP DFB laser and a discrete electroabsorptive modulator within a single package, and 3) a 1550-nm InP DFB laser and an electroabsorptive modulator monolithically integrated on a single device. The 182-step, 165-step, and 111-step process flows for production of the 1) discretely packaged laser and discretely packaged modulator designs, 2) discrete laser and modulator in a single package, and 3) monolithically integrated are shown at the end of the document. All three scenarios are intended to represent the production of functionally equivalent 10-Gb/s devices with stringent quality specifications. All three product scenarios were modeled using a common set of operational and financial conditions as listed in Tables I and II.

Data for both the processes and the process flows relevant to these cases were collected from 20 firms across the optoelectronics supply chain, including end users, original equipment manufacturers (OEMs), and equipment manufacturers. These data were aggregated to construct a scenario illustrative of general industry practice. The process flow and process information for case 1 (discrete devices in discrete packages) was derived based on information collected about case 2 (discrete devices in a single package). As such, it likely represents an upper bound of cost and a lower bound of yield for case 1.

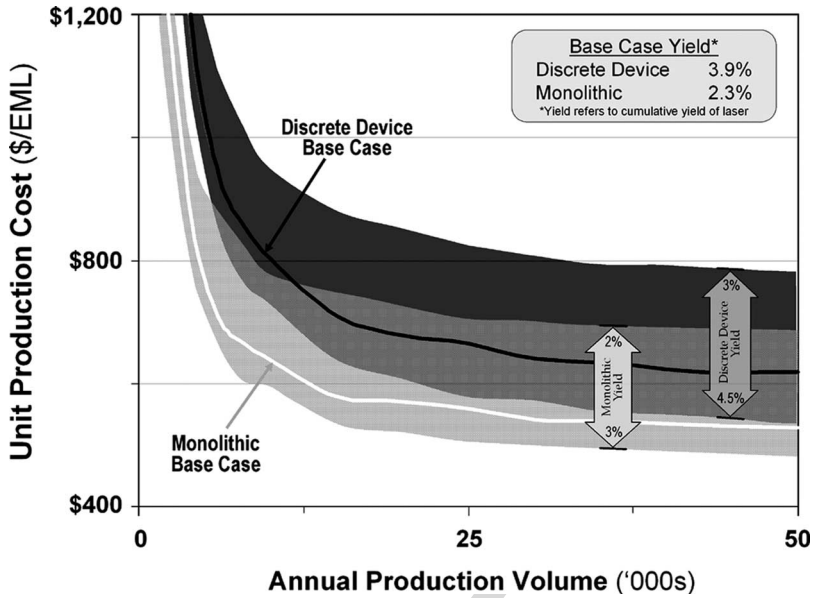

Fig. 3. Cost sensitivity of production volume analysis to final product yield. (For this analysis, the yield Y_n of the final step was varied to create the cumulative yields $Y_{\mathrm{Cumulative}}$ reported. In both of these process flows, the final step is a test.)

The following section details the use of CTR PBCM to map the technological and strategic characteristics of the tradeoff between packaging gains and processing losses for discrete and integrated designs of a 1550-nm DFB laser and an electroabsorptive modulator realized on an InP platform. Particular focus is paid to three economic aspects of this problem, namely 1) quantifying the impact of production scale growth, 2) identifying cost drivers, and 3) quantifying process performance levels necessary to achieve production cost targets.

A. Quantifying the Impact of Production Scale Growth

A critical economic characteristic of any technology is the manner in which its production costs change as a function of total units produced. A PBCM forecasts this change in production costs with scale by first determining the minimum efficient fabrication line that is capable of producing a given quantity of good devices and then inferring the cost of operating that line. Fig. 3 shows such an analysis for the laser modulator design options. To generate these results, the model projects technical and operational characteristics of the smallest efficient fabrication and assembly facility capable of meeting the production volume (of good devices) enumerated along the x-axis.

The reported cost figures represent the operating and allocated capital expenses associated with that facility and the product of interest. All three design options, namely 1) a discretely packaged 1550-nm InP laser and a discretely packaged modulator (discrete package), 2) a discrete laser and a discrete modulator within a single package (discrete device), and 3) a monolithically integrated 1550-nm InP laser modulator (monolithically integrated), showed strong economies of scale up to annual production volumes of approximately 30 000 units. At annual volumes above 30 000 units, the production costs of all three devices become effectively insensitive to production scale. The unit cost of the monolithically integrated electroabsorptive modulated laser (EML) levels out at just above $500 per unit, the discretely produced devices within a single package level out at a cost just below $600 per unit, and the discretely packaged devices level out at a cost of around $850 per unit. The discrete device case (i.e., within a single package) showed the strongest sensitivity to scale, followed by production of discretely packaged devices. This relative behavior emerges because both discrete products require larger total investments compared to the monolithically integrated design. The monolithically integrated EML requires the least investment and therefore shows the least sensitivity to scale. The largest contributors to investment cost for each device can be seen in Table V. Because the discretely packaged devices were found to be cost inferior to the other two options at all production volumes, this scenario is left out of the analyses for the rest of this paper.

It may seem surprising that the model would project a smaller capital outlay (and corresponding less volume-sensitive unit cost) for the monolithic device despite its overall lower production yield; lower yield products require more units to be

TABLE V
LARGEST CONTRIBUTORS TO INVESTMENT FOR EACH DESIGN AT ANNUAL PRODUCTION VOLUMES OF 30 000 ANNUALLY

Design	Monolithically Integrated		Discrete Device		Discretely Packaged	
Total Investment	$61,037,000		$70,697,000		$102,436,000	
Top Contributor	Assembly Test	10.0%	Assembly Test	10.3%	Assembly Test	20.2%
	Device Test	8.5%	Device Test	9.7%	Alignment	11.3%
	Alignment	5.6%	Lithography	6.8%	Device Test	9.7%
	Lithography	4.9%	Alignment	5.6%	Lithography	6.8%
	Burn-In	2.9%	E-Beam Evap	4.5%	E-Beam Evap	4.5%
	E-Beam Evap	2.2%	Burn-In	2.9%	Visual Test	3.2%
	Visual Test	1.9%	Visual Test	2.6%	Bench Attach	2.9%
	Bench Attach	1.5%	Lapping	2.2%	Burn-In	2.9%
	Bench Assembly	1.5%	Chip Bond	1.8%	Bench Assembly	2.9%
	Lapping	1.5%	Bench Attach	1.5%	Sleeve Attach	2.5%

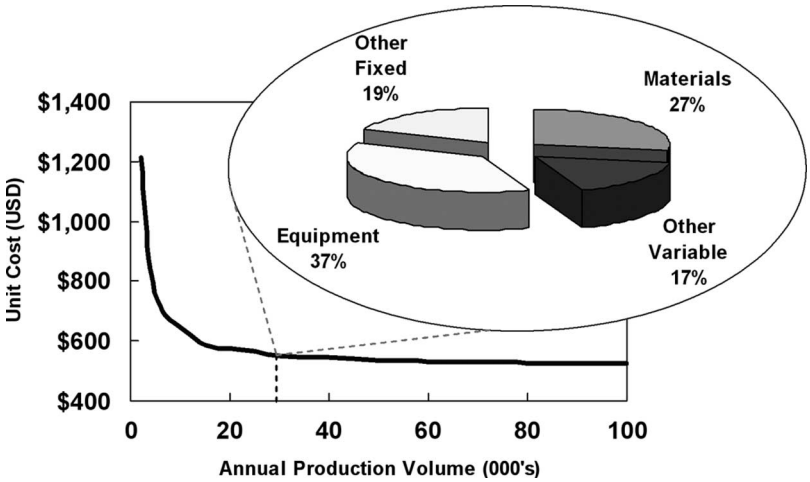

Fig. 4. Monolithically integrated laser-modulator device cost breakdown at 30 000 units annually.

processed that in turn drives higher equipment requirements. While the model does project that production of the monolithic device requires higher capital utilization than its discrete device counterparts, in all three cases, production requirements can usually be satisfied by a single piece of equipment across the range of production volumes being considered. As such, for many processing steps, the yield disadvantage of the monolithic device is insufficient to drive additional capital expenditure. However, there are a few processing steps that both have long cycle times (i.e., require multiple units of equipment) and must be repeated for each discrete component. Excellent examples of this are chip bonding and its associated testing operations. In these cases, the additional required instances of these processes in the discrete cases lead to additional capital requirements and the observed cost behavior.

Both the volume at which economies of scale are reached and the eventual cost at scale are dependent on the specific processing decisions and conditions faced by an individual plant. In the analysis shown in Fig. 3, testing occurs after six key intervals for the front end, after individual die isolation (bar cleave), and at five key locations during the back end processes (see Appendix, for specific locations). The final product yields achieved are 2.3% for the monolithically integrated device, and 3.9% and 7.9% for the discrete laser and modulator, respectively, in a single package. Because data for the discretely packaged devices are derived directly from information collected on case 2, the yields for this case match those of the discrete-device single-package case.

With yields in single digits, even slight improvements or digressions within individual process steps can have significant consequences. The impact of small yield changes on the final product cost can be seen for the monolithic and discrete device cases as the shaded areas in Fig. 3. The dominance of one case over the other is susceptible to the yields producers are actually able to achieve.

B. Identifying Cost Drivers

Although knowing the costs of alternative scenarios and how these costs vary with production scale is useful for strategic decision making, more detailed information is required for informed operational decisions and firm-wide efforts to reduce cost. PBCM addresses this issue by providing the user with a wide variety of scenarios under which to observe the dominant drivers of production cost. Knowledge of cost drivers enables the industry to focus scarce development resources on these dominant areas. The next five figures demonstrate the insights the CTR PBCM provides on the cost drivers in 1550-nm InP laser modulator production.

Fig. 4 provides an aggregate breakdown of costs for the monolithically integrated device at a production volume of 30 000 units per year. In this and the four subsequent figures, costs are grouped into four headings, namely 1) materials (including purchased packaging components), 2) labor (direct and indirect, both with benefits, but not managerial costs); 3) energy, and 4) equipment, and other fixed (comprising of building, maintenance, and overhead, with overhead including managerial overhead costs). For the monolithically integrated case, equipment represents the largest cost, accounting for nearly 37% of the total at this production volume. Equipment costs are followed by materials, which comprise almost 27% of the total cost.

Fig. 5 shows how the cost breakdown by element differs for the three alternative designs studied. Notably, the relative contribution of both the fixed (equipment, fixtures, building, maintenance, and overhead) and the variable (material, labor, and energy) is remarkably similar across different devices. Although material plays a slightly larger role, and labor and equipment a slightly smaller role for the discrete devices in a single package, the top two costs—equipment followed by material—remain the same for all three options.

Although an aggregate breakdown begins to identify the cost drivers—in this case the cost of equipment—to truly focus research and development efforts, it is necessary to further isolate the causes of cost. Figs. 6 and 7 do this by showing the cost impact of particular groups of processes within the overall production of each product. In comparing the two figures, it is interesting to note that although equipment and material dominate aggregate costs across all three designs, this domination of equipment and materials is not true for all processes.

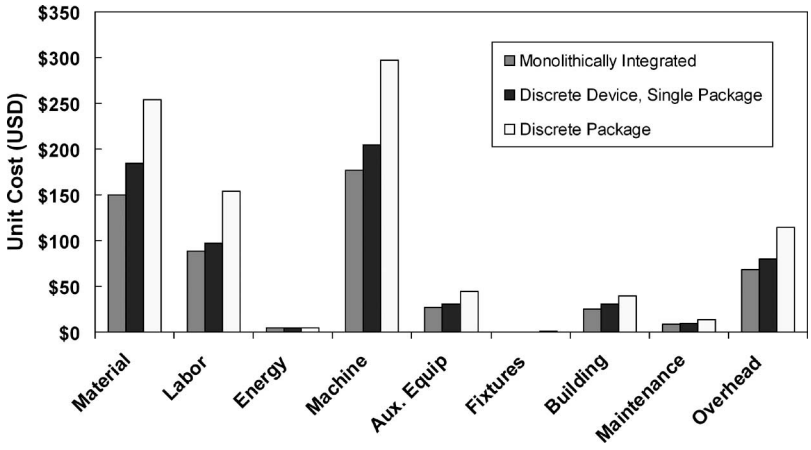

Fig. 5. Cost breakdown comparison at 30 000 units annually for different levels of integration.

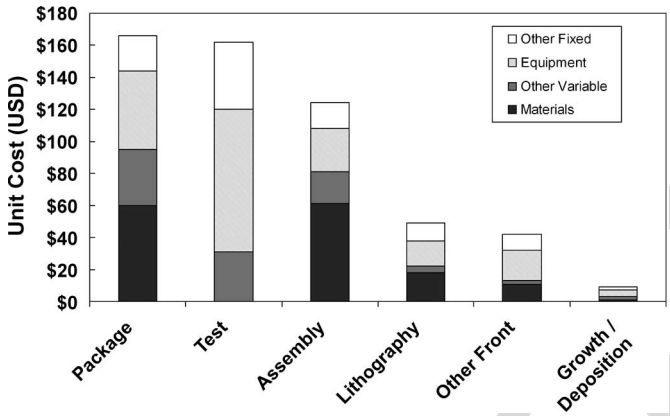

Fig. 6. Monolithically integrated device cost breakdown by process at 30 000 units annually.

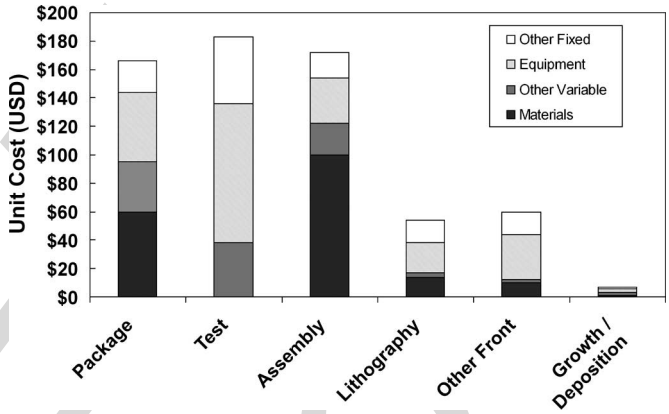

Fig. 7. Discrete-device single-package product cost breakdown by process at 30 000 units annually.

Fig. 6 shows that for the monolithically integrated EML, within-package assembly ("package") and testing ("test") make the largest contribution to production costs, followed by prepackage assembly (primarily the placement of the laser on the carrier). While testing is dominated by equipment costs, assembly, packaging, and lithography are dominated by material costs. Equipment costs dominate for testing due both to the expensive specialized groupings of equipment required and to the long testing times for which this equipment must be committed. Equipment costs are much less dominant in assembly and packaging, where much of this paper is often done by hand, requiring only microscopes with slight specialization. On the other hand, in these assembly and packaging stages, extensive parts from outside are required, which often come at high costs. Front-end processes other than lithography (but including epitaxial growth) are dominated by equipment costs.

In contrast to the monolithically integrated device in which testing and packaging are close to equal in cost, testing is the largest cost driver for the discrete devices in a single package, followed by prepackage assembly ("assembly"), and then package assembly ("package") (see Fig. 7). Testing continues to be dominated by equipment costs, and materials costs continue to be the largest contributors to costs during packaging and assembly. Although the significance of material costs for assembly within the package remains the same, the significance of material costs in prepackage assembly becomes 67% greater than they were for the monolithically integrated EML due to the assembly required on each separate device.

Because of the level of technical detail incorporated into CTR PBCM, it is possible to use the model to identify very detailed cost drivers. Fig. 8 demonstrates this capability, identifying the drivers of laser EML cost by individual processes. The top contributors to the overall costs for the monolithically integrated EML are, in decreasing order, alignment (i.e., microoptical alignment including the addition of lenses into the package), assembly stage testing, isolated die testing after transfer to back-end facility, chip bonding, fiber attachment, bench assembly, visual testing, bench attach, wire bond, and cooler assembly. Together, these ten processes account for 74% of the total product cost. Obviously, developmental efforts focused on eliminating costs within these steps will have a significant effect on the overall cost. It is also worth noting that there is great variety in the underlying causes of cost for each of these processes. Some processes are dominated by equipment costs [e.g., front to back testing, metal–organic chemical vapor deposition (MOCVD)], some by material costs (e.g., alignment, chip bond, fiber attach), and others by labor (e.g., assembly and visual test). Remarkably, these top ten cost drivers remain nearly the same across the differently integrated products.

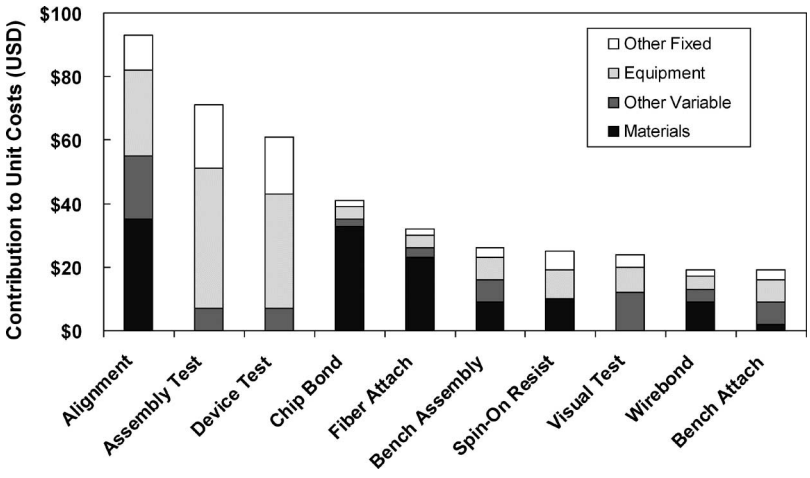

Fig. 8. Monolithically integrated EML top ten processes driving costs at 30 000 units annually.

TABLE VI
TOP TEN COST DRIVERS FOR DEVICES AT DIFFERENT LEVELS OF INTEGRATION

	Monolith Integrated	Discrete Device	Discrete Package
Alignment[1]	1	1	1
Assembly Tests	2	3	2
Device Test	3	4	4
Chip Bond	4	2	3
Fiber Attach	5	5	5
Bench Assembly	6	8	6
Spin-On Resist	7	6	10
Visual Test	8	9	7
Wirebond	9	10	9
Bench Attach	10		8
EBeam Evaporation		7	

[1] Alignment refers to micro-optical alignment including the assembly of lenses into the package.

Rankings of the top ten cost contributors for the discrete devices within a single package and for the discretely packaged device products can be seen in Table VI.

C. Quantifying Process Performance Targets

Because cost models build economic estimates up from the technical characteristics of a process, it is possible to use these models to investigate the impact of changing those characteristics. For the purposes of the optoelectronics industry, this capability can be particularly valuable in identifying processing performance targets (e.g., required yield, run rate, or materials consumption) and process steps on which to focus improvement efforts.

Along these lines, it is clear that per step yield is a primary driver of unit cost for the laser modulator device. Development efforts to improve that yield are critical, but should be targeted to achieve the greatest return on investment. However, guiding these efforts can be difficult because the efficacy of a particular process yield improvement depends on the current yield of that process, the frequency with which that process is repeated in the overall process flow, and on the specific positions in the process flow where that processing occurs. Nonetheless, despite the interrelationship of these effects, the operational detail of the MIT CTR model makes it possible to investigate the total cost effect of individual process yield changes.

Fig. 9 shows the direct impact of a change in selected process yields on unit cost for the monolithically integrated laser modulator. A change in alignment yield, whether an improvement or a set back, has the largest impact on unit cost. An alignment yield of only 94.5% versus one of 95.5% (the range shown in Fig. 9) adds over $10 to the final unit cost. MOCVD yield has the second largest impact on the final unit cost—changing cost by $7 for a change in yield between 91.5% and 92.5%. Notably, for a process like wire bonding, a reduction in wire bonding yield has the second largest impact on cost—the steepness of the curve being second only to alignment—while an improvement in wire bonding yield has the smallest effect on the final cost among the top ten the processes shown.

While informative, the analysis presented in Fig. 9 suggests that improvement efforts be ranked solely by their impact on unit cost. While important, this metric sheds no light on the underlying difficulty of realizing the required change in yield. To gain insight on this tradeoff, a second measure, known as the reject rate elasticity of total unit cost (ε_{r_j}), was calculated for each process in the production of the 111-step monolithically integrated laser modulator. The reject rate for each step (r_i) is calculated as

$$r_i = (1 - Y_i). \tag{19}$$

Because a process may be used at multiple steps in the production flow, the effective reject rate for process j(effr_j) was calculated as

$$\text{eff}r_j = \left(\prod_{q=1}^{Q_j} r_q \right)^{1/Q_j} \qquad \forall \text{ steps } q_j \in [1, \ldots, Q_j] \tag{20}$$

such that step q_j uses process j, and Q_j is the total number of steps using process j. The reject rate elasticity of the total unit cost (ε_{r_j}) can then be calculated as

$$\varepsilon_{r_j} = \frac{C' - C^o}{C^o} \Big/ \frac{\text{eff}r'_j - \text{eff}r^o_j}{\text{eff}r^o_j} \tag{21}$$

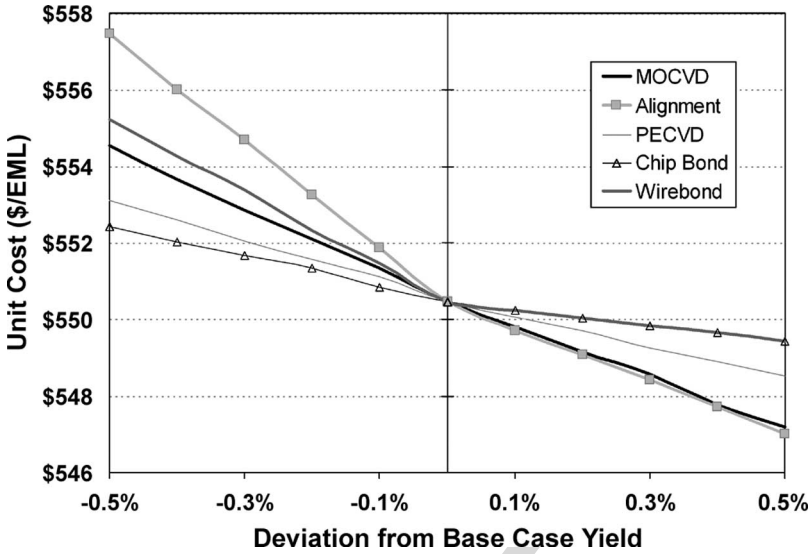

Fig. 9. Monolithically integrated EML cost sensitivity to changes in process yield (x-axis represents deviation from baseline-modeled yield).

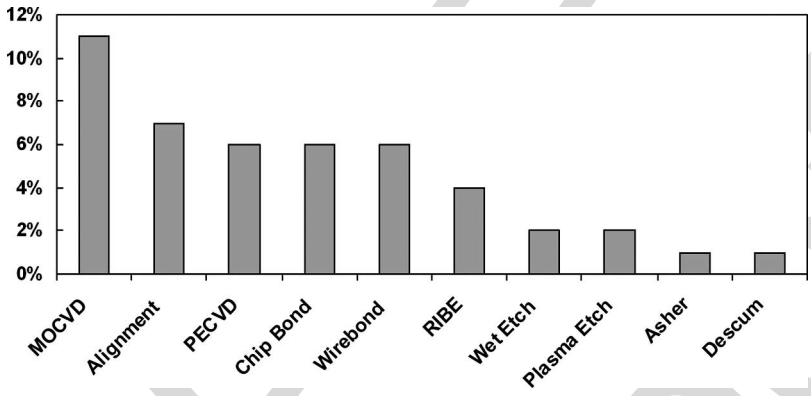

Fig. 10. Unit cost elasticity to reject rates (ε_{r_j}) for different process steps.

where r_j^o is the original reject rate for process j, where $j \in [1, \ldots, J]$, and J is the total number of processes; r'_j is the perturbed reject rate for process j; C^o is the total unit cost with all reject rates at original values; and C' is the total unit cost at the perturbed state. By normalizing change in cost against the percent change in reject rate, this elasticity attempts to account for the relative difficulty of lowering the reject rate of a process. Implicitly, this figure of merit assumes that improvements in low-yield processes should be easier to realize than for those processes with yields already at 98% or 99%, making them potentially better targets for improvement efforts.

Fig. 10 shows such an analysis for the monolithically integrated device using a uniform 0.1% decrease in reject rate for all processes. The elasticity results also show that changes in alignment and MOCVD reject rates have the largest impact on total unit cost. A 0.1% decrease in the reject rate (increase in the yield) of MOCVD generates savings at a rate ten times that of some other processes. This importance of MOCVD yield is not identified in an earlier paper by Stirk *et al.*, which provides instead a detailed analysis of the theoretical contributions of thermal mechanical stress and optical coupling to yield. Stirk *et al.*'s conclusions regarding thermal mechanical stress and optical coupling contributions to yield may be important, however, to improving process yields in alignment, which along with MOCVD has one of the largest impacts on the total unit cost [16].

Because processing defects are often difficult to detect until the final product is assembled, one of the largest yield hits is at the "Final Test." The Final Test represents the tests performed as the last step (step n) of the process. According to previous studies, thermal dissipation within the package, mechanical expansion and stress during both epitaxy and epoxy steps, and compound effects of component placement on optical coupling efficiency, play major roles in contributing to optical transceiver module yields experienced in this Final Test [16], [23]. Previous studies also suggest that for an integrated EML, the yield at the Final Test is mostly dependent on the coupling constant (κL) and the grating phase error [23]. Yields at the Final Test (Y_n) ranged from as low as 33% to 67% at observed facilities. Due to the continual improvement observed in the process, this paper assumes a "best practice" Final Test yield (Y_n) of 67%. In the model, the Final Test includes testing for laser light, current, and voltage; back facet monitor current, modulated power, line width, wavelength, alternating current extinction ratio, rise/fall time, side mode suppression ratio, mask margin, signal to noise ratio, and sensitivity and dispersion at one fiber length.

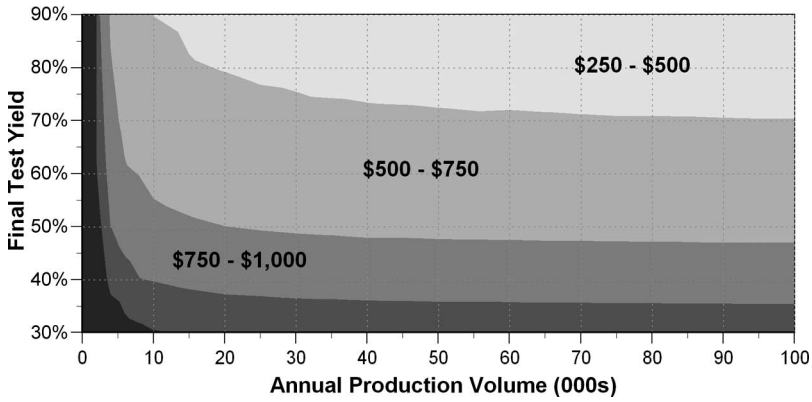

Fig. 11. Monolithically integrated device unit cost sensitivity to Final Test yield.

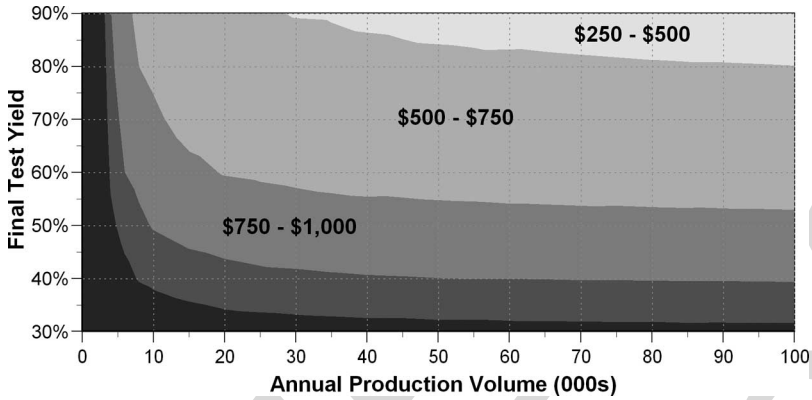

Fig. 12. Discrete laser and modulator devices in a single package cost sensitivity to Final Test yield.

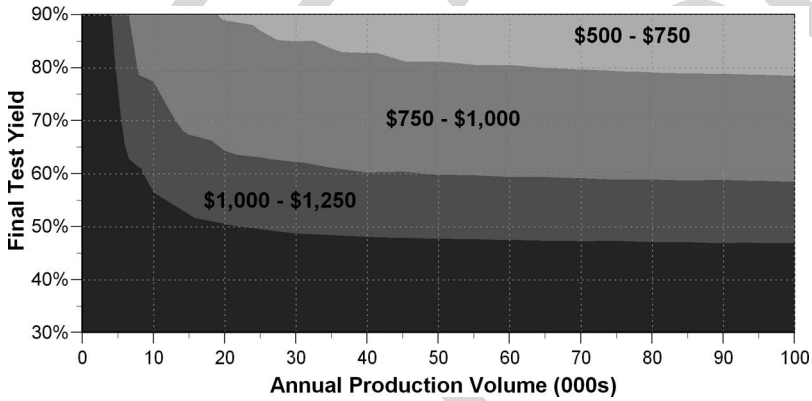

Fig. 13. Discretely packaged laser and modulator cost sensitivity to Final Test yield.

Figs. 11–13 present maps of the sensitivity of the final component cost to the yield experienced at the Final Test. The yield (Y_n) experienced at the Final Test, given that components have gone through over 100 steps to reach this stage, has an enormous impact on unit cost. A map of unit cost sensitivity to yield and production volume provides key insights on the Final Test yields necessary at different production volumes to achieve targeted unit costs.

Unit costs under \$1000 are essential to selling a laser modulator on today's market. As Figs. 11–13 show, the monolithically integrated EML can be produced at much lower yields than its discrete device counterparts, and still achieve production costs under \$1000, regardless of scale. For the base case yield of 67%, costs remain under \$1000 up through production volumes above 2800/year. In comparison, for the discretely produced device in a single package's production costs to fall under \$1000, yields and production volumes must be higher. For the 67% Final Test yield base case, annual production volumes must be above 4800 annually for the single-package discrete laser and modulator production costs to fall under \$1000. Yields

must be significantly higher for the discretely packaged product's production costs to fall under $1000. Production volumes must be above 15 000 annual units for the discretely packaged product to cost under $1000.

Some estimates suggest that it will be necessary for EML production costs to drop under $500 per unit within the next decade to remain competitive. Assuming that these products will at least monolithically integrate the laser and modulator, a set of Final Test yield and production demand objectives emerges. If production volumes rise to 100 000 units annually or more, the Final Test yield must only rise at around 3% beyond the current base case of 67%. If demand is expected to be such that production volumes will remain below 100 000 units annually, the Final Test yields required become far more difficult to achieve. With the current process assumptions, production costs cannot be brought under $500 for production volumes lower than 10 000. Notably, as pointed out by the earlier analysis of lidding yield, Final Test yield and annual production volumes are not the only parameters available for companies to improve. Processing parameters can be changed to improve yield, new equipment can be bought with better yield performances, and testing positions can be moved earlier in the process to allow yield hits to be felt earlier in the process, to just name a few. Given the results shown, further integration may have the most significant impact on lowering costs, despite resulting in lower yields.

The inherent lowering of the Final Test yield caused by placing more steps in series during monolithic integration has previously often been overlooked. Instead, alternative reasons for monolithic integration lowering yields, such as extended processing time and increasingly structured wafer surfaces [17], often dominate discussions. The results shown above are particularly significant because they suggest that even though integration will lead to less favorable yields, these integrated devices can achieve the same cost targets with lower Final Test yields than a discrete device. Thus, competency in other areas affecting yield discussed earlier—such as thermal dissipation within the package, mechanical expansion and stress during both epitaxy and epoxy steps, and compound effects of component placement on optical coupling efficiency—may be able to remain the same or even less in the monolithically integrated device and still achieve the same costs.

IV. Analysis and Conclusion

Integration has been a singular driving force for the explosion of microelectronics-based devices and the infusion of electronic products into every aspect of life [24]. As such, it should come as no surprise that realizing integration is a focus for many segments of the optoelectronics industry. Integration eliminates packaging expenses by removing both the physical artifact and the time-consuming and error-prone processes required to assemble the packages. With integration, however, comes complexity; complexity in both design and processing. This complexity increases the incidence of performance and processing failures, which translates into higher costs. The pace of integration must therefore be measured, balancing packaging gains against processing losses.

For the industry to effectively lower production costs, scarce development resources in design, manufacturing, and tooling must be carefully focused. PBCMs enable a targeted approach to cost reduction. This paper shows the ability of the CTR PBCM to assess the techno-economic characteristics of three integration strategies for high-performance laser modulator pairs. For each of the products evaluated, the CTR PBCM has provided the following key insights.

A. Role of Production Scale

Production volumes above 30 000 units/year are critical to reaching economies of scale. The unit cost of one monolithically integrated EML is $1110 if only 2000 are produced annually, but is $550 if 30 000 are produced annually (and $520 if 250 000 are produced annually). Given that the global markets for these products are currently not much higher than 30 000 units annually, the extreme cost pressures being faced by the industry should come as no surprise. Discussions of an opto-fab or extreme industry mergers may become necessary solutions unless global production volumes rise significantly above economies of scale in the near future. The quick technological turnover of such optical devices, however, may make outsourcing to a single fab either too difficult or too dangerous toward losses of IP. An alternative solution for firms needing to increase production volumes to reach economies of scale not evaluated in this paper is platform sharing across products and increasing the capability to run multiple products on a single line.

B. Cost Drivers/Cost Reduction Opportunities

In terms of categories of processes, the top three cost drivers for all of the integration levels analyzed were packaging, prepackage assembly, and testing. Alone, these three drivers comprise 82%, 81%, and 87% of total costs for the monolithically integrated laser and modulator, discrete laser and modulator with single package, and discretely packaged laser and modulator devices, respectively. Given this dominance of packaging and of the specific benefits of integration, it is not surprising that the monolithic design provides cost advantages over such a broad range of strategic and operational conditions. Notably, the unit costs per good device presented in this paper include the direct costs of testing. The lost value added for rejected components is shown in the step where the expense is originally incurred. Testing is clearly key for delivering quality product. These results, however, show that both judicious application and technological development around testing, in particular, reducing the cycle times for testing, would have a strong impact on manufactured cost.

Improvements in MOCVD and alignment process yields would have the largest consequences for unit cost reduction in a monolithically integrated laser modulator device. A 0.1% improvement in the MOCVD yield would reduce the final unit cost at a rate ten times that of other processes. For devices with different process flows, MOCVD and alignment may or may not be the processes whose yield improvements would have

the most significant impact on cost; however, analyses such as this one would readily identify effective targets for yield improvements.

C. Role of Yield

Along with production volume, production yield is an essential part of manufacturing cost; improving that yield will be necessary to meeting long-term cost targets within the optoelectronics industry. Given the process assumptions made in this study, to reach cost targets of $500/monolithically integrated EML with production volumes of 100 000 units annually, yields at the final product test must be at or above 70%. If yields at the Final Test drop below 36%, costs cannot be brought below $1000/monolithically integrated EML regardless of scale.

Achieving higher levels of integration requires more process steps in series. This manufacturing reality results in lower yields. For example, while the discretely processed laser and modulator in a single package have cumulative yields of 3.9% and 7.9%, respectively, the monolithically integrated EML's cumulative yield, using the same processing techniques, is only 2.3%. Despite these differences in cumulative yield, the monolithically integrated EML costs less than the discrete laser and modulator in a single package, regardless of scale. The complexity that comes with higher levels of integration leads to greater process difficulties and, therefore, lower process yields. However, the cost advantages of the integrated designs do not require as high yields to reach low price points. For the monolithically integrated EML, with annual production volumes of 100 000, only 70% of the products produced must pass the Final Test for costs to reach $500/unit. In contrast, for the discrete laser and modulator in a single package, given annual production volumes of 100 000, 80% of the products produced must pass the Final Test for costs to reach this low.

The benefits of integration are even more drastic when going from separately packaged devices to a single package. Given the processing assumptions in this study, the discretely packaged laser and modulator cannot meet cost targets of $500/unit (where one "unit" includes both the packaged laser and the packaged modulator), regardless of Final Test yield or production scale. To meet cost targets of $1000/unit for the discretely packaged laser and modulator product requires Final Test yields above 60% with annual production volumes of 100 000 products/year.

Ultimately, manufacturing cost reduction will be key to the long-term growth of optoelectronic component sales. Realizing this will require both organizational and technological changes throughout the industry. On the technological front, engineers have many design options—materials, processes, and architectures. Unfortunately, neither engineering nor traditional accounting methods are individually able to resolve the cost impact of novel technical changes. This paper presents a method, i.e., PBCM, that incorporates the strengths of both methods to provide those insights. As demonstrated in the case analysis, the model identifies both the strategic strengths of an integrated design and pinpointed specific development targets that will allow production economics to be improved effectively.

APPENDIX
PROCESS FLOW 1: MONOLITHICALLY INTEGRATED LASER AND MODULATOR

STEP	FUNCTION	DESCRIPTION	Wafer/Bar/Die	Next Step
1	Clean	incom. wafer clean	WAFER	2
2	Incoming_Inspection	Incoming Inspection	WAFER	3
3	MOCVD	70nm InGaAsP (1.25) on InP	WAFER	4
4	MOCVD	6.7nm InGaAsP (1.55) and 15.1nm InGaAsP (1.25) on InP	WAFER	6
5	MOCVD	70nm InGaAsP (1.25) on InP	WAFER	6
6	PL_Test	Post Depositn	WAFER	7
7	PECVD	100nm SiN	WAFER	8
8	HMDS	HMDS Prime	WAFER	9
9	SpinOn_Resist	1.5 micron Polyimide	WAFER	10
10	Prebake	Prebake PMMA	WAFER	11
11	Litho	Lithography	WAFER	12
12	Develop	Develops PMMA	WAFER	13
13	Postbake	Postbake PMMA	WAFER	14
14	Plasma_Etch	100nm PECVD SiN	WAFER	15
15	Asher	Ash 500nm PMMA	WAFER	16
16	Visual_Test	Post Ash Visual	WAFER	17
17	RIBE	256nm InGaAsP	WAFER	18
18	PL_Test	Autom. Inspectn	WAFER	19
19	MOCVD	50 nm InGaAsP (1.10) on InP	WAFER	20
20	MOCVD	9.7nm InGaAsP (1.55) and 5.0nm InGaAsP (1.10) on InP	WAFER	21
21	MOCVD	50 nm InGaAsP (1.10) on InP	WAFER	22
22	Wet_Etch	100 nm PECVD SiN	WAFER	23
23	Spin_Dry	-	WAFER	24
24	PECVD	100nm SiN	WAFER	25
25	HMDS	HMDS Prime	WAFER	26
26	SpinOn_Resist	1.5 micron Polyimide	WAFER	27
27	Prebake	Prebake PMMA	WAFER	28
28	Litho	Lithography	WAFER	29
29	Develop	Develops PMMA	WAFER	30
30	Postbake	Postbake PMMA	WAFER	31
31	Plasma_Etch	100nm PECVD SiN	WAFER	32
32	Asher	Ash 500nm PMMA	WAFER	33
33	RIBE	114nm InGaAsP	WAFER	34
34	Wet_Etch	100 nm PECVD SiN	WAFER	35
35	Spin_Dry	-	WAFER	36
36	Descum	Pre-epi surface clean	WAFER	37
37	MOCVD	120nm Undoped InP Overgrowth	WAFER	38
38	MOCVD	1000nm p-type InP	WAFER	39
39	PECVD	1000nm SiN	WAFER	40
40	HMDS	HMDS Prime	WAFER	41
41	SpinOn_Resist	1.5 micron Polyimide	WAFER	42
42	Prebake	Prebake PMMA	WAFER	43
43	Litho	Lithography	WAFER	44
44	Develop	Develops PMMA	WAFER	45
45	Postbake	Postbake PMMA	WAFER	46
46	Plasma_Etch	1000nm PECVD SiN	WAFER	47
47	RIBE	1000nm InP	WAFER	48
48	Asher	Ash 500nm PMMA	WAFER	49
49	Wet_Etch	1000 nm PECVD SiN	WAFER	50
50	Spin_Dry	-	WAFER	51
51	SpinOn_Resist	1.5 micron Polyimide	WAFER	52
52	Cure	Polyimide Cure	WAFER	53
53	RIBE	500nm Polyimide	WAFER	54
54	PECVD	100nm SiN	WAFER	55
55	HMDS	HMDS Prime	WAFER	56
56	SpinOn_Resist	1.5 micron Polyimide	WAFER	57
57	Prebake	Prebake PMMA	WAFER	58
58	Litho	Lithography	WAFER	59
59	Develop	Develops PMMA	WAFER	60
60	Postbake	Postbake PMMA	WAFER	61
61	Plasma_Etch	100nm PECVD SiN	WAFER	62
62	RIBE	1000nm InP	WAFER	63
63	Hion_Implant	1 micron deep H2 Isol. betw. Mod. and laser	WAFER	64
64	Asher	Ash 500nm PMMA	WAFER	65
65	Wet_Etch	100 nm PECVD SiN	WAFER	66
66	Spin_Dry	-	WAFER	67
67	Anneal	Post Implant	WAFER	68
68	Descum	Pre-epi surface clean	WAFER	69
69	Litho	Photolithography	WAFER	70
70	Ebeam	20nm Ti/ 20nm Pt/ 300 nm Au	WAFER	71
71	Anneal	Anneal Ti/Pt/Au	WAFER	72
72	Metal_Liftoff	Strips AZ512	WAFER	73
73	Lapping	-	WAFER	74
74	Clean	post-lapping clean	WAFER	75
75	Spin_Dry	-	WAFER	76
76	Ebeam	25nm Ni/32.5nm Ge/150 nm Au	WAFER	77
77	Anneal	Anneal Ni/Ge/Au	WAFER	78
78	Wafer_Cleave	-	WAFER	79
79	Bar_Cleave	-	BAR	80
80	HR_Coating	-	DIE	81
81	AR_Coating	-	DIE	82
82	Isolated_Die_Test	Post Plant Transfer Test	DIE	83
83	Chip_Bond	COC	DIE	84
84	Cure	COC Epoxy Bond & Cure	DIE	85
85	Wirebond	COC	DIE	86
86	Visual_Test	Post-Wire bond	DIE	87
87	Burn_In	Burn In 1	DIE	88
88	EalacTest	-	DIE	89
89	Burn_In	Burn In 2+3	DIE	90
90	EalacTest	-	DIE	91
91	Visual_Test	Final COC Visual	DIE	92
92	Cooler_Assembly	-	DIE	93

93	Cooler_Assembly	-	DIE	94
94	Assembly_Test	Cooler Asmbly AC Test	DIE	95
95	Bench_Assembly	Sled Assembly	DIE	96
96	Bench_Attach	-	DIE	97
97	Wirebond	Assembly	DIE	98
98	Visual_Test	Assmbly Visual	DIE	99
99	Alignment	Alignmnt 1 -- Horizontal Welder	DIE	100
100	Alignment	Alignmnt 2 -- Horizontal Welder	DIE	101
101	Visual_Test	Pre-Lid Visual	DIE	102
102	Bake	Nitrogen Bake	DIE	103
103	Lidding	-	DIE	104
104	Package_Clean	Plasma Clean	DIE	105
105	Fiber_Attach	-	DIE	106
106	Sleeve_Attach	-	DIE	107
107	Assembly_Test	Post-Bake Test	DIE	108
108	Temp_Cycle	-	DIE	109
109	Assembly_Test	AC Resistance Test	DIE	110
110	Assembly_Test	Final Test	DIE	111
111	Assembly_Test	Special Test	DIE	END

PROCESS FLOW 2: DISCRETE LASER AND MODULATOR IN A SINGLE PACKAGE

STEP	FUNCTION	DESCRIPTION	Wafer/Bar/Die	Next Step
1	Clean	incom. wafer clean	WAFER	2
2	Incoming_Inspection	Incoming Inspection	WAFER	3
3	MOCVD	70nm InGaAsP (1.25) on InP	WAFER	4
4	MOCVD	6.7nm InGaAsP (1.55) and 15.1nm InGaAsP (1.25) on InP	WAFER	5
5	MOCVD	70nm InGaAsP (1.25) on InP	WAFER	6
6	PL_Test	Post Depositn	WAFER	7
7	PECVD	100nm SiN	WAFER	8
8	HMDS	HMDS Prime	WAFER	9
9	SpinOn_Resist	1.5 micron Polyimide	WAFER	10
10	Prebake	Prebake PMMA	WAFER	11
11	Litho	Lithography	WAFER	12
12	Develop	Develops PMMA	WAFER	13
13	Postbake	Postbake PMMA	WAFER	14
14	Plasma_Etch	100nm PECVD SiN	WAFER	15
15	Asher	Ash 500nm PMMA	WAFER	16
16	RIBE	114nm InGaAsP	WAFER	17
17	Wet_Etch	100 nm PECVD SiN	WAFER	18
18	Spin_Dry	-	WAFER	19
19	Descum	Pre-epi surface clean	WAFER	20
20	MOCVD	120nm Undoped InP Overgrowth	WAFER	21
21	MOCVD	1000nm p-type InP	WAFER	22
22	PECVD	1000nm SiN	WAFER	23
23	HMDS	HMDS Prime	WAFER	24
24	SpinOn_Resist	1.5 micron Polyimide	WAFER	25
25	Prebake	Prebake PMMA	WAFER	26
26	Litho	Lithography	WAFER	27
27	Develop	Develops PMMA	WAFER	28
28	Postbake	Postbake PMMA	WAFER	29
29	Plasma_Etch	1000nm PECVD SiN	WAFER	30
30	RIBE	1000nm InP	WAFER	31
31	Asher	Ash 500nm PMMA	WAFER	32
32	Wet_Etch	1000 nm PECVD SiN	WAFER	33
33	Spin_Dry	-	WAFER	34
34	SpinOn_Resist	1.5 micron Polyimide	WAFER	35
35	Cure	Polyimide Cure	WAFER	36
36	RIBE	500nm Polyimide	WAFER	37
37	PECVD	100nm SiN	WAFER	38
38	HMDS	HMDS Prime	WAFER	39
39	SpinOn_Resist	1.5 micron Polyimide	WAFER	40
40	Prebake	Prebake PMMA	WAFER	41
41	Litho	Lithography	WAFER	42
42	Develop	Develops PMMA	WAFER	43
43	Postbake	Postbake PMMA	WAFER	44
44	Plasma_Etch	100nm PECVD SiN	WAFER	45
45	RIBE	1000nm InP	WAFER	46
46	Hion_Implant	1 micron deep H2 Isol. betw. Mod. and laser	WAFER	47
47	Asher	Ash 500nm PMMA	WAFER	48
48	Wet_Etch	100 nm PECVD SiN	WAFER	49
49	Spin_Dry	-	WAFER	50
50	Anneal	Post Implant	WAFER	51
51	Descum	Pre-epi surface clean	WAFER	52
52	Litho	Photolithography	WAFER	53
53	Ebeam	20nm Ti/ 20nm Pt/ 300 nm Au	WAFER	54
54	Anneal	Anneal Ti/Pt/Au	WAFER	55
55	Metal_Liftoff	Strips AZ512	WAFER	56
56	Lapping	-	WAFER	57
57	Clean	post-lapping clean	WAFER	58
58	Spin_Dry	-	WAFER	59
59	Ebeam	25nm Ni/32.5nm Ge/150 nm Au	WAFER	60
60	Anneal	Anneal Ni/Ge/Au	WAFER	61
61	Wafer_Cleave	-	BAR	62
62	Bar_Cleave	-	DIE	63
63	HR_Coating	-	DIE	64
64	AR_Coating	-	DIE	65
65	Isolated_Die_Test	Post Plant Transfer Test	DIE	66
66	Chip_Bond	COC	DIE	67
67	Cure	COC Epoxy Bond & Cure	DIE	68
68	Wirebond	COC	DIE	69
69	Visual_Test	Post-Wire bond	DIE	70
70	Burn_In	Burn In 1	DIE	71
71	EalacTest	-	DIE	72
72	Burn_In	Burn In 2+3	DIE	73
73	EalacTest	-	DIE	74
74	Visual_Test	Final COC Visual	DIE	75
75	Cooler_Assembly	-	DIE	76
76	Cooler_Assembly	-	DIE	77
77	Assembly_Test	Cooler Asmbly AC Test	DIE	149
78	Clean	incom. wafer clean	WAFER	79
79	Incoming_Inspection	Incoming Inspection	WAFER	80
80	MOCVD	50 nm InGaAsP (1.10) on InP	WAFER	81
81	MOCVD	9.7nm InGaAsP (1.55) and 5.0nm InGaAsP (1.10) on InP	WAFER	82
82	MOCVD	50 nm InGaAsP (1.10) on InP	WAFER	83
83	PL_Test	Post Depositn	WAFER	84
84	HMDS	HMDS Prime	WAFER	85
85	SpinOn_Resist	1.5 micron Polyimide	WAFER	86
86	Prebake	Prebake PMMA	WAFER	87
87	Litho	Lithography	WAFER	88
88	Develop	Develops PMMA	WAFER	89
89	Postbake	Postbake PMMA	WAFER	90
90	Plasma_Etch	100nm PECVD SiN	WAFER	91
91	Asher	Ash 500nm PMMA	WAFER	92
92	RIBE	114nm InGaAsP	WAFER	93
93	Wet_Etch	100 nm PECVD SiN	WAFER	94
94	Spin_Dry	-	WAFER	95
95	Descum	Pre-epi surface clean	WAFER	96
96	MOCVD	120nm Undoped InP Overgrowth	WAFER	97
97	MOCVD	1000nm p-type InP	WAFER	98
98	PECVD	1000nm SiN	WAFER	99
99	HMDS	HMDS Prime	WAFER	100
100	SpinOn_Resist	1.5 micron Polyimide	WAFER	101
101	Prebake	Prebake PMMA	WAFER	102
102	Litho	Lithography	WAFER	103
103	Develop	Develops PMMA	WAFER	104
104	Postbake	Postbake PMMA	WAFER	105
105	Plasma_Etch	1000nm PECVD SiN	WAFER	106
106	RIBE	1000nm InP	WAFER	107
107	Asher	Ash 500nm PMMA	WAFER	108
108	Wet_Etch	1000 nm PECVD SiN	WAFER	109
109	Spin_Dry	-	WAFER	110
110	SpinOn_Resist	1.5 micron Polyimide	WAFER	111
111	Cure	Polyimide Cure	WAFER	112
112	RIBE	500nm Polyimide	WAFER	113
113	PECVD	100nm SiN	WAFER	114
114	HMDS	HMDS Prime	WAFER	115
115	SpinOn_Resist	1.5 micron Polyimide	WAFER	116
116	Prebake	Prebake PMMA	WAFER	117
117	Litho	Lithography	WAFER	118
118	Develop	Develops PMMA	WAFER	119
119	Postbake	Postbake PMMA	WAFER	120
120	Plasma_Etch	100nm PECVD SiN	WAFER	121
121	RIBE	1000nm InP	WAFER	122
122	Hion_Implant	1 micron deep H2 Isol. betw. Mod. and laser	WAFER	123
123	Asher	Ash 500nm PMMA	WAFER	124
124	Wet_Etch	100 nm PECVD SiN	WAFER	125
125	Spin_Dry	-	WAFER	126
126	Anneal	Post Implant	WAFER	127
127	Descum	Pre-epi surface clean	WAFER	128
128	Litho	Photolithography	WAFER	129
129	Ebeam	20nm Ti/ 20nm Pt/ 300 nm Au	WAFER	130
130	Anneal	Anneal Ti/Pt/Au	WAFER	131
131	Metal_Liftoff	Strips AZ512		132
132	Lapping	-	WAFER	133
133	Clean	post-lapping clean	WAFER	134
134	Spin_Dry	-	WAFER	135
135	Ebeam	25nm Ni/32.5nm Ge/150 nm Au	WAFER	136
136	Anneal	Anneal Ni/Ge/Au	WAFER	137
137	Wafer_Cleave	-	WAFER	138
138	Bar_Cleave	-	BAR	139
139	HR_Coating	-	DIE	140
140	AR_Coating	-	DIE	141
141	Isolated_Die_Test	Post Plant Transfer Test	DIE	142
142	Chip_Bond	COC	DIE	143
143	Cure	COC Epoxy Bond & Cure	DIE	144
144	Chip_Bond	COC	DIE	145
145	Wirebond	COC	DIE	146
146	Visual_Test	Post-Wire bond	DIE	147
147	Assembly_Test	Post-Bake Test	DIE	148
148	Visual_Test	Post-Wire bond	DIE	149
149	Bench_Assembly	Sled Assembly	DIE	150
150	Bench_Attach	-	DIE	151
151	Wirebond	Assembly	DIE	152
152	Visual_Test	Assmbly Visual	DIE	153
153	Alignment	Alignmnt 1 -- Horizontal Welder	DIE	154
154	Alignment	Alignmnt 2 -- Horizontal Welder	DIE	155
155	Visual_Test	Pre-Lid Visual	DIE	156
156	Bake	Nitrogen Bake	DIE	157
157	Lidding	-	DIE	158
158	Package_Clean	Plasma Clean	DIE	159
159	Fiber_Attach	-	DIE	160
160	Sleeve_Attach	-	DIE	161
161	Assembly_Test	Post-Bake Test	DIE	162
162	Temp_Cycle	-	DIE	163
163	Assembly_Test	AC Resistnc Test	DIE	164
164	Assembly_Test	Final Test	DIE	165
165	Assembly_Test	Special Test	DIE	END

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