Robust System Design

By: Subhasish Mitra
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Abstract
Today’s mainstream electronic systems typically assume that transistors and interconnects operate correctly over their useful lifetime. With enormous complexity and significantly increased vulnerability to failures compared to the past, future system designs cannot rely on such assumptions. At the same time, there is explosive growth in our dependency on such systems. For example, in 2009, a glitch in a single circuit board of the air-traffic control system resulted in hundreds of flights being canceled or delayed.

With extreme miniaturization of circuits, factors such as transient errors, device degradation, and variability induced by manufacturing and operating conditions are becoming important. While design margins are being squeezed to achieve high energy efficiency, expanded design margins are required to cope with variability and transistor aging. Even if error rates stay constant on a per-bit basis, total chip-level error rates grow with the scale of integration. Moreover, difficulties with traditional burn-in can leave early-life failures unscreened.

This talk will address the following major robust system design goals:

- New approaches to thorough post-silicon validation that scale with tremendous growth in complexity
- Cost-effective tolerance and prediction of failures in hardware during system operation
- A practical way to overcome substantial inherent imperfections in emerging nanotechnologies

Significant recent progress in robust system design impacts almost every aspect of future systems, from ultra-large-scale networked systems, all the way to their nanoscale components.

About the Speaker:
Prof. Subhasish Mitra directs the Robust Systems Group in the Department of Electrical Engineering and the Department of Computer Science of Stanford University. Before joining Stanford, he was a Principal Engineer at Intel Corporation.

Prof. Mitra’s research interests include robust system design, VLSI design, CAD, validation and test, and emerging nanotechnologies. His X-Compact technique for test compression has been used in more than 50 Intel products, and has influenced major CAD tools. The IFRA technology for post-silicon validation, created jointly with his student, was characterized as “a breakthrough” in the Communications of the ACM. His work on the first demonstration of carbon nanotube imperfection-immune VLSI circuits, jointly with his students and collaborators, was selected by NSF as a Research Highlight to the US Congress, and was highlighted as “a significant breakthrough” by the Semiconductor Research Corporation and the MIT Technology Review.

Prof. Mitra’s major honors include the Presidential Early Career Award for Scientists and Engineers from the White House, IEEE CAS/CEDA Pederson Award for the IEEE Transactions on CAD Best Paper, Terman Fellowship, and the Intel Achievement Award, Intel’s highest corporate honor. He and his students presented award-winning papers at several major conferences: IEEE/ACM Design Automation Conference, IEEE VLSI Test Symposium, Symposium on VLSI Technology, IEEE International Test Conference, and the Intel Design and Test Technology Conference. Prof. Mitra also serves as an invited member on DARPA’s Information Science and Technology Board.